Article

Average Current Mode Control of a DC–DC Boost Converter to Reduce the Decoupling Capacitance at the PV Array Output

Sobhan Mohamadian, Concettina Buccella [ID] and Carlo Cecati *[ID]

Department of Information Engineering, Computer Science and Mathematics, University of L'Aquila, 67100 L'Aquila, Italy
* Correspondence: carlo.cecati@univaq.it

Abstract: Due to the full-wave AC–DC power conversion, second-order frequency oscillations of current and voltage are created in single-phase PV-grid-connected inverters. These oscillations propagate toward the input and adversely affect the PV power utilization ratio. Large power decoupling capacitors are the preliminary solution for coping with voltage ripples across PVs, and they decrease the lifetime of the overall system. This paper proposes the average current mode control (ACMC) of the input inductor in a DC–DC boost converter in a double-stage PV power conversion system. Through extensive explanations of the modeling and control of a DC–DC boost converter, it is shown that the ACMC reduces the propagation of the second-order frequency components (SOFCs) toward the input PV array. Two controllers—a proportional–integral controller and an integral single-lead controller—are considered to adjust the average value of the PV output current in a single-loop control structure. This control approach is simple to implement and exhibits high impedance to current oscillatory components, which, in turn, reduces the size of the required capacitance.

Keywords: boost converter; current control; photovoltaic array; power decoupling capacitor; second-order oscillations; utilization ratio

1. Introduction

Single-phase photovoltaic (PV) converters usually consist of a DC–DC boost converter and an H-bridge inverter. The DC–DC converter sets the output voltage and current of the PV array at its maximum power point (MPP). Furthermore, it increases the PV array's output voltage to supply the DC-link of the H-bridge inverter with a voltage capable of injecting active power into the AC grid.

The DC-link current consists of an average or DC component and a second-order frequency component (SOFC) with a considerable amplitude. In renewable energies, such as photovoltaics and fuel cell applications, the SFOC propagates along the DC side and results in either efficacy aggravation of the MPP tracking process in the PV or the lifetime reduction of the fuel cell [1,2]. The imbalance existing between the output DC power of a PV and the input power of the inverter must be compensated with a relatively large capacitor. For instance, a 13.9 mF capacitor is needed to reduce the ripple voltage across the PV array in a 200 W AC module below 1% [1]. Consequently, electrolytic capacitors are the only practical option. However, these capacitors have a lower lifetime than that of a PV array and other power electronic components, which remarkably reduces the overall lifetime of the system. Thus, various methods and circuit configurations have been proposed in the literature to replace electrolytic capacitors with film (non-polarized) types in either isolated or double-stage non-isolated converters.

A complete literature survey was conducted in [3] on structures intended to reduce the capacitance in micro-inverters (or AC modules [4]). AC modules were subsumed under the category of isolated converters. Based on this literature survey, the required capacitance for power decoupling in AC modules can be reduced by either additional decoupling circuits or

modifications in the control strategies. Moreover, a third terminal (an additional H-bridge) called a ripple port was utilized in [5] in a high-frequency double-stage-module-integrated inverter to eliminate the SOFC. In a similar study, a current decoupling tank was proposed in [6] to reduce the power decoupling capacitance in a 240 W AC module. This circuit was composed of all components needed to build a DC–DC converter and placed at the tertiary of a high-frequency transformer. A series power decoupling circuit based on a single-stage flyback converter was introduced in [7] for a 100 W AC module.

A combination of proportional–integral (PI) and repetitive controllers was proposed in [8] to reduce the SOFC in the current of an input inductor in a boost converter of non-isolated double-stage converters. A multi-phase DC–DC converter and an inverter were used in [2] to inject the output power of a 5 kW fuel cell into an AC grid. In this reference, an internal-filter-current control loop was added to the voltage control loop of an AC–DC rectifier with a larger bandwidth than the external voltage control loop. The increase in the output impedance in the DC–DC converter through the control system is another approach that could be adopted to reduce the propagation of SOFCs to the input [9,10]. An internal PI control loop was designed for the inductor of a boost converter in [9] to increase the converter's output impedance. On the other hand, a parallel path with a nonlinear gain was designed to improve the dynamic response of the output voltage control loop. Similarly, sliding-mode control was utilized in [10] to increase the output impedance of a 1 kW boost converter in a double-stage power conversion system. A new circuit topology of a double-stage converter with an additional capacitor and diode was employed in [11] with a new control strategy for power decoupling purposes. An additional active low-frequency ripple control circuit (ALFRC) was able to inject the compensating SOFC into the DC-link of an H-bridge module [12,13]. An adaptive linear neural network and sliding-mode controller were used in [12] to provide this compensating SOFC. On the other hand, a current integrator (virtual capacitor) was introduced in [13] instead of unit feedback in a control system. The ALFRC circuit was an H-bridge or a buck–boost converter in [12,13], respectively.

A control structure based on average current mode control (ACMC) is proposed in this paper for the PV DC–DC boost converters to reduce the propagation of SFOCs to the input DC supply. A converter with current mode control (CMC) benefits from improved dynamic response against the input and output disturbances compared to those with the voltage control mode [14]. Two common approaches to implementing CMC are peak current mode control (PCMC) and average current mode control (ACMC). Compared to PCMC, ACMC is advantageous in terms of its higher accuracy in following the average current of the inductor, the elimination of slope compensations, and improved noise immunity [14]. For these reasons, ACMC is widely used in boost converters in power factor correction systems [15–17]. This paper will show that the employment of a simple controller (PI controller or integral single-lead controller (ISLC)) in the ACMC method can prevent the propagation of SFOCs to the PV array without the need to use more complicated control structures, such as a sliding-mode [10] or repetitive controller [8]. Furthermore, contrary to the work in [11–13], the need for additional circuits, such as ALFRC, is removed. This paper presents a detailed procedure for the design of the controller parameters. In addition, the maximum required power decoupling capacitance is computed based on the proposed control structure to meet the minimum permissible utilization factor of the PV array. It is shown that the size of this capacitance is remarkably reduced with respect to the conventional approaches. This relatively low capacitance enables the use of film capacitors, resulting in an increase in the expected lifetime of the inverter.

This paper is structured as follows—the concept of the utilization factor in a PV array considering its output current ripple is explained in Section 2. The parameters of the PV array under study are introduced and a brief highlighting of the hardware design are presented in Section 3. These parameters are required to extract the transfer functions of the DC–DC converter and controller, as explained in Section 4. Then, the lowest possible capacitance needed to have a permissible utilization factor for the PV array is identified

in Section 5, and the claims for reducing the SFOCs with the low value of capacitance are verified via simulation studies. Finally, the paper is concluded in Section 6.

2. Output Current Ripple and Power Decoupling Capacitor of a PV Array

The voltage and current ripples at the output of a PV array reduce its available average output power [4]. To calculate the average output power in the presence of output voltage and current ripples, we consider the PV array to be working at its MPP. Thus,

$$u_{PV} = U_{MPP} + \widetilde{u} = U_{MPP} + \hat{u}\sin(2\omega t), \tag{1}$$

where $\widetilde{u}$ is the ripple component (SOFC) of the PV voltage (u_{PV}), $\hat{u}$ is the amplitude of the SOFC, U_{MPP} is the PV voltage at the MPP, and ω is the angular frequency of the single-phase grid. The output current of the PV array, which is a series or a series/parallel connection of diodes, is calculated as a function of its voltage and based on its voltage–current characteristics. As described in [4], this function can be approximated as a polynomial Taylor equation as follows:

$$i_{PV} = k_1 u_{PV}^2 + k_2 u_{PV} + k_3 = I_{MPP} + \widetilde{i}, \tag{2}$$

where $\widetilde{i}$ is the ripple component of the array current and k_1, k_2, k_3 are coefficients that describe the second-order Taylor approximation. I_{MPP} is the PV output current at the MPP. Accordingly, the PV's instantaneous output power is

$$p_{PV} = u_{PV}i_{PV} = (U_{MPP} + \hat{u}\sin(2\omega t))\left(k_1(U_{MPP} + \widetilde{u})^2 + k_2(U_{MPP} + \widetilde{u}) + k_3\right). \tag{3}$$

By taking the integral of the two sides in (3) in a period of $T = 2\pi/\omega$, the average power, P_{PV}, is calculated as

$$P_{PV} = P_{MPP} + \frac{(3U_{MPP}k_1 + k_2)\hat{u}^2}{2}, \tag{4}$$

where $P_{MPP} = U_{MPP}I_{MPP}$. The utilization factor, k_{PV}, is defined as the ratio of average power generated in (4) to the available power P_{MPP} at the MPP:

$$k_{PV} = \frac{P_{PV}}{P_{MMP}} = 1 + \frac{(3U_{MPP}k_1 + k_2)\hat{u}^2}{2P_{MPP}}. \tag{5}$$

Thus, the maximum permissible voltage ripple needed to obtain a desired value of k_{PV} is

$$\hat{u} = \sqrt{\frac{(k_{PV} - 1)2P_{MPP}}{3U_{MPP}k_1 + k_2}}. \tag{6}$$

Since Taylor approximation was utilized to obtain (6), the value of k_{PV} should not be less than 0.98 to keep the computational error in the permissible range [4]. In addition, a low value of k_{PV} is not desired.

For typical values of k_1 and k_2, k_{PV} decreases as the SOFC of the output voltage increases. As a solution, a capacitance is added in parallel to the PV array as the energy storage. Figure 1 shows a block diagram of the complex of the DC–DC boost converter and grid-connected inverter, where the power decoupling capacitor is placed across the PV array. In this figure, i_g and v_g are the grid current and voltage, respectively, with the following equations:

$$i_g = I_m\sin(\omega t - \varphi); \qquad v_g = V_m\sin(\omega t), \tag{7}$$

where I_m and V_m are the peak of the grid current and voltage and φ is the power factor angle. Disregarding the losses of the inverter and boost converter, $p_i = p_g$; thus:

$$u_{PV}i_i = v_g i_g \Rightarrow i_i = \frac{V_m I_m \sin(\omega t) \sin(\omega t - \varphi)}{u_{PV}}. \tag{8}$$
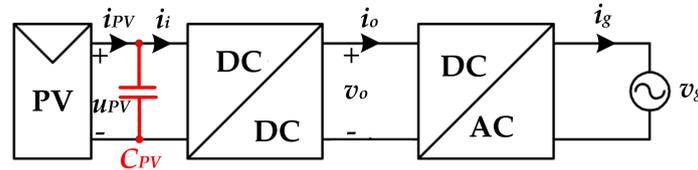
Figure 1. Power decoupling capacitor in parallel with the PV array and DC–DC boost converter.

Normally, φ is set to zero (unity power factor operation) in the control of the grid-connected inverter [18]. In this case, (8) is simplified to

$$i_i = \frac{V_m I_m}{u_{PV}} \sin^2(\omega t) = \frac{V_m I_m}{u_{PV}} \left(\frac{1 - \cos(2\omega t)}{2} \right) = I_{MPP} - I_{MPP} \cos(2\omega t) \tag{9}$$

i_i in (9) consists of a ripple or AC component and a DC component, I_{MPP}. Since the impedance of the capacitive branch is low enough, it is reasonable to assume that the whole ripple component passes through C_{PV} and generates a ripple voltage equal to

$$\tilde{u} = \frac{I_{MPP}}{C_{PV}} \int \cos(2\omega t) dt = \frac{I_{MPP}}{2\omega C_{PV}} \sin(2\omega t) = \hat{u} \sin(2\omega t). \tag{10}$$

Therefore, the maximum amplitude of the ripple voltage is equal to

$$\hat{u} = \frac{I_{MPP}}{2\omega C_{PV}} = \frac{P_{MPP}}{2\omega C_{PV} U_{MPP}}. \tag{11}$$

By combining (6) and (11), the minimum required capacitance to obtain the minimum permissible k_{PV} is obtained as

$$C_{PV} \geq \frac{P_{MPP}}{2\omega U_{MPP}\sqrt{\frac{(k_{PV}-1)2P_{MPP}}{3U_{MPP}k_1+k_2}}}. \tag{12}$$

Equation (12) results in a relatively large capacitance that can be accomplished solely with electrolytic capacitors. On the other hand, the electrolytic capacitors are counted as a distinguishing factor in the lifetime of PV inverters.

It should be noted that the concept of single-stage power conversion was utilized in the formula presented in this section. This means that the DC-link capacitor was eliminated in the double-stage power conversion process. In other words, theoretically, there will be no need for the DC-link capacitor as long as the desired value of k_{PV} is accomplished by the proposed control structure.

3. Design of Energy Storage Elements for the PV Array under Study

Figure 2a shows the circuit of the DC–DC boost converter. In this section, the energy storage elements—L and C in Figure 2a—are designed. For this purpose, the BP Solar BP4170B module was selected as the PV array, and the specifications were available from MATLAB models. The overall specifications are listed in Table 1. In addition, for this case study, $k_1 = -2.631 \times 10^{-4}$, $k_2 = 0.1066$, and $k_3 = -5.9665$. It should be mentioned that k_1, k_2, k_3 were calculated based on the parameters in Table 1 and according to the procedure explained in [4]. According to Table 1, the maximum achievable power was 170.88 W for each module. Therefore, a series connection of six modules was needed to obtain 1 kW

of output power. Table 2 summarizes the operating points required to design the energy storage elements and switching devices of the boost converter. Based on this table, the MPP voltage and current at a maximum irradiation of $1\,\mathrm{kW/m^2}$ were $V_{MPPmax} = 213.6\,\mathrm{V}$ and $I_{MPPmax} = 4.8\,\mathrm{A}$, respectively. For the minimum irradiation, i.e., $50\,\mathrm{W/m^2}$, these were $V_{MPPmin} = 195.4\,\mathrm{V}$ and $I_{MPPmin} = 0.26\,\mathrm{A}$, respectively.
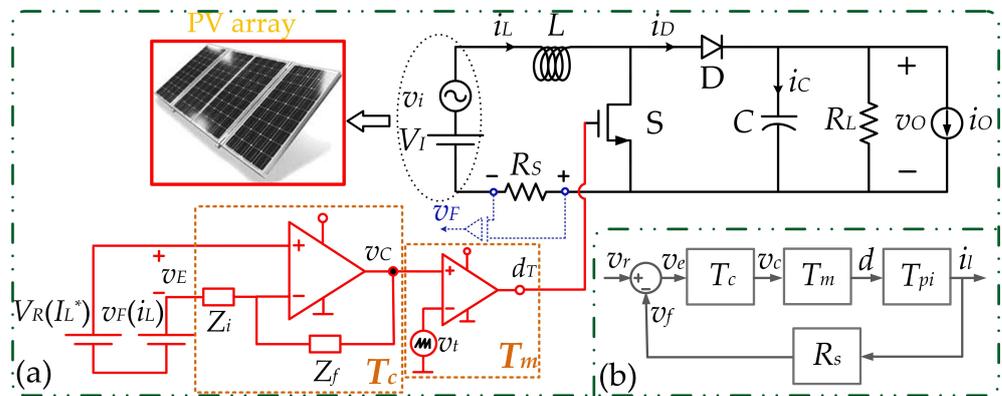
Figure 2. The PV-connected DC–DC boost converter: (**a**) power and control circuits and (**b**) small-signal block diagram representation assuming that $i_O = v_i = 0$.

Table 1. Specifications of the BP Solar BP4170B module.

Parameter	Unit	Value
Maximum power at maximum irradiation, P_{max}	W	170.88
Open-circuit voltage, U_{oc}	V	43.6
Short-circuit current, I_{sc}	A	5.2
MPP voltage at maximum irradiation	V	35.6
MPP current at maximum irradiation, I_{MPP}	A	4.8
Equivalent series resistance, R_s	Ω	0.533
Thermal coefficient of short-circuit current, k_{temp}	(%/deg.C)	0.11
Equivalent parallel resistance, R_p	Ω	251.26
Diode reverse recovery current, $i_{rs,STC}$	A	-2.3958×10^{-10}
Number of series-connected cells, N_{cell}	-	72
Diode ideality factor, A	-	0.99161

Table 2. Operating points of the 1 kW PV array designed for grid integration.

V_{MPPmax}	I_{MPPmax}	V_{MPPmin}	I_{MPPmin}	$\Delta v_O / V_O$
213.6 V	4.8 A	195.4 V	0.26 A	1 %
V_{gmax}	V_{gmin}	V_O	f_{sw}	
242 V	198 V	350 V	50 kHz	

The input data for designing the energy storage elements were the input voltage, V_I, minimum input current, I_{MPPmin}, output voltage, V_O, permissible output voltage ripple, $\Delta v_O / V_O$, and switching frequency, f_{sw}. The first two data were obtained according to the above-mentioned MPP characteristics. The maximum and minimum PV output voltages, V_{Imin} and V_{Imax}, were equal to V_{MPPmax} and V_{MPPmin}. The PV converter had to inject the power into the grid for the minimum irradiation [4]. Thus, the minimum PV current at the lowest irradiation was $I_{MPPmin} = 0.26\,\mathrm{A}$. It was assumed that the rms value of the single-phase grid voltage, V_g, changed in the range of $(220 \pm 10\%)$; then, $198 < V_g < 242\,\mathrm{V}$. In the control of a grid-connected inverter, the modulation index, M, was set to near unity to minimize the harmonic content of the inverter output voltage and current [19]. With these explanations and with $M = 1$, the maximum DC-link voltage was calculated as equal

to $V_O = \sqrt{2} \cdot 242 = 342$ V. Hence, V_O was set equal to 350 V. The allowable ripples on the DC–DC output voltage were considered as 1%. Finally, the converter switching frequency was 50 kHz.

Thus, all of the information required to design the energy storage elements is ready. The minimum inductance for meeting the continuous current mode (CCM) for the minimum irradiation level was calculated as equal to 3.3 mH. The output capacitance for meeting the maximum 1% of output voltage oscillations was obtained as equal to 16.8 µF (the complete design process based on the input data is explained in [20] and is not repeated here for the sake of brevity). Then, the power decoupling capacitance had to be selected based on (12). For this purpose, based on Table 1, the maximum allowed ripple at the output of six series-connected PV modules was equal to 25.65 V, considering $k_{PV} = 0.98$. Hence, based on (12), the minimum required power decoupling capacitance was calculated as nearly equal to 300 µF. Obviously, a 220 V, 300 µF capacitor is available as an electrolytic one, which, as explained earlier, reduces the reliability and lifetime of the PV structure. In the following part of this paper, a novel method for controlling the DC–DC boost converter is proposed with a remarkable reduction of the size of the power decoupling capacitor. Thus, the application of film capacitors is possible.

4. Transfer Functions and Current Mode Control in a PV-Connected DC–DC Boost Converter

Two general control methods are proposed in the literature for DC–DC boost converters [4,20]: voltage mode control (VMC) and current control mode (CMC). In VMC, also known as duty-cycle control, the purpose is to control the output voltage, v_O, and it consists of a single loop that directly adjusts the duty cycle to respond to variations in the output voltage. On the other hand, CMC consists of two loops: one internal current control loop and one external voltage control loop [21]. The first one controls either the inductor peak (PCMC) or the average current (ACMC). A converter with CMC exhibits a proper dynamic response to input and output disturbances [14].

In this paper, ACMC is utilized to control the output current of the PV array. Contrary to previous works, a single current control loop is adopted. Therefore, it is necessary to design the control structure according to the duty-cycle-to-inductor current transfer function, i.e., i_L/d. An integral single-lead controller (ISLC) and a PI controller are utilized to compensate for the error between the reference and feedback currents of the inductor. In addition, it is shown that the i_L/d transfer function exhibits a low amplitude at the SOFC and, therefore, reduces the amplitude of pulsations across the PV array. This is particularly beneficial in terms of using lower power decoupling capacitance.

4.1. Transfer Function of the DC–DC Boost Converter

The aim is to control the inductor's average current through the control circuit, as shown in Figure 2a. An analog implementation of the control structure is presented due to its availability on integrated circuits (ICs), such as the TL494. This IC integrates all of the functions required by a PWM circuit with various applications, such as those in personal computers, switching-mode power supplies, PV AC modules, etc. [22]. It is worth mentioning that the digital implementation of the control structure is also possible according to the presented transfer functions. According to Figure 2a, a measuring resistance, R_s, was used to apply the circuit's current to the controller. The switch's duty cycle, d, was generated through a comparison between the control voltage, v_C, and the reference in the modulator with the transfer function of T_m. By applying this duty cycle to the switch, the inductor current, i_L, was set to the reference value, i_L^*. In [20], the linearized small-signal model of a DC–DC boost converter was presented by considering the effect of parasitic resistances of passive elements, diodes, and transistors. Through this model, the input-to-output transfer function in the Laplace domain was extracted with the following final equation [20]:

$$T_{pi}(s) = \left.\frac{i_l(s)}{d(s)}\right|_{v_i=i_O=0} = T_{pi0}\frac{1 + s/\omega_{z_{i1}}}{1 + s/Q\omega_0 + (s/\omega_0)^2}, \tag{13}$$

in which s is the Laplace operator and i_l and d are small-signal variations in the inductor current and duty cycle, respectively. The amplitude of T_{pi} at zero frequency is equal to

$$T_{pi0} = T_{pi}(0) = \frac{2V_O}{(1-D)^2 R_L + r}. \tag{14}$$

In this equation, $r = D_{nom}r_{DS} + (1 - D_{nom})R_F + r_L$, with $D_{nom}, r_{DS}, R_F, r_L$ being the nominal duty cycle, switch drain–source resistance, diode conducting resistance, and inductor resistance, respectively. In addition, the angular undamped natural frequency, ω_0, and the damping ratio, ξ, are equal to

$$\omega_0 = \sqrt{\frac{(1-D)^2 R_L + r}{LC(R_L + r_C)}}; \quad \xi = \frac{C\left[r(R_L + r_C) + (1-D)^2 R_L r_C\right] + L}{2\sqrt{LC(R_L + r_C)\left[r + (1-D)^2 R_L\right]}}. \tag{15}$$

The quality factor is equal to $Q = 1/(2\xi)$. The transfer function T_{pi} is generally a second-order low-pass filter with one zero, z_{i1}, at the left-hand plane (LHP) and two poles, p_1 and p_2, at the LHP:

$$z_{i1} = -\omega_{z_{i1}} = -\frac{1}{C(R_L/2 + r_C)}; \quad p_1, p_2 = -\xi\omega_0 \pm j\omega_0\sqrt{1 - \xi^2}. \tag{16}$$

With the parameters listed in Table 3, the values of r, z_{i1}, $f_{z_{i1}}$, f_0, ξ, $p1$, $p2$, and f_d were calculated and are listed in Table 4 for the designed DC–DC boost converter connected to the mentioned PV array. It should be mentioned that V_{Inom} and D_{nom} were set equal to the average values of the PV output voltage and duty cycle, respectively.

Table 3. Parameters of the designed DC–DC boost converter for controlling the PV array's output.

V_{Inom}	D_{nom}	r_{DS}	R_F	L	r_L	C	r_C	V_O	R_{Lmin}
204 V	0.4754	0.5 Ω	0.025 Ω	3.3 mH	0.5 Ω	17 μF	0.04 Ω	350 V	120 Ω

Table 4. Parameters of T_{pi} of the DC–DC boost converter.

r	z_{i1}	$f_{z_{i1}}$	f_0	ξ	p_1, p_2	f_d
0.751 Ω	−987 rad/s	157 Hz	358 Hz	0.16	−362 ± j2221 rad/s	353 Hz

4.2. Transfer Function of the Average Current Mode Controller

The loop gain of the block diagram shown in Figure 2b is equal to $T_{ol} = R_s T_C T_m T_{pi}$, with T_m and T_C being the pulse-width modulator and controller transfer functions, respectively. The pulse-width modulator is a sawtooth waveform changing linearly between 0 and V_{Tm} in a switching period of T_s. In other words, the slope of this change is equal to $S = V_{Tm}/T_s = V_{Tm}f_s$. The control-voltage-to-duty-cycle transfer function in the small-signal domain, $T_m(ac)$, is as follows:

$$T_m(ac) = \frac{d}{v_c} = \frac{1}{V_{Tm}} = \frac{1}{ST_s} = \frac{f_s}{S}. \tag{17}$$

On the other hand, two controllers with a transfer function of $T_C(s) = Z_f(s)/Z_i(s)$ [20] were considered for the implementation. One was an integral single-lead controller (ISLC), and the other was a PI controller, as described in the following.

4.3. Integral Single-Lead Controller (ISLC)

The circuit diagram of an ISLC is shown in Figure 3. This controller has a pole at the origin and a zero–pole pair. The pole at the origin makes the integral part and the zero–pole pair makes the lead part of the controller. The transfer function of the ISLC is obtained as in [20].

$$T_C(s) = \frac{Z_f(s)}{Z_i(s)} = \frac{B(1 + s/\omega_{zc})}{K^2 s(1 + s/\omega_{pc})},$$ (18)

Here,

$$B = \frac{1}{C_2 R_1}; \ \omega_{zc} = \frac{1}{R_2 C_1}; \ \omega_{pc} = K^2 \omega_{zc}; \ K = \sqrt{\frac{\omega_{pc}}{\omega_{zc}}} = \sqrt{\frac{C_1}{C_2} + 1}.$$ (19)

Replacing $s = j\omega$ in (18), the frequency response of the ISLC is obtained as $T_C(j\omega) = |T_C| e^{j\phi_{T_C}}$.

$$|T_C| = \frac{B}{\omega K^2} \sqrt{\frac{1 + (\omega/\omega_{zc})^2}{1 + (\omega/\omega_{pc})^2}}; \ \phi_{T_C} = -\frac{\pi}{2} + \arctan\left(\frac{\omega/\omega_{zc} - \omega/\omega_{pc}}{1 + \omega^2/(\omega_{pc}\omega_{zc})}\right).$$ (20)

By taking the derivatives of the expression within the parentheses in the equation of ϕ_{T_C} and setting them to zero, the frequency at which the phase-shift of ϕ_{T_C} is at its maximum is acquired as

$$\omega_m = \sqrt{\omega_{zc}\omega_{pc}} = \frac{\omega_{pc}}{K} = K\omega_{zc} = \frac{K}{R_2 C_1}.$$ (21)

Substituting (21) into (20) yields,

$$\phi_{T_C}(f_m) = -\frac{\pi}{2} + \arctan\left(\frac{K^2 - 1}{2K}\right) = -\frac{\pi}{2} + \arcsin\left(\frac{K^2 - 1}{K^2 + 1}\right).$$ (22)

The ideal (approximate) Bode plots for T_C are shown in Figure 3b. According to this figure and (22), the maximum phase shift, which is also known as the phase boost (shown in Figure 3b by ϕ_m), is

$$\phi_m = \phi_{T_C}(f_m) - \left(-\frac{\pi}{2}\right) = \arcsin\left(\frac{K^2 - 1}{K^2 + 1}\right); \ K = \tan\left(\frac{\phi_m}{2} + 45°\right).$$ (23)

(a)   (b)   (c)
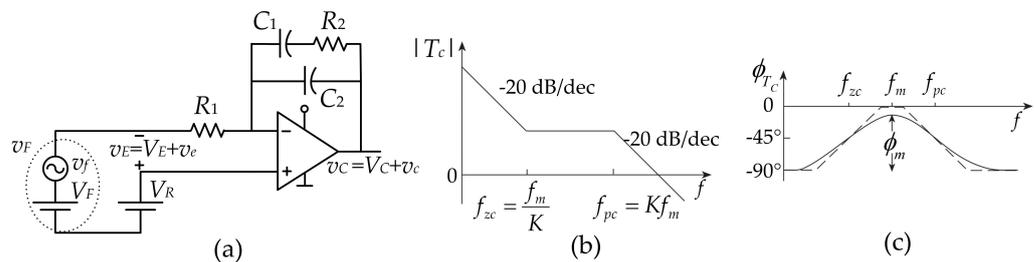
Figure 3. ISLC, (**a**) analog implementation, (**b**) amplitude, and (**c**) phase of ideal Bode plots [20].

4.4. Proportional–Integral (PI) Controller

The reason for introducing this controller along with the ISLC is its simple implementation, for example, on the TL494. The analog implementation of the proposed PI controller is shown in Figure 4a. The current i_{Z_i} in Figure 4a is calculated with the following equation:

$$i_{Z_i} = \frac{V_R - v_F}{Z_i} = \frac{v_F - v_C}{Z_f}.$$ (24)
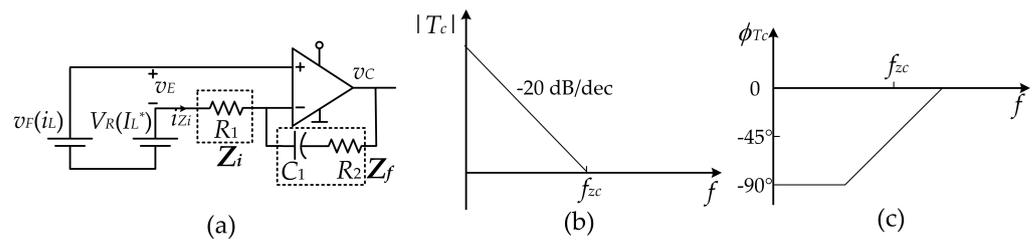
Figure 4. Proposed PI controller:(**a**) analog implementation, (**b**) amplitude, and (**c**) phase of the ideal Bode plots.

By rearranging the above equation based on the control voltage, v_C,

$$v_C = V_C + v_c = v_F + \frac{Z_f}{Z_i}(V_F + v_F - V_R). \tag{25}$$

According to the above equation, the small-signal control voltage, i.e., v_c, is calculated as follows:

$$v_c = \frac{Z_f + Z_i}{Z_i} v_f. \tag{26}$$

On the other hand, based on Figure 4a,

$$v_E = v_F - V_R. \tag{27}$$

According to the relation of $v_e = v_f$, which are the small-signal portions of the error and feedback signals, respectively, (26) turns into

$$T_C = \frac{v_c}{v_e} = \frac{Z_f + Z_i}{Z_i}. \tag{28}$$

Based on Figure 4a, by putting $Z_i = R_1$ and $Z_f = 1/C_1 s + R_2$ into (28), the following transfer function is obtained:

$$T_C(s) = \frac{(R_1 + R_2)}{R_1}\frac{(s + \omega_{zc})}{s}; \; \omega_{zc} = \frac{1}{C_1(R_1 + R_2)}. \tag{29}$$

By replacing $s = j\omega$ in the above equation, the transfer function in the frequency domain is obtained:

$$T_C(j\omega) = \frac{(R_1 + R_2)}{R_1}\frac{(j\omega + \omega_{zc})}{j\omega} = K\frac{(j\omega + \omega_{zc})}{j\omega}, \tag{30}$$

with the amplitude and phase of

$$|T_C(j\omega)| = \frac{(R_1 + R_2)}{R_1}\frac{\sqrt{\omega^2 + \omega_{zc}^2}}{\omega}; \; \phi_{T_C}(j\omega) = -\frac{\pi}{2} + \arctan\left(\frac{\omega}{\omega_{zc}}\right). \tag{31}$$

The ideal Bode plots of the PI controller are shown in Figure 4b,c. According to this figure, the maximum decrease in the phase (phase boost of the controller) is

$$\phi_m = \arctan\left(\frac{\omega}{\omega_{zc}}\right). \tag{32}$$

4.5. Designing the ISLC

In this section, the ISLC is designed so that the phase margin of the open-loop transfer function, T_{ol}, is equal to 60 degrees. The parameters mentioned in Tables 1–4 are considered for the connection of the DC–DC converter to the PV array. For the starting point and according to the design recommendations made in [23], the gain crossover frequency

(GCF) was selected as equal to one-sixth of the switching frequency. Then, according to (13) and (17), the phase angle of the open-loop transfer function was calculated at the GCF while excluding the effect of the compensating transfer function (controller), i.e., $T_k(f_c)$ with $T_k = R_s T_m T_{pi}$. Thus, the required phase boost to have the necessary phase margin (*PM*) was

$$\phi_{T_k}(f_c = f_m) + \phi_{T_C}(f_c = f_m) = -180° + PM. \tag{33}$$

This phase boost should be provided by the controller. Using (22) and (33),

$$\phi_m = PM - \phi_{T_k}(f_m) - 90°. \tag{34}$$

Then, *K* can be defined according to (23), and, consequently, the angular frequencies of the controller pole and zero, p_c and z_c, are obtained based on (19). On the other hand, the amplitude of the open-loop transfer function at GCF is unity, which means that

$$|T_C(f_c)| = \frac{1}{|T_k(f_c)|}. \tag{35}$$

Hence, *B* is defined as

$$B = \omega_c K |T_C(f_c)|. \tag{36}$$

The above process was applied for the design of the ISLC with the parameters in Tables 3 and 4. The designed parameters are shown in Table 5. The Bode plots of the controller and open-loop transfer function are shown in Figure 5a,b, respectively. A phase margin of 60 degrees was observed at the GCF, as shown in Figure 5b. However, with a GCF equal to 8.3 kHz, the phase margin was remarkably reduced at around 600 Hz. Hence, the disturbances at these frequencies could drive the controller into instability. Table 6 lists the controller's parameters for a GCF equal to 2 kHz. The Bode plot was redrawn for this crossover frequency, as shown in Figure 6, where the required phase margin was observed in the intended frequency range. However, the decrease in the GCF increased the penetration of the SOFC into the input, and a trade-off had to be made for the selection of the GCF. This issue will be discussed in the next section.

Table 5. Parameters of the ISLC with a GCF equal to 8.3 kHz.

V_{T_m}	R_s	$\phi_{T_k}(f_c)$	$|T_k(f_c)|$	ϕ_m	K	f_{pc}	f_{zc}
5 V	0.1 Ω	$-90.28°$	-27.81 dB	$60.28°$	3.77	31.41 kHz	2.21 kHz

Table 6. Parameters of the ISLC with GCF = 2 kHz.

V_{T_m}	R_s	$\phi_{T_k}(f_c)$	$|T_k(f_c)|$	ϕ_m	K	f_{pc}	f_{zc}
5 V	0.1 Ω	$-91°$	-15.14 dB	$61.08°$	3.88	7.76 kHz	515.74 Hz
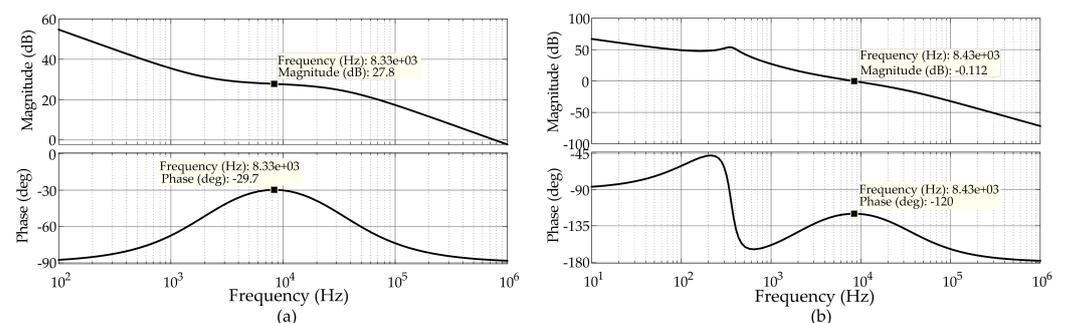
Figure 5. Bode plots for the (**a**) ISLC, T_C, and (**b**) open-loop transfer function, T_{ol}, with GCF = 8.33 kHz.
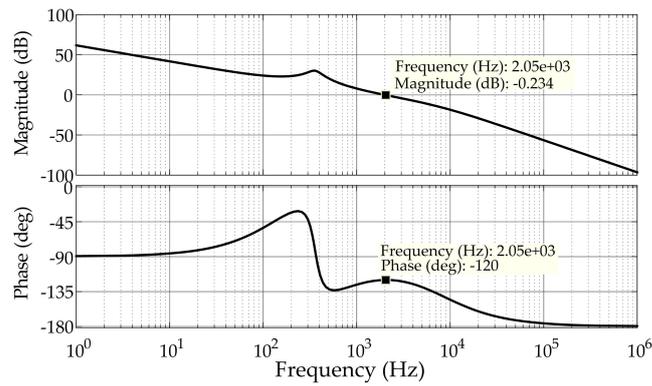
Figure 6. Bode plots for the open-loop transfer function with the ISLC with GCF = 2 kHz.

4.6. Designing the PI Controller

Similarly, the GCF was set to 2 kHz for the PI controller. A block diagram representation of the ACMC in a boost converter with a PI controller is shown in Figure 7, in which the closed-loop transfer function for this controller, i_l/v_r, is obtained as

$$\frac{i_l}{v_r} = \frac{T_C T_{pi}}{V_{Tm} + R_s T_C T_{pi}}. \tag{37}$$

By defining the phase angle at the GCF according to (13) and considering a phase margin of 60 degrees, the required phase boost of ϕ_m was calculated based on (34). Then, the angular frequency of the PI controller zero was obtained based on (32). Furthermore, K in (18) was recognized, as it was known that the amplitude of the controller's transfer function should be the inverse of the amplitude of T_k at the GCF:

$$K = \frac{\omega_c \sqrt{\omega_c^2 + \omega_{zc}^2}}{|T_k|}. \tag{38}$$

Table 7 lists the PI controller parameters for the designed boost controller with a GCF equal to 2 kHz. In addition, the Bode plots of the controller and open-loop transfer functions are drawn in Figure 8a,b, respectively. According to Figure 8b, a phase margin of 60 degrees was observed at GCF = 2 kHz. However, the phase margin was reduced to 30 degrees at the frequency of 500 Hz, which could influence the converter's stability under low-frequency disturbances.
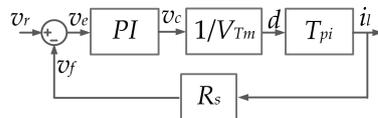
Figure 7. Block diagram representation of the ACMC's closed-loop control with a PI controller.
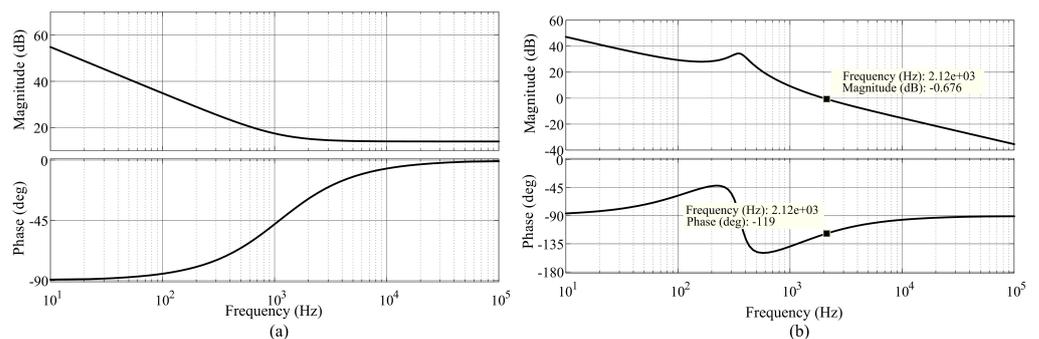
Figure 8. Bode plots for the (**a**) PI controller, T_C, and (**b**) open-loop transfer function, T_{ol}, with GCF = 2 kHz.

Table 7. Parameters of the PI controller with GCF = 2 kHz.

V_{Tm}	R_s	$\phi_{T_k}(f_c)$	$|T_k(f_c)|$	ϕ_m	K	f_{zc}
5 V	0.1 Ω	$-271°$	-15.14 dB	241°	5	1105 Hz

5. Design of a Power Decoupling Capacitor Based on the Allowable Utilization Factor

The effects of the studied controllers on the penetration of the SOFC into the input are investigated in this section. For this purpose, first, the open-loop transfer function from the output disturbance current, i_O, to the inductor's small-signal current, i_l ($A_i = i_l/i_o$, as shown in Figure 2a), was obtained according to the block diagram shown in Figure 9, where the factors contributing to the small-signal variations in the inductor current were i_o, v_i, and d. In [20], a procedure for finding $A_i(s)$ was presented based on a small-signal model of the circuit, and the final equation is mentioned here for the sake of brevity:

$$A_i(s) = \frac{i_l}{i_o}\bigg|_{v_i=d=0} = A_{ix}\frac{s+\omega_{zn}}{s^2+2\xi\omega_0 s+\omega_0^2}; \; A_{ix} = \frac{(1-D)R_L r_C}{L(R_L+r_C)}. \tag{39}$$

Then, the closed-loop transfer function was obtained based on Figure 9. Setting $i_{l,ref}$ and v_i equal to zero, the transfer function was obtained as

$$A_{i,cl}(s) = \frac{A_i(s)}{1+R_s T_C(s) T_m(s) T_{pi}(s)}. \tag{40}$$
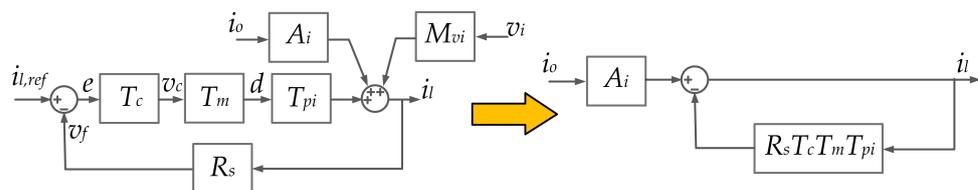
Figure 9. Small-signal model of the boost converter in the ACMC of the inductor current.

Replacing (18) in (40), for the ISLC, $A_{i,cl}$ is

$$A_{i,cl} = \frac{A_{ix}\left(s^3+(\omega_{zn}+\omega_{pc})s^2+\omega_{zn}\omega_{pc}s\right)}{s^4+(\omega_{pc}+2\xi\omega_0)s^3+(\omega_0^2+2\xi\omega_0\omega_{pc}+G_{cl})s^2+(\omega_0^2\omega_{pc}+(\omega_{zi1}+\omega_{zc})G_{cl})s}, \tag{41}$$

where,

$$G_{cl} = \frac{B\omega_{pc}R_s T_{pi0}\omega_0^2}{K^2\omega_{zc}V_{Tm}\omega_{zi1}}. \tag{42}$$

On the other hand, replacing (37) in (41), for the PI controller, $A_{i,cl}$ is

$$A_{i,cl} = \frac{A_{ix}\left(s^2+\omega_{zn}s\right)}{s^3+(G_{cl}+2\xi\omega_0)s^2+(\omega_0^2+(\omega_{zi1}+\omega_{zc})G_{cl})s+\omega_{zi1}\omega_{zc}G_{cl}}, \tag{43}$$

where

$$G_{cl} = \frac{KR_s T_{pi0}\omega_0^2}{V_{Tm}\omega_{zi1}}. \tag{44}$$

Consequently, the SOFC for the two introduced controllers at the input of the boost converter is $i_{l,2} = i_{O,2} \times A_{i,cl}(s=j2\omega)$. The voltage ripple due to this current ripple is calculated based on (10). The Bode plots of (41) and (43) are shown in Figure 10 under the same gain crossover frequency. Figure 10 reveals that the PI controller has better SOFC rejection capabilities compared to those of the ISLC at the cost of a lower phase margin under low-frequency disturbances. The amplitude of the SFOC in the input inductor

current is 6.76% of that in the output current for the PI controller, while it is 12.16% for the ISLC.
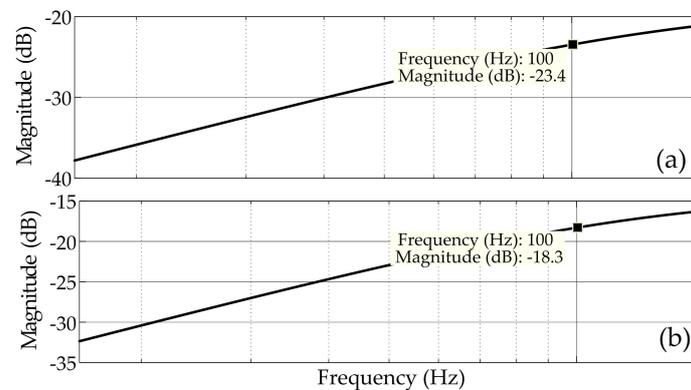
Figure 10. Bode plots of $A_{i,cl}$ for $D = 0.47$, $V_I = 204\,\text{V}$, $f_c = 2\,\text{kHz}$, $V_O = 350\,\text{V}$: (**a**) PI controller; (**b**) ISLC.

In summary, the design procedure is as follows. First, (6) is used to calculate the allowable voltage ripple of the PV array based on the minimum allowable utilization factor, $k_{PV} = 0.98$. Second, considering a capacitance that could be implemented by the film capacitors, $i_{l,2}$ is obtained based on (8). Third, the value of $i_{O,2}$, which is the SOFC of the DC-link current, is computed while assuming the equal input and output powers of the inverter:

$$i_O = \frac{V_m I_m \sin(\omega t) \sin(\omega t - \phi)}{V_{DC}} \Rightarrow i_{O,2} = \frac{-V_m I_m}{2V_{dc}} \cos(2\omega t), \tag{45}$$

with V_{DC} being the DC-link voltage. Finally, the GCF is computed so that $\left|A_{i,cl}(s = j2\omega)\right| = \left|i_{O,2}\right| \times \left|i_{l,2}\right|$.

For the designed PV system, the maximum allowable voltage is calculated as equal to 25.65 V in order to have $k_{PV} = 0.98$. Therefore, the current ripple of a 40 μF film power decoupling capacitor is equal to 0.645 A. On the other hand, the maximum current ripple at the output of the boost converter, $i_{O,2}$, is 6.43 A for the power of 1 kW and $V_m = 311$ V. In other words, the amplitude of i_l/i_O at an SOFC of 100 Hz must be equal to $0.645/6.43 = 0.1 = -19.97\,\text{dB}$. With the procedure explained for the PI controller, a gain crossover frequency of 2 kHz is adequate to observe the permissible voltage ripple with a 40 μF capacitor.

The complex of the PV array and the DC–DC boost converter were implemented in MATLAB/SIMULINK with the designed circuit elements to verify the efficacy of the proposed design procedure. For the simulation studies, the voltage and current of the PV array were controlled at its MPP for different irradiation levels with the incremental conductance (IC) method. The temperature of the PV panels was considered to be equal to 25 °C in the simulations. In addition, a fixed voltage source equal to 350 V was placed at the output to replace the single-phase grid-connected inverter. Figure 11 shows the simulation results of the inductor current for three irradiation levels of 50, 500, and 800 W/m². According to this figure, the inductor current could perfectly follow the reference value (that is, the output of the IC algorithm), which is indicative of the proper design of controllers (the results for the PI controller and ISLC were the same).

In the next step, a current source was connected in parallel with the output of the DC–DC boost converter to represent the SFOC disturbance. Figure 12 shows a Fourier analysis of the inductor current with the ISLC and PI controller. The amplitude of the SFOC in the inductor current was lower for the PI controller. Furthermore, with the designed GCF, the amplitude of the input SOFC was, at most, 7% in the case of the ISLC and the maximum irradiation level. This was below the 10% considered for the amplitude of $A_{i,cl}$,

which created the maximum permissible voltage ripple of 25.65 V in the presence of a 40 μF power decoupling capacitance.

The propagation of the SOFC could be decreased further by selecting a higher GCF. Figure 13 shows the simulation results of the inductor current for GCF = 8.33 kHz. This figure indicates the drastic shrink in the input SOFC compared to the case when the GCF was equal to 2 kHz (0.2% versus 3.74% for the PI controller). However, attention should be paid to the reduced phase margin under low-frequency disturbances.
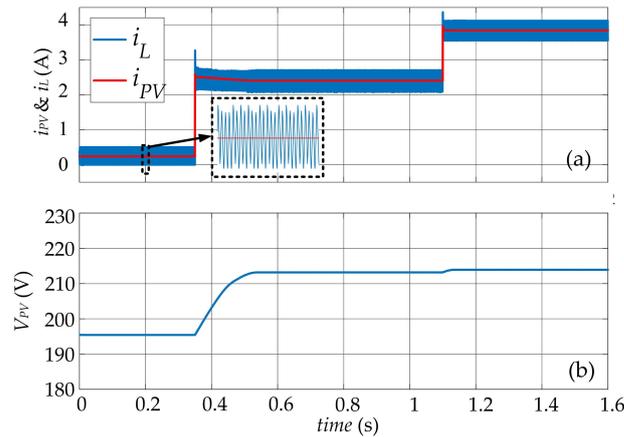
Figure 11. MPPT control of the PV array: (**a**) inductor current and (**b**) the PV array's output voltage.
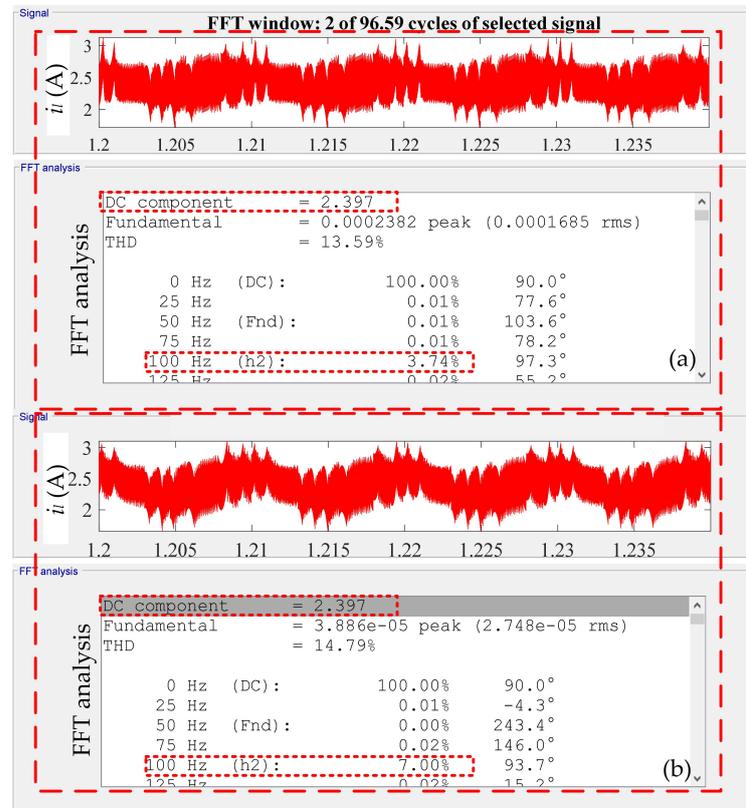
Figure 12. Inductor current when the harmonic source is placed at the output and GCF = 2 kHz: (**a**) PI controller and (**b**) ISLC.
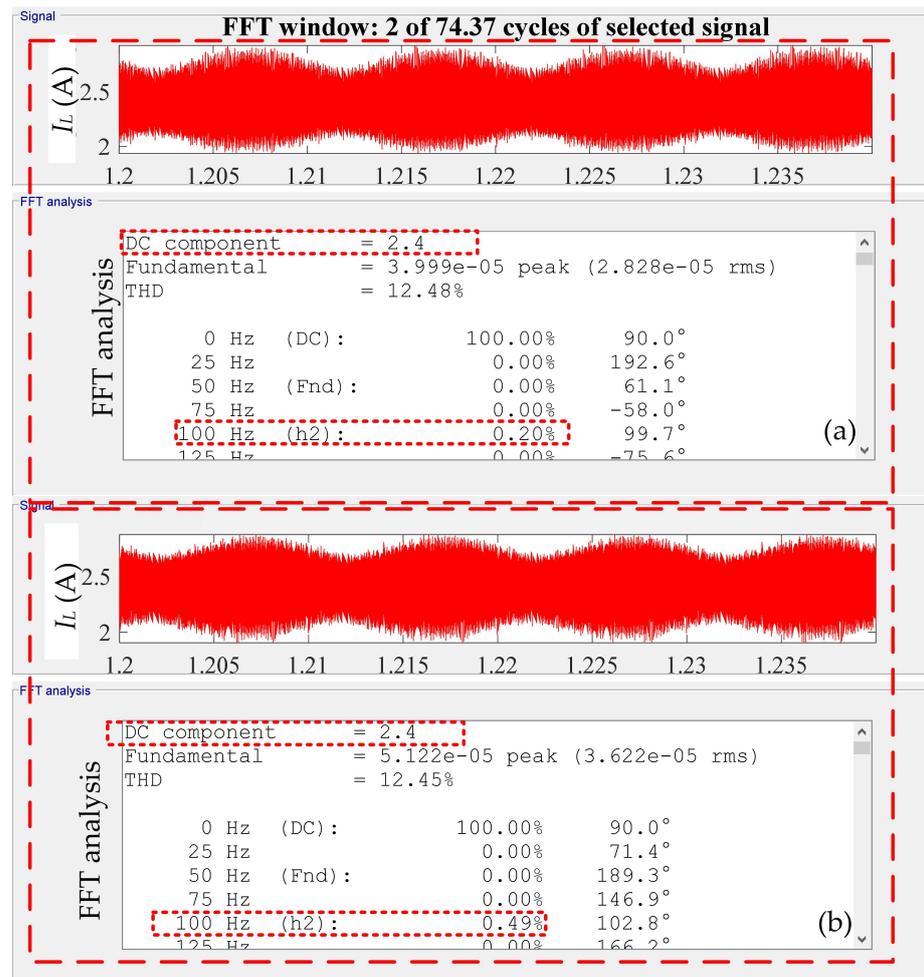
Figure 13. Inductor current when the harmonic source is placed at the output and GCF = 8.33 kHz: (**a**) PI controller and (**b**) ISLC.

6. Conclusions

The propagation of second-order frequency components (SFOCs) into an input PV array aggravates the energy harvesting efficiency in single-phase grid-connected inverters. Auxiliary circuits are added or modifications in the control loops are made to avoid the use of bulky electrolytic capacitors. This paper proposes the use of average current mode control (ACMC) to impose a high impedance toward SOFCs. The transfer function from the output oscillatory current to the input inductor current, $A_{i,cl}$, is extracted when two types of controllers are utilized, i.e., an integral single-lead controller (ISLC) and a proportional–integral (PI) controller. These controllers must be designed for the specific case of PV-grid-connected inverters, since the transfer function depends on the gain crossover frequency (GCF), zeros, and poles of controllers and their gains, which all depend on the switch's duty cycle and, consequently, the operating point of the PV array. It is shown in this paper that the GCF greatly affects the amplitude of $A_{i,cl}$. Higher GCFs are advantageous in terms of a drastic reduction in the input current and voltage ripples, but at the cost of a phase margin reduction in the low-frequency range. This paper introduced a design procedure based on the allowable utilization factor of a PV array (maximum allowable voltage ripple at the output of the PV array). Then, the GCF was selected based on the amplitude of $A_{i,cl}$ and the available film capacitor. This showed that the required power decoupling capacitance was significantly reduced (40 µF compared to 300 µF) by applying the presented design procedure.

Abbreviations

The following abbreviations are used in this manuscript:

ALFRC	Active low-frequency ripple control
ACMC	Average current mode control
CMC	Current mode control
GCF	Gain crossover frequency
IC	Incremental conductance
ISLC	Integral single-lead controller
PV	Photovoltaic
PI	Proportional–integral
SOFC	Second-order frequency component
VMC	Voltage mode control

References

1. Kjaer, S.B.; Pedersen, J.K.; Blaabjerg, F. A review of single-phase grid-connected inverters for photovoltaic modules. *IEEE Trans. Ind. Appl.* **2005**, *41*, 1292–1306. [CrossRef]
2. Liu, C.; Lai, J. Low frequency current ripple reduction technique with active control in a fuel cell power system with inverter load. *IEEE Trans. Power Electron.* **2007**, *22*, 1429–1436. [CrossRef]
3. Hu, H.; Harb, S.; Kutkut, N.; Batarseh, I.; Shen, Z.J. A review of power decoupling techniques for microinverters with three different decoupling capacitor locations in PV systems. *IEEE Trans. Power Electron.* **2013**, *28*, 2711–2726. [CrossRef]
4. Kjaer, S.B. Design and Control of an Inverter for Photovoltaic Applications. Ph.D. Dissertation, Aalborg University, Aalborg East, Denmark, 2005.
5. Harb, S.; Mirjafari, M.; Balog, R.S. Ripple-port module-integrated inverter for grid-connected PV applications. *IEEE Trans. Ind. Appl.* **2013**, *49*, 2692–2698. [CrossRef]
6. Liao, C.-Y.; Lin, W.-S.; Chen, Y.-M.; Chou, C.-Y. A PV micro-inverter with PV current decoupling strategy. *IEEE Trans. Power Electron.* **2017**, *32*, 6544–6557. [CrossRef]
7. Zare, M.H.; Mohamadian, M.; Beiranvand, R. Single-stage AC module with series power decoupling capability for connecting PV to a single-phase power grid. *IET Power Electron.* **2017**, *10*, 517–524. [CrossRef]
8. Zeng, J.; Zhuo, M.; Cheng, H.; Kim, T.; Winstead, V.; Wu, A.L. Power pulsation decoupling for a two-stage single-phase photovoltaic inverter with film capacitor. In Proceedings of the 2017 IEEE Energy Conversion Congress and Exposition (ECCE), Cincinnati, OH, USA, 1–5 October 2017; pp. 468–474.
9. Ahmad, A.A.; Abrishamifar, A.; Samadi, S. Low-frequency current ripple reduction in front-end boost converter with single-phase inverter load. *IET Power Electron.* **2012**, *5*, 1676–1683. [CrossRef]
10. Gautam, A.R.; Gourav, K.; Guerrero, J.M.; Fulwani, D. Ripple mitigation with improved line-load transients response in a two-stage DC-DC-AC converter adaptive SMC approach. *IEEE Trans. Ind. Electron.* **2018**, *65*, 3125–3135. [CrossRef]
11. Ohnuma, Y.; Orikawa, K.; Itoh, J.-I. A single-phase current source PV inverter with power decoupling capability using an active buffer. *IEEE Trans. Ind. Appl.* **2015**, *51*, 531–538. [CrossRef]
12. Wai, R.-J.; Lin, C.-Y. Active low-frequency ripple control for clean-energy power-conditioning mechanism. *IEEE Trans. Ind. Electron.* **2010**, *57*, 3780–3792. [CrossRef]
13. Cai, W.; Liu, B.; Duan, S.; Jiang, L. An active low-frequency ripple control method based on the virtual capacitor concept for BIPV systems. *IEEE Trans. Power Electron.* **2014**, *29*, 1733–1745. [CrossRef]
14. He, D.; Nelms, R.M. Average current-mode control for a boost converter using an 8-bit microcontroller. In Proceedings of the 2004 IEEE International Symposium on Industrial Electronics, Ajaccio, France, 4–7 May 2004; pp. 1185–1190.
15. Rajagopalan, J.; Lee, F.C.; Nora, P. A general technique for derivation of average current mode control laws for single-phase power-factor-correction circuits without input voltage sensing. *IEEE Trans. Power Electron.* **1999**, *14*, 663–672. [CrossRef]
16. Lu, Z.; Wang, M.; Zheng, L. A predictive averaged current mode control for high power factor boost rectifier. In Proceedings of the International Conference on Electrical Machines and Systems, Nanjing, China, 27–29 September 2005; pp. 1228–1231.

17. Jayahar, D.; Ranihemamalini, R. Inductor average current mode control for single phase power factor correction buck-boost converter. In Proceedings of the International Conference on Emerging Trends in Electrical and Computer Technology, Nagercoil, India, 23–24 March 2011; pp. 274–279.

18. Mohamadian, S.; Pairo, H.; Ghasemian, A. A straightforward quadrature signal generator for single-phase SOGI-PLL with low susceptibility to grid harmonics. *IEEE Trans. Ind. Electron.* **2021**, *69*, 6997–7007. [CrossRef]

19. Mohamadian, S.; Pazoki, M.; Hamidi, R.J. LCL filter design for single-phase grid-connected PV inverters with double-frequency unipolar PWM switching. In Proceedings of the IEEE Power & Energy Society General Meeting (*PESGM*), Washington, DC, USA, 26–29 July 2021; pp. 1–5.

20. Kazimierczuk, M.K. *Pulse-Width Modulated DC-DC Power Converters*, 2nd ed.; John Wiley & Sons: Chichester, UK, 2016.

21. Qiu, Y.; Liu, H.; Chen, X. Digital average current-mode control of PWM DC–DC converters without current sensors. *IEEE Trans. Ind. Electron.* **2010**, *57*, 1670–1677.

22. TL494 Pulse-Width-Modulation Control Circuits, Application Note. Available online: https://www.ti.com/product/TL494 (accessed on 20 November 2022).

23. Dixon, L.H. Average current mode control of switching power supplies. In *Unitrode Power Supply Design Seminar Handbook*; Unitrode Corporation: Merrimack, NH, USA, 1990; pp. 5.1–5.14.