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An FPGA Hardware-in-the-Loop Approach for Comprehensive Analysis and Development of Grid-Connected VSI System

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Abstract: Power electronic converters are used for an efficient and controlled conversion of power generated from renewable energy sources and can interface generated power to the grid. Among available power converters, voltage source inverters (VSIs) have been widely employed for grid-connected applications due to better controllability with higher efficiency. Although various conventional, as well as modern control techniques, have been developed for grid connected VSI system, there is a need to select suitable control technique based on application and control requirements. Hardware-in-the-loop (HIL) is considered as a realistic approach for the development of system and control due to the inclusion of an actual hardware system. In this paper, a HIL approach is adopted for the comprehensive analysis and development of a grid connected VSI system using a field programmable gate array (FPGA). The control techniques must deal with trade-off, based on the features and limitations. Therefore, a grid-connected VSI system is developed considering employment of two different conventional control techniques: hysteresis current control (HCC) and PI-based space vector modulation (PI-SVM), as well as finite state model predictive control (FS-MPC) as a modern control technique for investigation considering different parameters. All three control systems are developed through a digital simulator of Xilinx that is integrated with MATLAB-Simulink, while considering an FPGA based system development and testing through FPGA HIL co-simulation methodology.

Keywords: field-programmable gate array; finite state model predictive control; grid-connected system; hardware-in-the-loop; hysteresis current control; space vector modulation; voltage source inverter



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1. Introduction

In recent years, energy demand has been growing at a rapid rate, because of population, technological advancement, and economic growth. The depletion of conventional or non-renewable energy sources along with environmental issues have become important matters of global concern due to the rise in energy demand. To cater for the need for increasing energy demand, a high-efficiency energy conversion system for industrial processes is essential. Furthermore, to fulfill energy demands and reduce the use of conventional energy sources, energy generation from non-conventional or renewable sources is essential. Adequate renewable sources such as Solar, Wind, Biomass, Ocean, and Geothermal, are capable of accomplishing clean and green energy without affecting the environment. Solar photovoltaic (PV) and wind are prominent among available renewable sources to generate power [1,2]. To harvest controlled power efficiently from these renewable sources, a suitable power conversion system is needed [3,4]. Further, for the efficient utilization of power generated by these sources, a grid integration is required.

Power electronic converters play a vital role in harvesting efficient power from renewable energy sources and for interconnection through a utility grid. The voltage source

inverter (VSI) is the most commonly used natural interfacing device for grid-connected applications due to better controllability with higher efficiency [1,5]. In order to harvest high-quality power through VSIs interconnected to a utility grid, appropriate controllers with rapid response and fast reference tracking ability are always desired. Further, controllers need to meet the expectations of various control objectives for grid-connected VSI, such as power factor correction, by regulating the current through the grid, harmonic reduction and power flow regulation [6,7]. A general block diagram of a three-phase grid-connected VSI system is depicted in Figure 1 which can be driven by dc sources such as battery, PV or fuel cell.

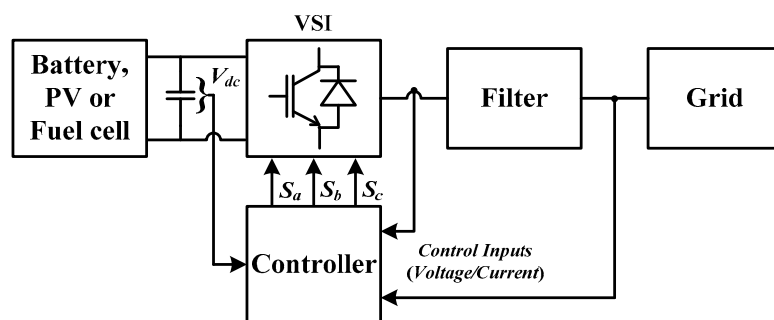


Figure 1. Block diagram of three-phase grid-connected VSI system.

Various conventional voltage, as well as current control, techniques have been studied and implemented for grid connected VSI applications. Conventional linear proportional-integral (PI) regulator-based space vector modulation (PI-SVM) and nonlinear hysteresis controller-based hysteresis current control (HCC) are well-established voltage and current control schemes used in industrial applications, respectively [8–17]. The PI-SVM technique possesses features such as switching frequency reduction, lower total harmonic distortion (THD) and better utilization of dc supply voltage with fixed switching frequency [8,10,11]. However, increased complexity is a concern due to various computations such as sector identification, switching time calculation, switching voltage vector identification and an optimum switching pattern in each sampling time. An improved PI-SVM from an implementation point of view has been proposed in [12,13] to generate switching times for inverter switches directly from the instantaneous sampled reference phase voltages. Due to the elimination of various computations involved in conventional PI-SVM, this improved technique has been considered a better scheme for experimental implementation. On the other hand, HCC is considered as a mature technique having features of accuracy, simplicity and good dynamic performance [14–16]. However, the variable switching frequency is the key factor of this technique. Further, switching frequency is crucial due to its dependency on system parameters and operating conditions.

Among modern control schemes, model predictive control (MPC) has become attractive to researchers for voltage as well as current control application of power electronics and drives. MPC possesses attractive features such as intuitive nature, excellent dynamic performance, functionality for the inclusion of constraints, and nonlinearities [17–23]. However, implementation needs fast and powerful digital signal processors (DSPs) and microprocessors due to the high computational requirements of MPC. Finite control-set MPC (FCS-MPC) or finite-state MPC (FS-MPC) is one of the categories of MPC that is based on the discrete-time model of the system and the limited number of switching states of the power converter [18,20–23]. The inherent discrete nature of the FS-MPC suits the algorithm implementation through digital platforms. Moreover, the discrete-time model of the power converter with short prediction horizon assists in reducing the online computations of the FS-MPC algorithm. Because of above mentioned features, FS-MPC has been extensively studied and applied for the various power converter and drive applications including inverters connected through the grid [24–27]. A compar-

ison among the control schemes is depicted in Table 1 to gain an understanding of their pros and cons.

Table 1. Advantages and Disadvantages of Control Schemes.

	Advantages	Disadvantages
PI-SVM	<ul style="list-style-type: none"> ☑ Design with Known Bandwidth ☑ Simple to Extend to Different Topologies due to Modulator ☑ Constant Switching Frequency ☑ Decreases Harmonic Content ☑ Mature Scheme (Used in Commercial Drives) 	<ul style="list-style-type: none"> ☒ Not Easy to Adapt for Special Requirements (Constraints, Nonlinearities, etc.) ☒ Slower Dynamics due to requirement of Modulator ☒ Usually Requires Coordinate Transformation
HCC	<ul style="list-style-type: none"> ☑ Nonlinear Controller, Very Robust ☑ No Modulator Required ☑ Very Fast Dynamic Performance ☑ Simple Design ☑ Well Established and Mature Scheme 	<ul style="list-style-type: none"> ☒ Digital Implementation Requires High Sample Rate ☒ Variable Switching Frequency ☒ Creates Resonance Problems ☒ Difficulty in Extending for Different Converter Topologies
MPC	<ul style="list-style-type: none"> ☑ Nonlinear Controller ☑ Modulator not Required ☑ Can Include Nonlinearities and Constraints ☑ Intuitive Design Based on Prediction Model and Cost Function 	<ul style="list-style-type: none"> ☒ Variable Switching Frequency ☒ High Computational Requirements ☒ High Dependency on Model Parameters ☒ Complex Design of Weighting Factors

The real-time implementation of PI-SVM and FS-MPC based systems needs digital platforms because of computational requirements. On the other hand, although HCC based systems are mainly implemented through analog circuits, lack of flexibility is one of the key issues of analog solutions. Thus, digital platforms with increased performance are required for experimental system implementation. Moreover, the availability of platforms with the functionality of modeling based digital system design and field-programmable gate array (FPGA) based hardware-in-the-loop (HIL) testing eases overall system development.

FPGA has gained attraction and is considered a more appropriate solution for digital implementation due to its flexibility and parallel processing architecture which can handle multiple operations together within the specified sampling time [28–33]. Further, FPGA based system implementation makes the system compact, cost-effective and reduces execution time drastically. A hardware description language (HDL), such as Verilog or VHDL, is used to implement an FPGA controller, which needs special training in HDL programming, extensive design-phase optimization and verification. It takes a lot of work to implement FPGA-based systems using a conventional HDL programming approach. FPGA vendors have thankfully provided high-level design tools, such as high-level synthesis (HLS) and block diagram-based design toolboxes such as System Generator for DSP from Xilinx and DSP Builder from Altera to aid in the acceleration of the development process [30]. However, System Generator for DSP from Xilinx provides the additional functionality of HIL testing including the ability to generate HDL code intuitively to configure FPGA [31,34–36].

In this paper, a comprehensive analysis of a grid-connected VSI system is presented considering conventional linear control PI-SVM, conventional nonlinear control HCC and modern control FS-MPC techniques. The controllers are developed in a model-based design platform named System Generator for DSP, provided by Xilinx for digital implementation, which is an integrated platform with MATLAB-Simulink. Furthermore, the FPGA HIL co-simulation functionality of System Generator, a dedicated simulator platform provided by Xilinx, is utilized for one step ahead controller validation before actual experimental system implementation. The controller performances are analyzed with the help of some necessary performance parameters such as grid synchronization, transient performance and effect of different sampling.

Other sections of this paper are organized as follows: Section 2 represents the discrete-time mathematical model of the grid-connected VSI system. Section 3 deals with the design and development of system controls. The HIL co-simulation methodology for FPGA

based system implementation is presented in Section 4. In Section 5, simulation results and discussion are presented with comparative analysis. Finally, appropriate conclusions are drawn in Section 6.

2. Discrete-Time Mathematical Model of System

A schematic diagram of the three-phase grid-connected VSI system in Figure 2 consists of a filter at inverter output side, three-phase grid and a dc supply to VSI. The three-phase VSI consists of 3 legs (a, b, and c) with two power switches (IGBTs) in each leg: S_1 – S_4 (leg a), S_2 – S_5 (leg b) and S_3 – S_6 (leg c). S_1, S_2, S_3 are termed as upper switches and S_4, S_5, S_6 lower switches.

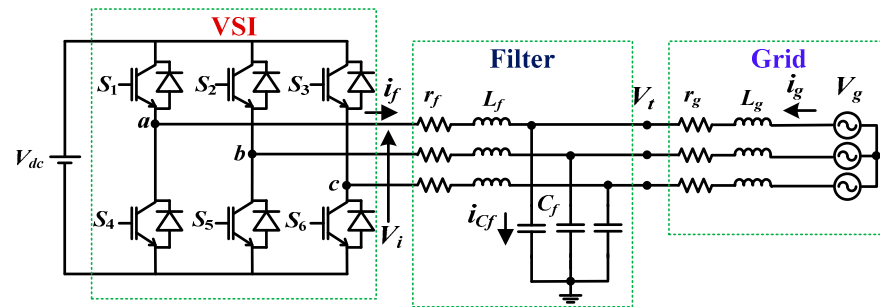


Figure 2. Schematic diagram of three-phase grid-connected VSI system.

2.1. Switching States and Voltage Vectors

Switching states of VSI are interpreted corresponding to the switching signals applied to the upper (S_1, S_2, S_3) and lower (S_4, S_5, S_6) switches that are complementary to each other. The switching states S_a, S_b, S_c in Table 2 denote the switching signals applied to IGBTs corresponding to three legs. The switching states S can be expressed in vector form as

$$S = \frac{2}{3} (S_a + aS_b + a^2S_c), \text{ where } a = e^{j\frac{2\pi}{3}} \tag{1}$$

Table 2. Switching Signals for Inverter Switches.

Leg a, S_a	Leg b, S_b	Leg c, S_c
S_1 ON, 1	S_2 ON, 1	S_3 ON, 1
S_4 OFF, 0	S_5 OFF, 0	S_6 OFF, 0
S_1 OFF, 0	S_2 OFF, 0	S_3 OFF, 0
S_4 ON, 1	S_5 ON, 1	S_6 ON, 1

The inverter output voltages V_i are controlled by switching states and a resulting eight voltage vectors ($V_0 \sim V_7$). Here $V_1 \sim V_6$ are active vectors and V_0 & V_7 are zero vectors. The voltage vectors with respect to switching states S_a, S_b and S_c , depicted in Table 3, can be formulated in complex space vectors as

$$V_i = \begin{cases} \frac{2}{3} V_{dc} e^{j(i-1)\frac{\pi}{3}}, & \text{for } i = 1 \sim 6 \\ 0 & , \text{for } i = 0, 7 \end{cases} \tag{2}$$

Table 3. Voltage Vectors and Switching States.

Voltage Vectors V_i	Switching States $S_a S_b S_c$	$\alpha\beta$ Components of Voltage Vectors	
		$V_{i\alpha}$	$V_{i\beta}$
V_0	0 0 0	0	0
V_1	1 0 0	$2V_{dc}/3$	0
V_2	0 1 0	$-V_{dc}/3$	$\sqrt{3}V_{dc}/3$
V_3	1 1 0	$V_{dc}/3$	$\sqrt{3}V_{dc}/3$
V_4	0 0 1	$-V_{dc}/3$	$-\sqrt{3}V_{dc}/3$
V_5	1 0 1	$V_{dc}/3$	$-\sqrt{3}V_{dc}/3$
V_6	0 1 1	$-2V_{dc}/3$	0
V_7	1 1 1	0	0

2.2. Discrete-Time Model

The three-phase grid-connected VSI system can be described by continuous-time dynamic Equations (3)–(5) as follows:

$$L_f \frac{di_f}{dt} = V_i - r_f i_f - V_t \tag{3}$$

$$C_f \frac{dv_t}{dt} = i_f + i_g \tag{4}$$

$$L_g \frac{di_g}{dt} = V_g - V_t - r_g i_g \tag{5}$$

where

- L_f : filter inductance,
- r_f : internal loss resistance of filter inductor,
- C_f : filter capacitance,
- r_g : grid resistance,
- L_g : grid inductance,
- i_f : three-phase filter currents flowing from the inverter,
- V_t : three-phase terminal voltage at point of common coupling,
- i_g : three-phase grid currents.

These continuous-time relations in Equations (3)–(5) can be represented by state-space model as

$$\begin{cases} \frac{dx(t)}{dt} = A_c x(t) + B_c u(t) \\ y(t) = C_c x(t) \end{cases} \tag{6}$$

where $x(t) = [i_f \ V_t \ i_g]^T$, $y(t) = i_f$ and $u(t) = [V_i \ V_g]^T$.

The continuous-time state-space matrices A_c , B_c , and C_c are as follows:

$$A_c = \begin{bmatrix} -r_f/L_f & -1/L_f & 0 \\ 1/C_f & 0 & 1/C_f \\ 0 & -1/L_g & -r_g/L_g \end{bmatrix}, B_c = \begin{bmatrix} 1/L_f & 0 \\ 0 & 0 \\ 0 & 1/L_g \end{bmatrix} \text{ and } C_c = [1 \ 0 \ 0].$$

The discrete-time state-space model from continuous-time model in Equation (6) is obtained by discretization with a sampling time T_s and the model is represented at sampling instant k as

$$\begin{cases} x(k+1) = A_d x(k) + B_d u(k) \\ y(k) = C_d x(k) \end{cases} \tag{7}$$

And,

$$\begin{cases} A_d = e^{A_c T_s} \\ B_d = \int_0^{T_s} e^{A_c \tau} B_c d\tau \\ C_d = C_c \end{cases} \tag{8}$$

where $x(k) = [i_f(k) \ V_t(k) \ i_g(k)]^T$, $y(k) = i_f(k)$ and $u(k) = [V_i(k) \ V_g(k)]^T$.

3. Modeling of System Control

The grid-connected VSI system as represented in Figure 2 is designed considering control techniques PI-SVM, HCC and FS-MPC for comprehensive analysis. The control system is developed through model-based design in a system generator provided by Xilinx (XSG) followed by MATLAB-Simulink [34].

3.1. PI-Based Space Vector Modulation (PI-SVM)

The Carrier-Based modulation technology, which is employed in the three-phase VSI application, can be replaced by space vector modulation. Both approaches convert a reference voltage into inverter switching signals, which is how they are comparable. Eight switching states, including six active and two zero states, are produced by the three-phase VSI. These vectors combine to produce a hexagon, which may be thought of as having six sectors with span of 60° each. PI-SVM is used to generate the reference vector, which represents the three-phase sinusoidal voltage, by switching between the two nearest active vectors and the zero-vector depicted in Table 2. The block diagram of the grid-connected VSI system controlled with PI-SVM technique is presented in Figure 3. The current control of the system is realized using dq synchronous rotating frame. In order to eliminate the current errors in dq components, two PI controllers are used. These PI regulators convert the current errors into reference voltage errors (dq components) which are further transformed into abc components using inverse Park transformation (Equation (9)) and given to SVM control. Briefly stated, the PI-SVM algorithm divides the reference vector into effective vectors corresponding to the sectors, and then recombines these effective vectors to produce the actual PWM switching pattern. Therefore, because of the standard SVM method's fundamental approach, the total calculation procedure is difficult to implement in practice. However, it is possible to recreate the real gating time without performing a partitioning or recombination operation by applying the effective voltage vector notion of the standard SVPWM in a different method. To generate switching signals by using reference phase voltages through SVM control, the required computational steps are demonstrated in a block diagram as shown in Figure 4.

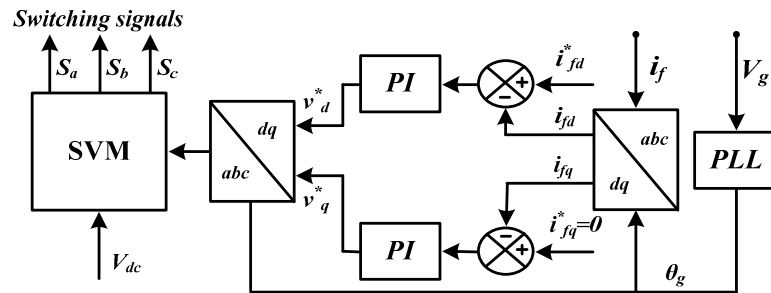


Figure 3. Block diagram of PI-SVM for grid-connected VSI system.

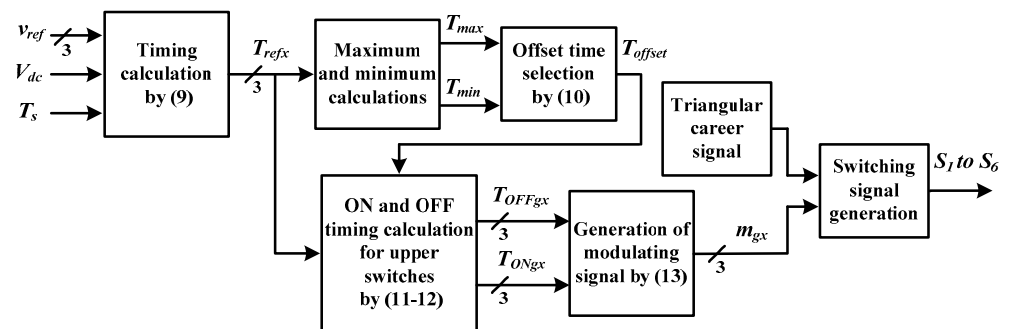


Figure 4. Block diagram for computational steps for SVM.

These computational steps can be represented in the following four subsections [12,13].

3.1.1. Reference Time Calculation

Firstly, sampled reference phase voltages v_{refa} , v_{refb} , and v_{refc} of the present sampling interval are used to calculate the time equivalents of these phase voltages known as reference times T_{refa} , T_{refb} , and T_{refc} . The calculation of reference time T_{refx} ($x = a, b, c$) for each phase corresponding to the particular reference phase voltage is formulated in Equation (9) as

$$T_{refx} = V_{refx} \left(\frac{T_s}{V_{dc}} \right), \text{ where } x = a, b, c \quad (9)$$

where T_s is the sampling time.

It can also be noted that, since $v_{refa} + v_{refb} + v_{refc} = 0$, hence, $T_{refa} + T_{refb} + T_{refc} = 0$.

3.1.2. Offset Time Computation

The offset time is required to distribute the zero voltage symmetrically during one sampling interval. To determine the effective time (T_{eff}) to the middle of the sampling interval, the zero-voltage time (T_0) is subjoined to the imaginary phase voltage times and will be symmetrically distributed at the start and end of one sample period. The offset time T_{offset} is determined using a straightforward three-element sorting technique. Only the maximum and minimum value among the three imaginary phase voltage times is necessary for this sorting technique. The offset time is calculated using the following equations as

$$\begin{cases} T_{eff} = T_{max} - T_{min} \\ T_0 = T_s - T_{eff} \\ T_{min} + T_{offset} = T_0/2 \end{cases} \quad (10)$$

$$T_{offset} = \frac{T_0}{2} - T_{min} \quad (11)$$

after substituting the values of T_0 and T_{eff} in Equation (11), T_{offset} can be calculated, as given in Equation (12)

$$T_{offset} = 0.5T_s - 0.5(T_{max} + T_{min}) \quad (12)$$

where T_{max} and T_{min} are the maximum and minimum of reference times, respectively, computed in Equation (9).

3.1.3. Timing Calculation for Inverter Switches

The actual switching times for inverter switches can now simply be obtained with the help of reference time calculated in Equation (9) and offset time calculated in Equation (12). The switching times (OFF sequence) for upper switches of VSI (S_1, S_2, S_3) can be obtained as follows:

$$T_{OFFgx} = T_{refx} + T_{offset}, \text{ where } x = a, b, c \quad (13)$$

In order to generate a symmetrical switching pattern, ON switching sequence is obtained by subtracting OFF sequence from sampling time as

$$T_{ONgx} = T_s - T_{OFFgx}, \text{ where } x = a, b, c \quad (14)$$

3.1.4. Generation of Modulating Signal

A modulating signal generation scheme is used to generate PWM switching signals for VSI switches using fixed frequency triangular career. The modulating signal for each phase is obtained from switching times calculated in step 3 as

$$m_{gx} = 2 \left(\frac{T_{OFFgx} - T_{ONgx}}{T_s} \right) - 1, \text{ where } x = a, b, c \quad (15)$$

3.2. Hysteresis Current Control (HCC)

The HCC scheme is one of the most widely used current control techniques for power electronics applications and it is considered as one of the simplest and mature control schemes in industrial applications. This scheme is based on the current error between the load current and reference current. The concept of this method is to keep the error within the specified tolerance band, the hysteresis band/error band. The switching signals for inverter power switches are generated through a hysteresis controller which has a non-linear nature. The actual current is forced to follow a sinusoidal current reference within the error band.

The block diagram of HCC for three-phase grid-connected VSI is shown in Figure 5. The reference current is generated considering only active power fed to the grid side from the inverter side. e_a, e_b and e_c are the current errors between measured filter currents i_f and generated reference currents i_f^* . The hysteresis controller used for switching signal generation has an upper hysteresis band (+HB) and lower hysteresis band (−HB). The switching signals are generated based on current error crossing the +HB and −HB. The expression for instantaneous switching frequency f_{sw} [15,16] for the given grid-connected system can be obtained as

$$f_{sw} = \frac{V_{dc}}{4L_f(HB)} \left[1 - \left\{ \frac{L_f}{V_{dc}} \left(\frac{di_f^*}{dt} - \frac{V_g}{L_f} \right) \right\}^2 \right] \tag{16}$$

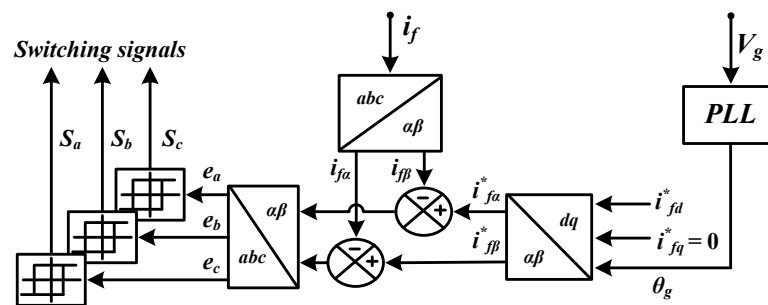


Figure 5. Block diagram of HCC for grid connected VSI system.

The expression of f_{sw} in Equation (16) depends on the system parameters (V_{dc}, L_f) as well as rate of change of i_f^* and HB. The maximum switching frequency f_{swmax} can be obtained by using Equation (16) as

$$f_{swmax} = \frac{V_{dc}}{4L_f(HB)} \tag{17}$$

The inversely proportional relation of the f_{swmax} and HB for a particular system results in the varying switching frequency, corresponding to the +HB and −HB.

3.3. Finite State Model Predictive Control (FS-MPC)

FS-MPC utilizes the discrete-time model of the power converter as a predictive model which is a first step for the implementation of the FS-MPC algorithm. The predictive model provides the information about the future behavior of the predicted variables for each switching state in every sampling interval. The next step is to formulation of an optimization function (also called cost function) that is defined based on the error between the predicted variables and the desired reference. Cost function is computed in consequence of the predicted variables and, correspondingly, minimum cost function is selected in every sampling interval. Further, an optimum switching state is selected based on the minimum cost function in each sampling interval and applied to the power converter for switching operation.

A block diagram of FS-MPC for three-phase grid-connected VSI system is shown in Figure 6. The model-based implementation process depicted in Figure 7 of FS-MPC for the given system is described in following two subsections.

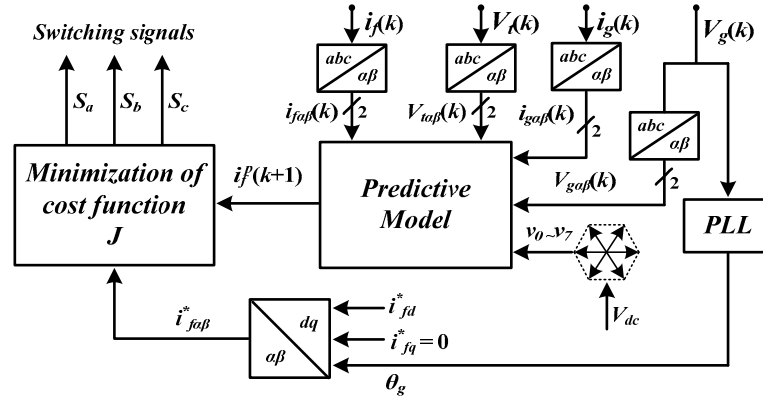


Figure 6. Block diagram of FS-MPC for grid-connected VSI system.

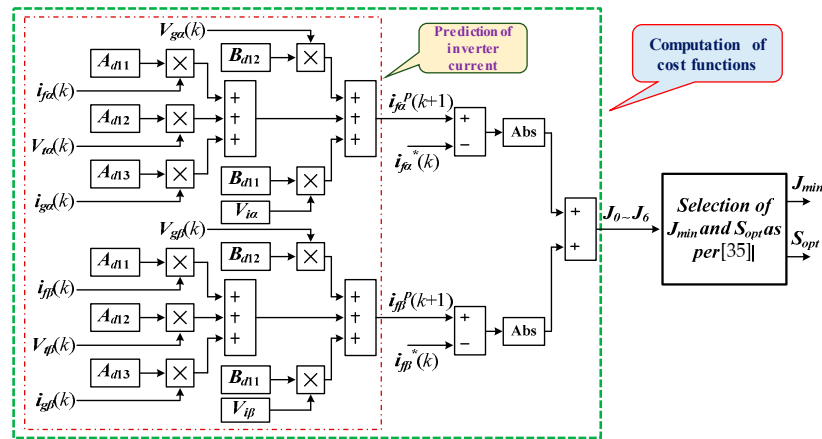


Figure 7. Block diagram for FS-MPC implementation [35].

3.3.1. Predictive Model

The discrete-time state-space model of the grid-connected VSI system described in Equations (7) and (8) of Section 2, is used as a predictive model that computes the prediction of future variables based on $\alpha\beta$ components of the measured parameters $i_f(k)$, $V_t(k)$, $i_g(k)$ and $V_g(k)$ at the k^{th} sampling interval. An expression for the prediction of the future values of the filter current $i_f^p(k+1)$ in the $(k+1)^{\text{th}}$ sampling interval for each of the possible switching states of the VSI, can be reproduced using the first row elements of system matrix A_d and the first row elements of control matrix B_d in Equation (7) as

$$i_f^p(k+1) = A_{d11}i_f(k) + A_{d12}V_t(k) + A_{d13}i_g(k) + B_{d11}V_i(k) + B_{d12}V_g(k) \quad (18)$$

where A_{d11} , A_{d12} , A_{d13} are the first row elements of system matrix A_d . B_{d11} , B_{d12} are the first row elements of control matrix B_d .

3.3.2. Cost Function

Based on the predicted filter current $i_f^p(k+1)$, an expression of cost function J is formulated with respect to the generated reference current $i_f^*(k+1)$ considering real and imaginary components of filter currents as

$$J = \left| i_{f\alpha}^*(k+1) - i_{f\alpha}^p(k+1) \right| + \left| i_{f\beta}^*(k+1) - i_{f\beta}^p(k+1) \right| \quad (19)$$

where $i_{f\alpha}^*(k+1)$, $i_{f\beta}^*(k+1)$ are the real, imaginary components of the reference current and $i_{f\alpha}^p(k+1)$, $i_{f\beta}^p(k+1)$ are the real, imaginary components of the predicted filter current, respectively, at sampling instant $k+1$.

The model-based design of the predictive model (Equation (18)) and the cost function (Equation (19)) are developed with the help of Xilinx blocksets available in the Simulink library, such as Constant, AddSub, Mult, Absolute, etc. A logic for the selection and application of optimum switching state is demonstrated extensively in [34].

4. HIL Simulation Methodology

HIL methodology is considered an intermediate level between the fully software-based simulation and the actual experimental system implementation for validation of controls. The verification through HIL is to reduce the possibility of system failure due to an inappropriate control system. Moreover, this functionality provides an atmosphere that can be used for wide testing conditions which are a tedious and risky task during the real experiment. Further, this functionality provides an atmosphere for wide testing conditions which are not possible during the real experiment. In FPGA based HIL co-simulation, the developed controller in hardware (FPGA) interacts with the virtual system designed in the software. In addition, it provides fast execution of complex simulations which generally take a long time for execution in software [33,34].

The process for FPGA HIL co-simulation is presented in Figure 8 with the model of the grid-connected system (VSI, filter, grid) developed in MATLAB-Simulink and the step-by-step design and modeling of controls performed in MATLAB-Simulink, digital simulator (XSG) and HIL. For a detailed description of this approach, the flowchart is presented in [34].

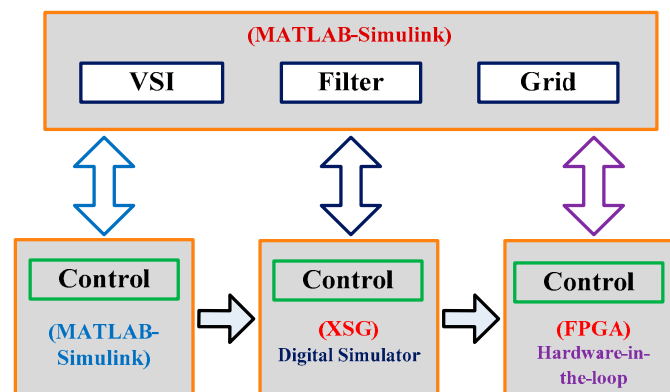


Figure 8. Block diagram representing steps for FPGA HIL co-simulation.

5. Results and Discussion

The three-phase grid-connected VSI system is developed considering the three mentioned control strategies modeled in XSG followed by MATLAB-Simulink. The grid-connected system is simulated through the HIL co-simulation approach using an FPGA board: ZedBoard Zynq evaluation and development FPGA kit.

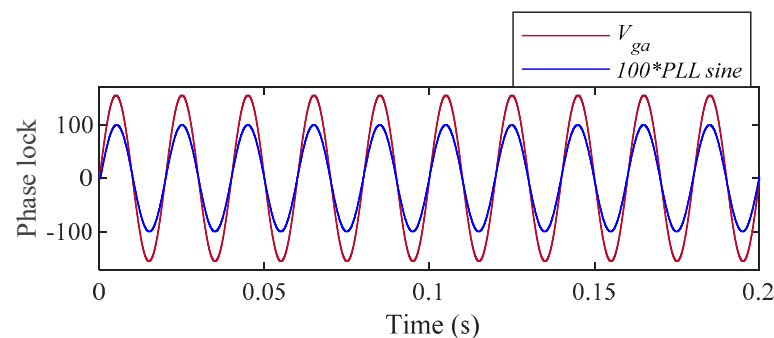
The comparative analysis is performed among the chosen control techniques based on phase synchronization, dynamic response, sampling time (T_s) and THD in currents. The parameters considered for the grid connected VSI system are listed in Table 4 including PI controller parameters used in PI-SVM control. The optimum values of PI controller parameters (K_p and K_i) are obtained using Trial and Error Method.

Table 4. System Parameters.

Parameter	Value	Description
V_{dc}	400 V	Supply dc
r_f	0.1 Ω	Filter loss resistance
L_f	4 mH	Filter inductance
C_f	20 μ F	Filter capacitance
r_g	0.1 Ω	Grid resistance
L_g	1 μ H	Grid inductance
V_g	110 V, 50 Hz	Grid phase voltage
T_s	50, 25, 10 μ s	Sampling time
K_p	0.08	Proportional gain
K_i	200	Integral gain

5.1. Phase Synchronization

PLL is required to synchronize phases between grid voltage and grid current for feeding only active power to the grid. The performance of digitally designed PLL is required to be verified with the correct phase capturing capability. The performance of PLL is shown in Figure 9 considering phase tracking of grid phase ‘a’ with the PLL output sine signal (scaled 100 times for clear observation).

**Figure 9.** Phase capturing of PLL.

Further, the system performance is investigated only for active power feed to the grid from the inverter and the reference current is generated by taking zero reactive power component for that operation. Although, the grid current should be in the phase to the grid voltage for unity power factor operation, the direction taken by the grid current is opposite (away from the grid), as depicted in Figure 2. Hence, grid current will be 180° out of phase with the grid voltage for only active power feed from the inverter side to the grid side according to the assumption. The FPGA HIL co-simulation results for grid voltage and current (phase ‘a’) are shown in Figure 10 for all three considered control techniques: PI-SVM, HCC, and FS-MPC. The grid current is scaled twice for clearer understanding.

5.2. Transient Performance

The analysis of controller performance at the transients describes the speed of the controller, that is, how fast the controller can tackle any sudden change and go to a steady state. In the case of PI-SVM, the dynamic performance depends on the linear (PI) controller parameters (modulator gain K_p , K_i) that gives a slightly sluggish response at transients. The transient response is observed considering a step change in the reference current from 15 A to 30 A at $t = 0.11$ s. The transient performance of PI-SVM, HCC and FS-MPC is analyzed based on the reference current tracking in Figure 11 considering $\alpha\beta$ stationary reference frame with the step change as reference.

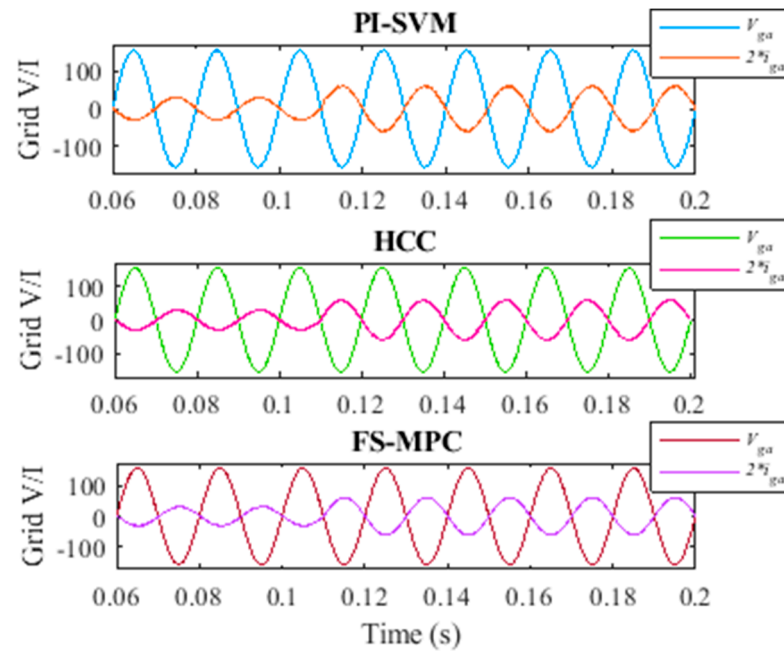


Figure 10. Grid voltage and current (phase 'a') for PI-SVM, HCC, and FS-MPC.

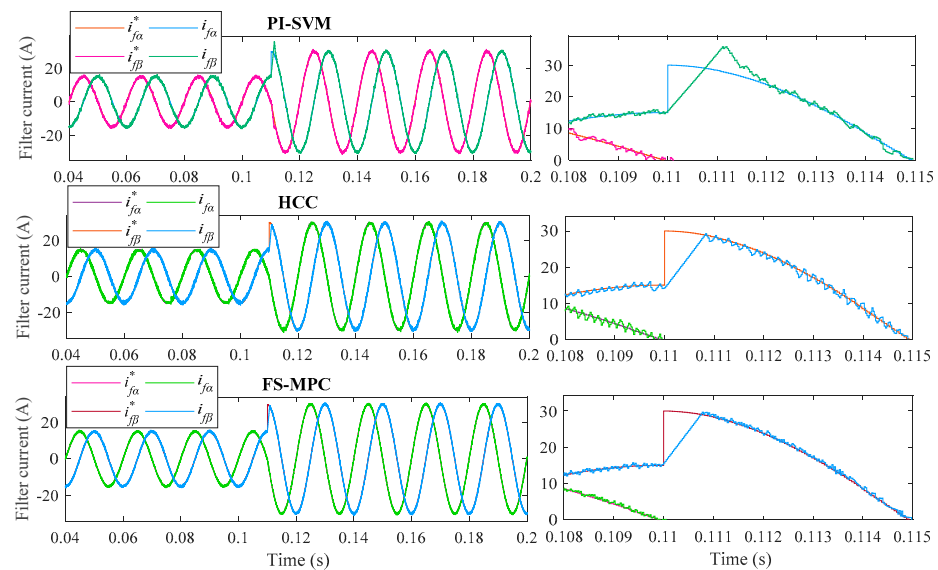


Figure 11. Reference current tracking with a step change from 15 to 30 A at $t = 0.11$ s for PI-SVM, HCC, and FS-MPC.

5.3. Effect of Sampling Time

The sampling time (T_s) is a crucial factor for the implementation of control techniques in digital platforms. Hence, the effect of a change in T_s is required to be observed for an in-depth analysis of considered control techniques. The system performance is analyzed considering different T_s .

In the case of PI-SVM, the FPGA HIL co-simulation results for filter and grid currents for $T_s = 50, 25 \mu\text{s}$ are depicted in Figure 12a,b. The harmonic contents in both currents are also presented in Figure 13 considering different T_s . It is quite pertinent that the percentage THD is more for higher T_s ; however, the shape of currents maintains sinusoidal behavior with three balanced phases. Moreover, for comparative analysis with other controls, a fixed switching frequency (f_{sw}) is considered comparable to the average switching frequencies of HCC and FS-MPC.

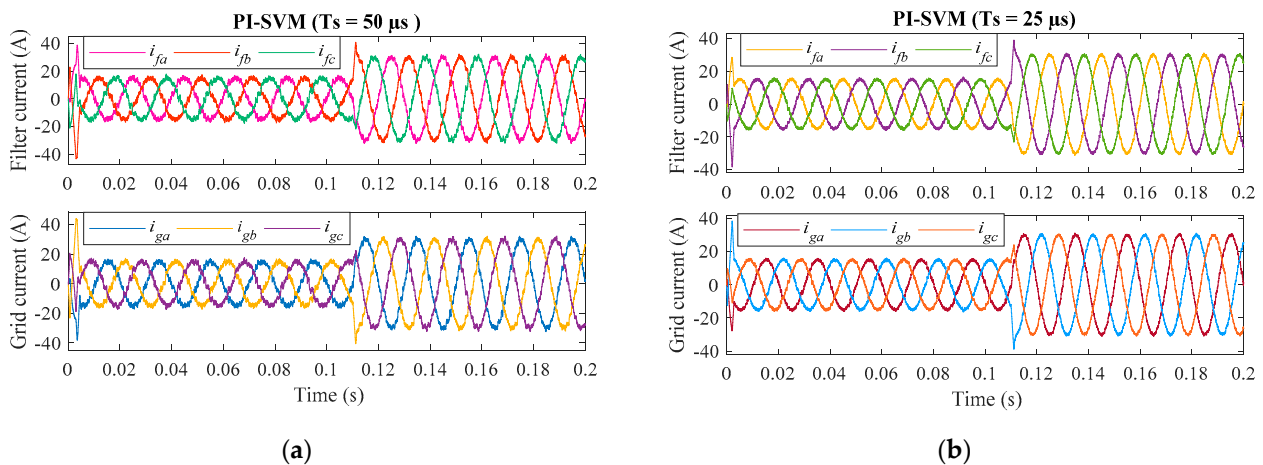


Figure 12. Filter current and grid current with a step change using PI-SVM for (a) $T_s = 50 \mu\text{s}$, (b) $T_s = 25 \mu\text{s}$.

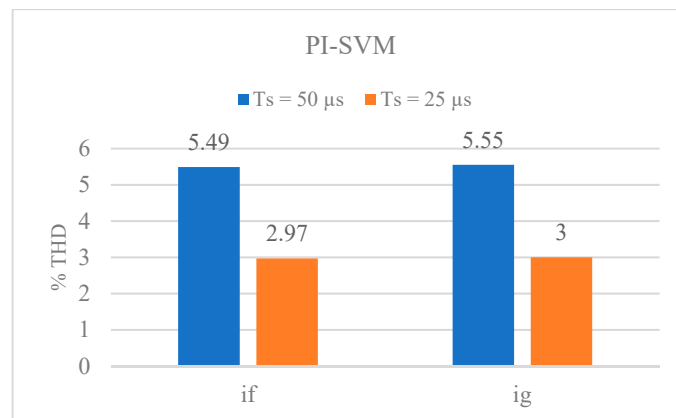


Figure 13. Percentage THD in filter and grid current with PI-SVM for $T_s = 50, 25 \mu\text{s}$.

The performance of HCC is illustrated based on the different T_s and change in hysteresis band (HB). The filter and grid currents are depicted in Figure 14a,b for HB = 2.5 A ($T_s = 50 \mu\text{s}$) and HB = 1.25 A ($T_s = 25 \mu\text{s}$), respectively. The value of HB is selected based on the limitation of maximum switching frequencies (f_{swmax}) according to the relation given in equation (15) for the comparative analysis. The percentages THD in filter and grid currents are also presented in Figure 15 based on the variation in T_s (50, 25 μs) as well as HB (2.5, 1.25, 0.75). The results show that the performance of HCC depends on both T_s and HB. The performance can be improved by using lower T_s as well as HB. However, as HB decreases, the f_{swmax} also increases which creates another issue related to the f_{swmax} rating of power devices, and f_{swmax} requirement increases the switching losses simultaneously.

In order to investigate the performance of FS-MPC and to compare with the other control techniques discussed above, HIL co-simulation is performed with different T_s (50, 25 μs). The results for filter and grid currents are depicted in Figure 16a,b for $T_s = 50 \mu\text{s}$ and $T_s = 25 \mu\text{s}$, respectively, and the percentage THD in the filter and grid current is demonstrated in Figure 17 for corresponding sampling times. A significant decrement in THD is observed with lower T_s for both currents. However, in the case of FS-MPC, the f_{swmax} is inversely proportional to T_s and it is considered as half of sampling frequency f_s . Hence, the maximum switching frequency permissible to a particular power device is one of the concerns for the selection of T_s .

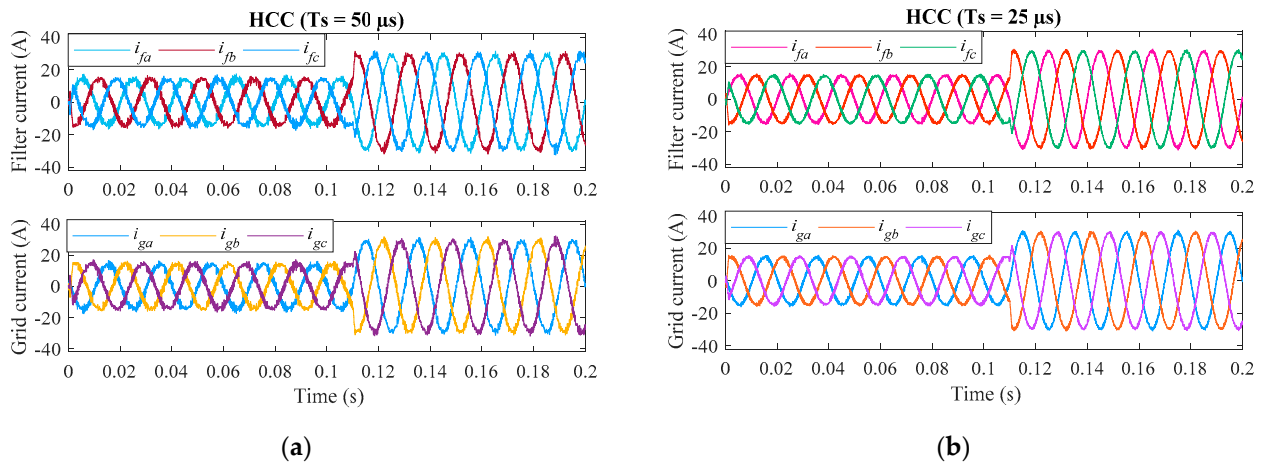


Figure 14. Filter current and grid current with a step change using HCC for (a) $T_s = 50 \mu s$ ($HB = 2.5 A$), (b) $T_s = 25 \mu s$ ($HB = 1.25 A$).

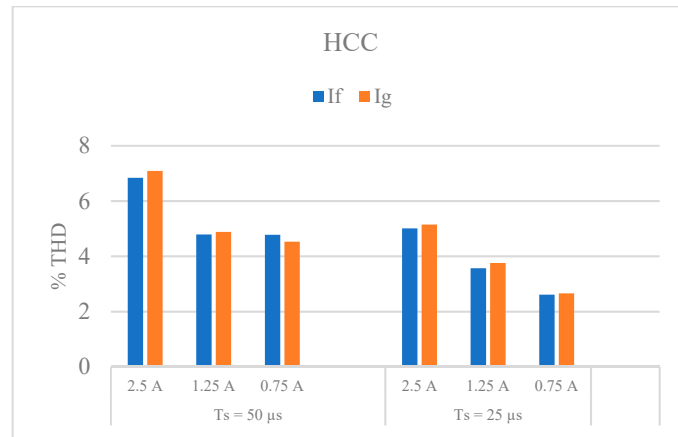


Figure 15. Percentage THD in filter and grid current with HCC for $T_s = 50, 25 \mu s$ and $HB = 2.5, 1.25, 0.75 A$.

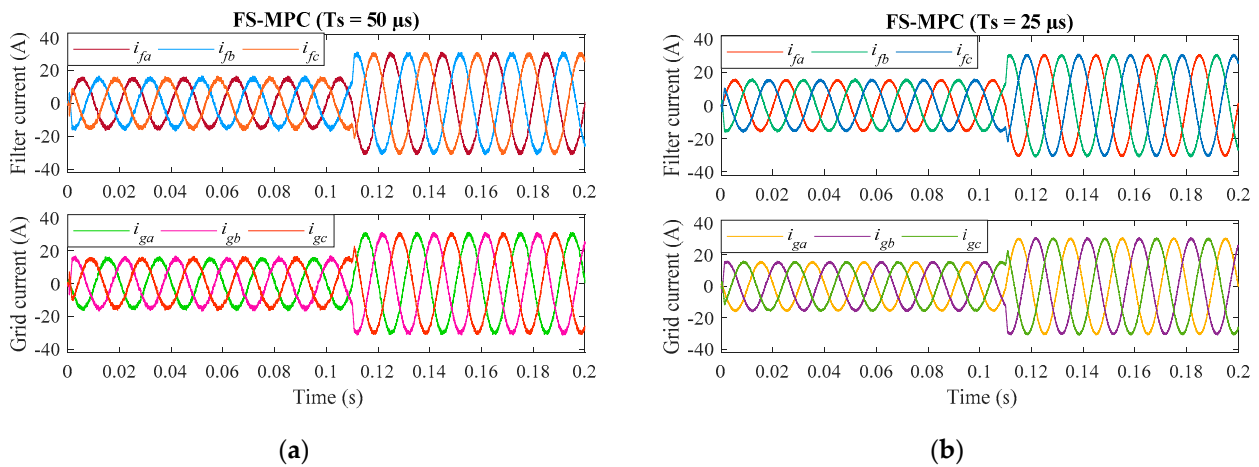


Figure 16. Filter current and grid current with a step change using FS-MPC for (a) $T_s = 50 \mu s$, (b) $T_s = 25 \mu s$.

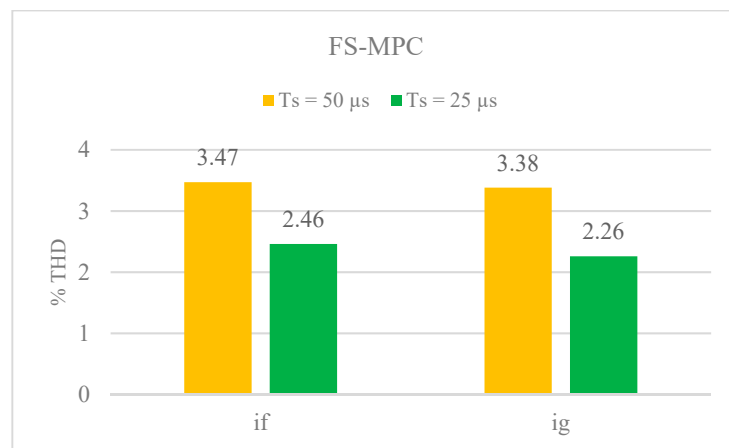


Figure 17. Percentage THD in filter and grid current with FS-MPC for $T_s = 50, 25 \mu s$.

A comparative analysis considering the THD variation discussed above in grid current (i_g) with various parameters based on the respective control technique is presented in Figure 18. The grid current THD shows a decreasing trend corresponding to decrease in T_s for all control techniques. The percentage THD is lowest in the case of FS-MPC as compared to other controls for the considered cases of T_s . However, even lower T_s is required for the similar decrement in THD based on the switching frequency considered for PI-SVM. Further, in the case of HCC, the decrement in THD is dependent on T_s , as well as HB.

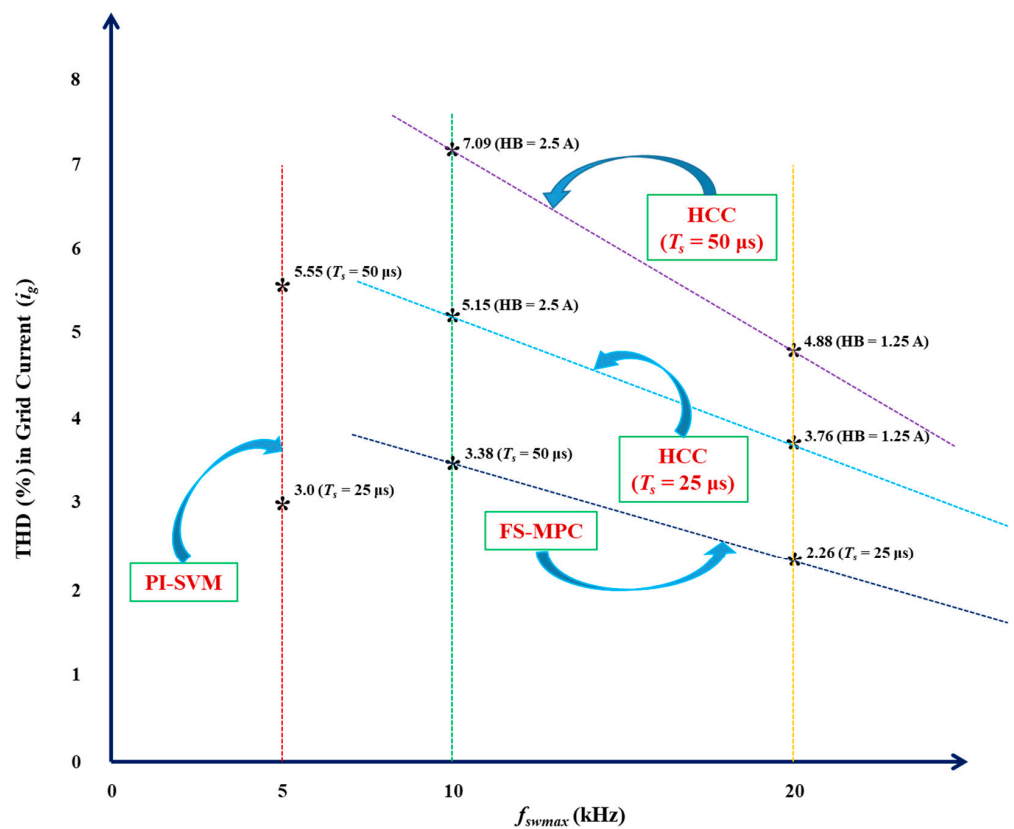


Figure 18. Comparison diagram for percentage THD in grid current.

6. Conclusions

In this paper, an insight into controller techniques PI-SVM, HCC, and FS-MPC considering the three-phase grid-connected VSI system is provided for digital implementation

through FPGA HIL co-simulation. The controller analysis is performed based on the effect of sampling time and dynamic response: transient condition and current tracking. The sampling time influences the controller performance significantly for the constant switching frequency condition of PI-SVM, as well as the variable switching frequency condition of HCC and FS-MPC. The influence of sampling time is most dominant in the case of PI-SVM considering percentage THD in current and improved significantly for lower sampling times; however, the dynamic performance is poor due to the modulator, as compared to non-linear controllers.

On the other hand, HCC has inherent modulator characteristic and demonstrates better dynamic response compared to PI-SVM; however, the hysteresis band decides the maximum switching frequency and sampling time, which are the governing factors considering percentage THD in the current. The FS-MPC demonstrated better performance even at higher sampling time as compared to PI-SVM and HCC considering both the quality parameters: percentage THD and dynamic response. In addition, performance characteristics demonstrated at higher sampling time are comparable to the performance of PI-SVM at lower sampling time and performance of HCC at lower sampling time and smaller hysteresis band. In the case of FS-MPC, the sampling time directly governs the maximum switching frequency, therefore lower sampling time is more feasible for high-frequency switching devices.

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