processes

MDPI

Article

Back-Channel Etched In-Ga-Zn-O Thin-Film Transistor Utilizing Selective Wet-Etching of Copper Source and Drain

Rauf Khan [1,2,*], Muhamad Affiq Bin Misran [1,2], Michitaka Ohtaki [1,2], Jun Tae Song [3,4], Tatsumi Ishihara [3,4] and Reiji Hattori [1]

1 Department of Applied Science for Electronics and Materials, Interdisciplinary Graduate School of Engineering Sciences, Kyushu University, Fukuoka 816-8580, Japan; muhamad.affiq90@gmail.com (M.A.B.M.); ohtaki@kyudai.jp (M.O.); hattori@gic.kyushu-u.ac.jp (R.H.)
2 Transdisciplinary Research and Education Center for Green Technologies, Kyushu University, Fukuoka 816-8580, Japan
3 Department of Applied Chemistry, Faculty of Engineering, Kyushu University, Fukuoka 819-0395, Japan; song.juntae@cstf.kyushu-u.ac.jp (J.T.S.); ishihara@cstf.kyushu-u.ac.jp (T.I.)
4 WPI, International Institute for Carbon-Neutral Energy Research (WPI-I2CNER), Kyushu University, Fukuoka 819-0395, Japan
* Correspondence: rauful.karim@gmail.com

Abstract: The electrical performance of the back-channel etched Indium–Gallium–Zinc–Oxide (IGZO) thin-film transistors (TFTs) with copper (Cu) source and drain (S/D) which are patterned by a selective etchant was investigated. The Cu S/D were fabricated on a molybdenum (Mo) layer to prevent the Cu diffusion to the active layer (IGZO). We deposited the Cu layer using thermal evaporation and performed the selective wet etching of Cu using a non-acidic special etchant without damaging the IGZO active layer. We fabricated the IGZO TFTs and compared the performance in terms of linear and saturation region mobility, threshold voltage and ON current (I_{ON}). The IGZO TFTs with Mo/Cu S/D exhibit good electrical properties, as the linear region mobility is 12.3 cm^2/V-s, saturation region mobility is 11 cm^2/V-s, threshold voltage is 1.2 V and I_{ON} is 3.16 $\times$ 10^{-6} A. We patterned all the layers by a photolithography process. Finally, we introduced a SiO_2-ESL layer to protect the device from external influence. The results show that the prevention of Cu and the introduced ESL layer enhances the electrical properties of IGZO TFTs.

Keywords: IGZO TFTs; Cu thermal diffusion; selective etching of Cu; barrier layer; DC sputtering

check for updates

Citation: Khan, R.; Misran, M.A.B.; Ohtaki, M.; Song, J.T.; Ishihara, T.; Hattori, R. Back-Channel Etched In-Ga-Zn-O Thin-Film Transistor Utilizing Selective Wet-Etching of Copper Source and Drain. *Processes* **2021**, *9*, 2193. https://doi.org/10.3390/pr9122193

Academic Editors: Arash Afshar and Prashant K. Sarswat

Received: 27 September 2021
Accepted: 2 December 2021
Published: 6 December 2021

Publisher's Note: MDPI stays neutral with regard to jurisdictional claims in published maps and institutional affiliations.

Copyright: © 2021 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https://creativecommons.org/licenses/by/4.0/).

1. Introduction

Currently, Indium–Gallium–Zinc-Oxide (IGZO) thin-film transistors (TFTs) have received considerable research attention as active-matrix backplanes for the next generation of display technology [1–3]. Recently, IGZO TFTs are used as a switching device in flat panel displays, such as active-matrix organic light-emitting diode (AMOLED) displays, active-matrix liquid crystal displays (AMOLCD) and electrophoretic displays [4,5]. Most of the studies are focused on the electrical, electronic, optical and thermal properties of IGZO thin films [6,7]. There are also several studies to improve these parameters for the transistors by using Dirac materials, with the tunneling and trapping effects as the main approach [8,9]. As they increase the resolution (≥8 K), display size (≥110 inch) and high frame rate (≥480 Hz) for the flat panel display, the low-resistance metals are highly necessary for the source (S) and drain (D) electrodes of IGZO TFTs to reduce resistance-capacitance (RC) delay of the display panel to avoid image distortion and shading [10–12]. However, several reports have been revealed that the diffusion of Cu into IGZO deteriorates the electrical performance, as it acts as acceptor-like trap states of IGZO TFT [13–17]. Recently, a low resistance stacked structure of S/D on IGZO was introduced to enhance the contact properties [18–20]. Ti and Mo have been used widely as an interfacial layer to protect the Cu diffusion into IGZO and to reduce the impact of the Schottky barrier. The work function

of Mo and Ti is 4.7 eV and 4.3 eV, respectively, which are very close to that of IGZO (4.5 eV). In this aspect, it is very difficult to pattern the Cu selectively with Cu etchant without damaging the active layer. Most of the studies are focused on the TFT-device fabrication process using shadow mask to avoid the wet process fabrication [20], but it is not possible to maintain the fine frame size that is very necessary for large panel display. The dry process helps to prevent the damage of the active layer. To achieve the fine frame size of S/D, the photolithography process is a very suitable process for device fabrication.

In this study, we fabricated IGZO TFT with Cu and Cu/Mo S/D using a photo lithography process. We investigated the electrical performance of IGZO TFTs with Mo/Cu S/D electrodes and a passivation SiO_2 layer. We selectively wet etched the Cu with non-acidic special Cu etchant using a wet process, as the dry etching process cannot etch the patterned Cu layer. Two test samples were fabricated and the transfer characteristics and mobility according to gate voltage (V_g) were measured to compare their performance. We performed the scanning electron microscopy (SEM) and energy dispersive X-ray analysis (EDX) for structural and materials analysis.

2. Experimental Details

Figure 1 shows the process flow of the samples used in this report. An inverted staggered bottom-gate IGZO were prepared on a glass substrate. First, the gate electrode with Al-Nd (85 nm)/Mo (15 nm) was deposited on a glass substrate by DC magnetron sputtering. Al-Nd alloy was deposited to avoid the electro migration and Mo was used as a barrier layer. The gate electrode was patterned using the photolithography process and wet etching. Subsequently, a gate insulator (GI) of 150-nm thick SiO_2 was formed using plasma-enhanced chemical vapor deposition (PECVD). Then, a 15-nm IGZO thin film as an active layer was deposited by DC magnetron sputtering in a gas mixture of Ar and Ar-O_2 (90–10%) at 150 °C, from the ceramic target atomic ratio In:Ga:Zn = 1:1:1. The deposition chamber pressure was evacuated less than 1×10^5 Pa and the working pressure was 1 Pa. Next, the active layer and GI layer was patterned. The oxygen partial pressure was calculated as [P (O_2) = O_2/(Ar + O_2)] and fixed at 1%. A 40 nm of 99.999% pure Cu interlayer was deposited on patterned active layer for Sample A. Stacked films of 20 nm Mo and 40 nm Cu were deposited for sample B using thermal evaporation and patterned again the S/D contact for all samples. A thinner Cu layer was deposited to reduce contact resistance, but it is possible to deposit a thicker one. The special Cu etchant etched the Cu layer only, not the IGZO active layer. S/D were patterned by a photo mask and photolithography process. Active channel width and length were 10 μm and 20 μm, respectively. Finally, a 200 nm SiO_2 passivation layer was deposited for both devices with a working pressure at 110 Pa at 200 °C by chemical vapor deposition (CVD) process. Furuta et al. reported that certain amounts of H_2 may be diffused into the IGZO active layer from the passivation layer, which can act as a shallow donor in IGZO films [21]. This passivation layer also protects the device from external influence. The SiO_2 passivation layer was deposited at the partial pressure of SiH_4 of P[SiH_4] = 1.36% using N_2, SiH_4 and N_2O gases. This passivation layer was also patterned by a photolithography process to make the contact. Ultimately, all the devices were annealed at 350 °C at N_2 environment for 1 h. The cross-sectional views of the TFT for Samples A and B are shown in Figure 2a,b, respectively, and the plane view is illustrated in Figure 2c. For the SEM and EDX analysis, 500 nm IGZO was deposited on the glass substrate. For the Cu diffusion analysis, 500 nm Cu was deposited on IGZO using a thermal evaporation process and evaluated before and after the annealing effect. To observe the effect of the barrier layer, 500 nm of Cu and Mo film was deposited on the IGZO thin film using thermal evaporation and DC sputtering process, and the before and after annealing effect was analyzed.

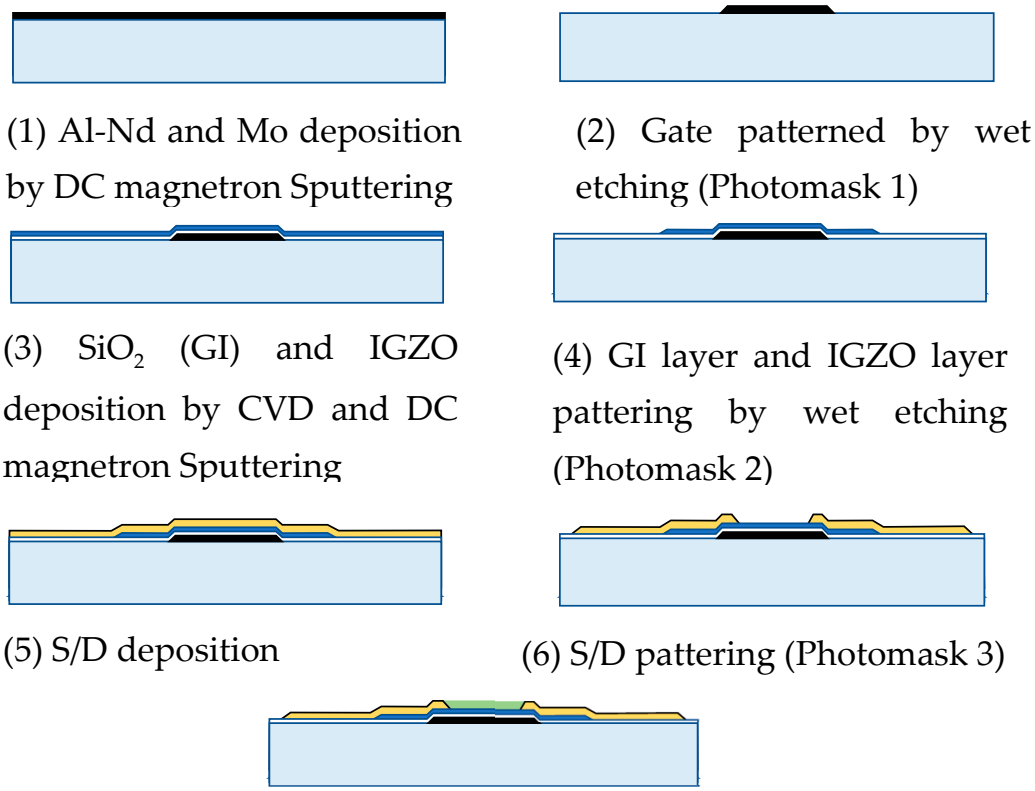


Figure 1. Process flow of bottom gate top contact IGZO TFTs.

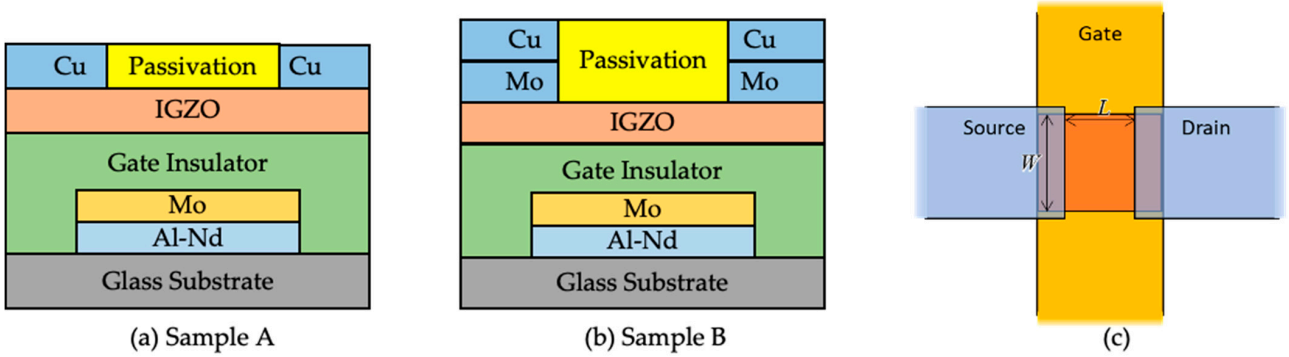


Figure 2. Schematic cross-section of the IGZO TFT on a glass substrate with a bottom-gate top-contact structure. (**a**) Sample A, (**b**) Sample B, and (**c**) top view of the IGZO TFTs.

3. Results

The active layer defines the channel width, and the separation of S/D electrodes defines the channel length. In this design, we can define the channel width correctly by the active layer width, but the edge of the active layer has a chance to be damaged by the etching. As shown later, we have problems with *SS* value and leakage current even after improving the mobility value. Therefore, there is still plenty of room for improvement in the design of the TFT layout. Figure 3a,b shows the microscopic image of IGZO TFTs samples with no defects after using Cu etchant.

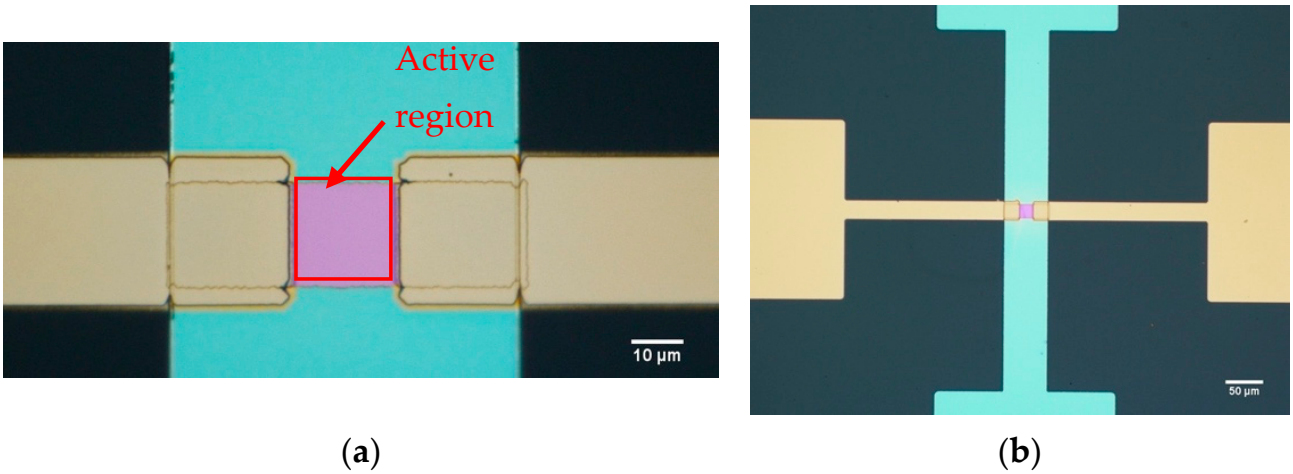


Figure 3. (**a**,**b**) Microscopic image of bottom gate top contact IGZO TFTs after using the special Cu etchant at different magnification.

Ferric chloride ($FeCl_3$), Cupric Chloride ($CuCl_2$), Hydrogen peroxide—Sulphuric acid (H_2O_2-H_2SO_4), Chromic—Sulphuric acid (CrO_3-H_2SO_4), ammonium persulphate $(NH_4)_2SO_4$) and Citric acid are widely used as a Cu etchant; however, all of them contain strong acids, such as HCL and H_2SO_4 [22–24]. All the etchants have a high-etched rate, high-Cu dissolving capacity and are very acidic [25]. For this reason, those acidic Cu etchants can damage the IGZO layer and device structure easily and affect the device performance. As a result, most researchers use shadow mask to deposit S/D to avoid wet Cu etchant [20,26–28]. TFTs characteristics are usually presumed from the transfer characteristics, where the drain to source current (I_d) is plotted against gate to source voltage (V_g) for various drain to source voltage (V_d) and from output characteristics, where I_d is plotted against drain to source voltage (V_d) for various gate to source voltage (V_g), as shown in Figure 4. The parameters of the output characteristics and the transfer characteristics of sample A and B are as follows; the gate voltage (V_g) was 0 V, 5 V and 10 V and drain voltage was 0.1 V, 5 V and 10 V, respectively. At the value of drain voltage (V_d) at 1 V, the threshold voltage (V_{th}) represents the gate voltage (V_g) corresponding to the drain current (I_d) of 1×10^{-9} A. The electrical characteristics of device performance are extracted by analyzing several parameters, such as saturation region mobility (μ_{SAT}), field-effect mobility (μ_{FE}), threshold voltage (V_{th}), On-Current (I_{ON}) and subthreshold swing (SS). The field-effect mobility is evaluated based on gradual channel approximation and the equation is as follows,

$$I_d = \frac{W}{L}\,\mu C_i \left[\left(V_g - V_{th}\right) V_d - \frac{V_d^2}{2} \right] \quad (1)$$

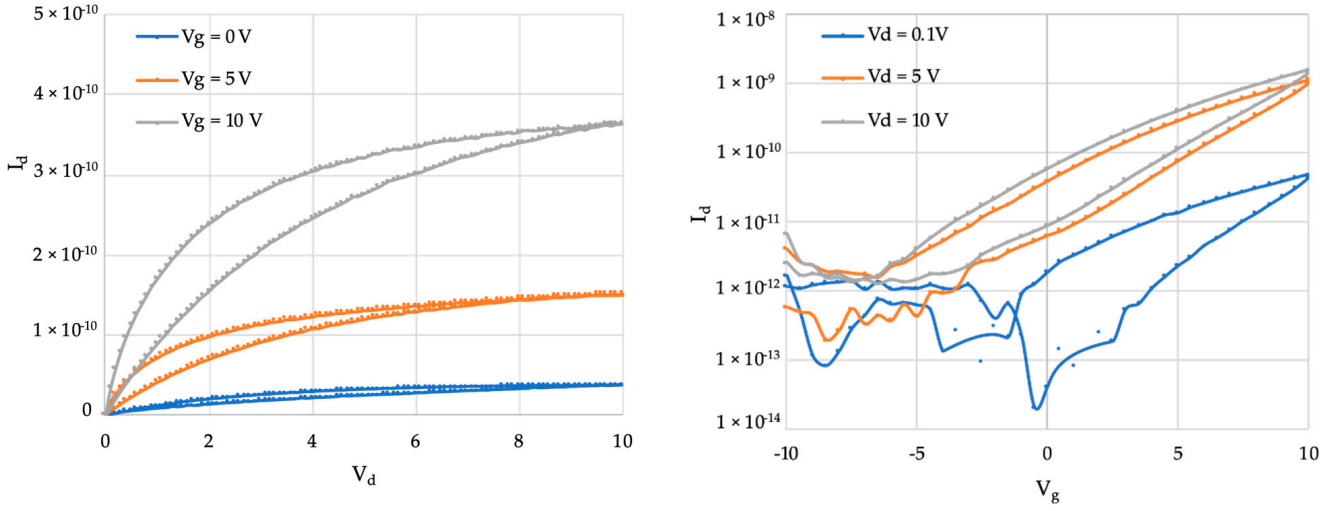
Here, μ is the channel carrier mobility, W and L are channel width and length, and C_i is the gate capacitance per unit area of the insulator layer. Furthermore, the saturation

region mobility was obtained from the curve of the square root of the drain current versus the V_g in saturation operation region:

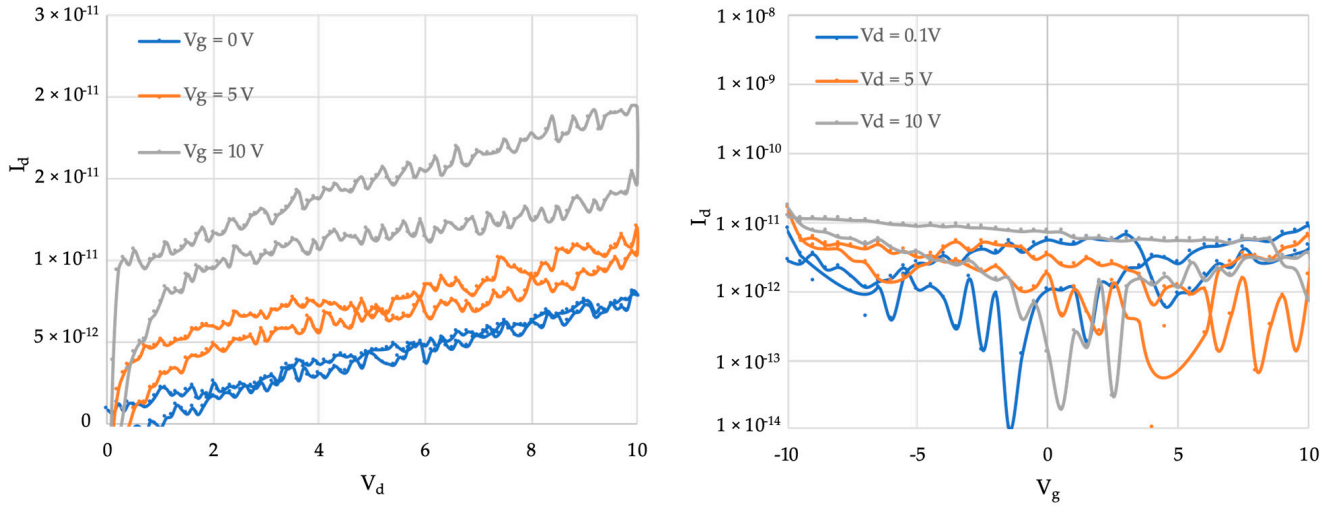
$$\sqrt{I_d} = \left(\frac{WC_i\mu_{SAT}}{2L}\right)^{1/2}(V_g - V_{th}) \quad (2)$$

Another important parameter subthreshold swing (SS) reflects the change of V_g instead of increase I_d; is determined by,

$$SS = \frac{dV_g}{dlog_{10}(I_d)} \quad (3)$$



(**a**)



(**b**)

Figure 4. Output (left side) and transfer characteristics (right side) of sample A (**a**) Pre-annealing and (**b**) post-annealing.

Figure 4 represents the output and transfer characteristics of sample A. The electrical characteristics of Figure 4a are better compared to Figure 4b, though the mobility is tiny and threshold voltage is quite high. Figure 4a is the electrical properties of sample A, which are calculated before annealing the sample. Moreover, the electrical characteristics

of sample A are becoming worst after post-annealing. The reason might be described by the diffusion of Cu into the IGZO layer for post annealing after the deposition of the Cu S/D contact or for depositing Cu onto the channel layer directly. Figure 4a has been extracted before annealing. Therefore, it has less chance of Cu diffusion into IGZO layer. Sample B has a 15-nm-thick Mo layer at the S/D contact, which makes ohmic contacts after annealing and prevents the diffusion of Cu into the IGZO layer. Figure 5 shows the output and transfer characteristics of sample B after post-annealing. The sample B for W/L of 10/20 (μm/μm) achieves improved performance as follows: V_{th} of 1.2 V, μ_{SAT} of 11 cm^2/V-s, and I_{ON} of 3.16 × 10^{-6} A. This experimental data assured that the non-acidic selective Cu etchant has no effect on IGZO layer. The hysteresis has completely minimized from the output characteristics, but still there is hysteresis at the transfer characteristics. The SS value becomes high because the density of the acceptor-like trap states of IGZO is also increased. Hu et al. reported the field effect mobility around 11.5 cm^2/V-s with ITO barrier layer [27]. On the other hand, Kim et al. also reported the field effect mobility around 12.8 cm^2/V-s with Mo-Ti/Cu S/D [28]. These results are quite similar to our experimental results. Figure 6 shows the negative bias temperature stress at the drain voltage of 10.1 V. The transfer characteristics are shifted left from the threshold voltage of 1.2 V to 0.4 V, which improve the TFT characteristics. The H_2 atom from the passivation layer may have been diffused into the IGZO layer due to of annealing, which can enhance the electrical properties. The IGZO TFT without a passivation layer does not exhibit remarkable electronic properties because it may be affected by external influence (see the Supplementary File, Figure S1). Table 1 exhibits the details analysis between sample A and B after post-annealing. The electrical performance of the TFTs is summarized in Table 1.

Figure 7 shows the SEM image of the sample A and B. In Figure 7a, the Cu layer and the IGZO thin film is completely separated from each other. From the mapping analysis and EDX layered analysis, the image also shows the clear demonstration of each layer (see the Supplementary File, Figure S2). The spectrum analysis of sample A before post annealing shows the individual peak intensity of Cu, In, Ga and Zn (See the Supplementary File, Figure S3). However, after post annealing the Cu was diffused into the IGZO layer. For this reason, the thickness of Cu layer was decreased. The mapping analysis of EDX layered analysis also reveals the clear demonstration of Cu diffusion (red dots) (See the Supplementary File, Figure S4). The spectrum analysis of sample A after post annealing also shows the Cu peaks into the IGZO active layer. It clearly shows that Cu is diffusing into the IGZO layer after post annealing, which deteriorated the electrical properties of IGZO TFTs. It also shows the peak intensity of Cu, In, Ga and Zn (See the Ssupplementary File, Figure S5) into the IGZO layer. The IGZO region near the IGZO-CU interfacial layer contains a large amount of Cu, but this decreased at the deeper region of IGZO. Before post annealing of sample B (Figure 7c), the stacked layer of Mo/Cu and the IGZO layer has been seen clearly. After post annealing (Figure 7d), the Mo layer is clearly seen in between Cu and IGZO layer. Here the Mo layer is acting as a barrier layer to prevent the Cu diffusion. The EDX-layered analysis of sample B before annealing shows the separate color dot of each material that confirms that there is no Cu diffusion of Cu into IGZO layer before post annealing (See the Supplementary File, Figure S6). On the other hand, Figure 7c clearly shows that the Cu cannot diffused into IGZO after post annealing. The stack layer of Mo can prevent the Cu diffusion. The EDX layered analysis and spectrum analysis of Sample B after post annealing also shows the clear representation of each layer. There are no peaks of Cu into the IGZO layer in the spectrum analysis, which clearly determines that in the Mo/Cu S/D IGZO TFTs, the Cu cannot diffuse into IGZO due to the Mo barrier layer (See the Supplementary File, Figure S7). This phenomenon also supports the enhancement the electrical characteristics.

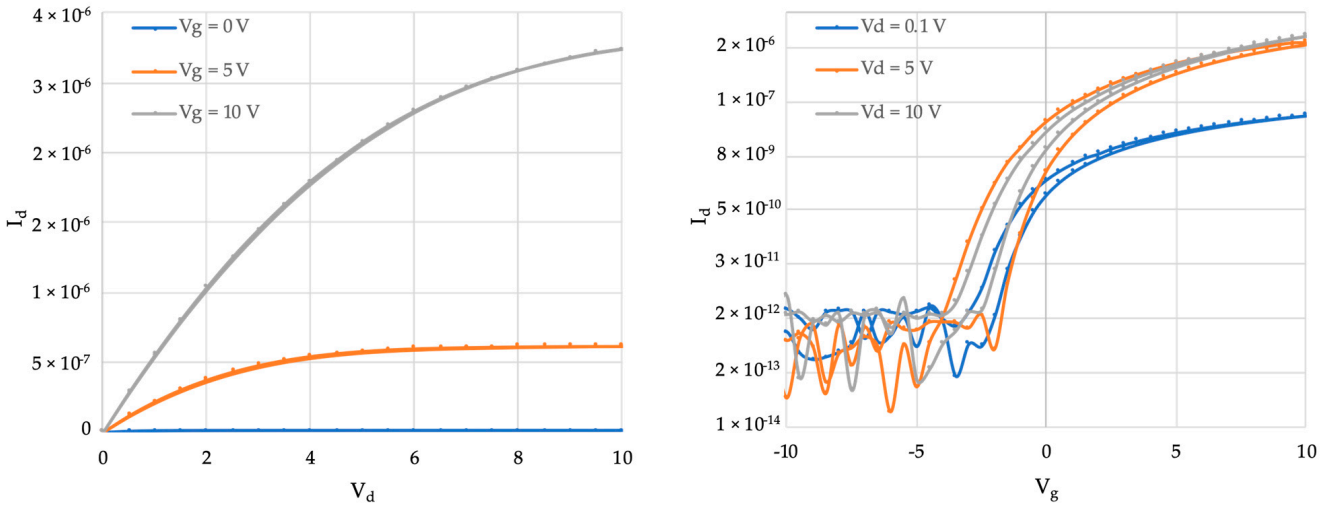


Figure 5. Output (**left side**) and transfer characteristics (**right side**) of sample B after annealing.

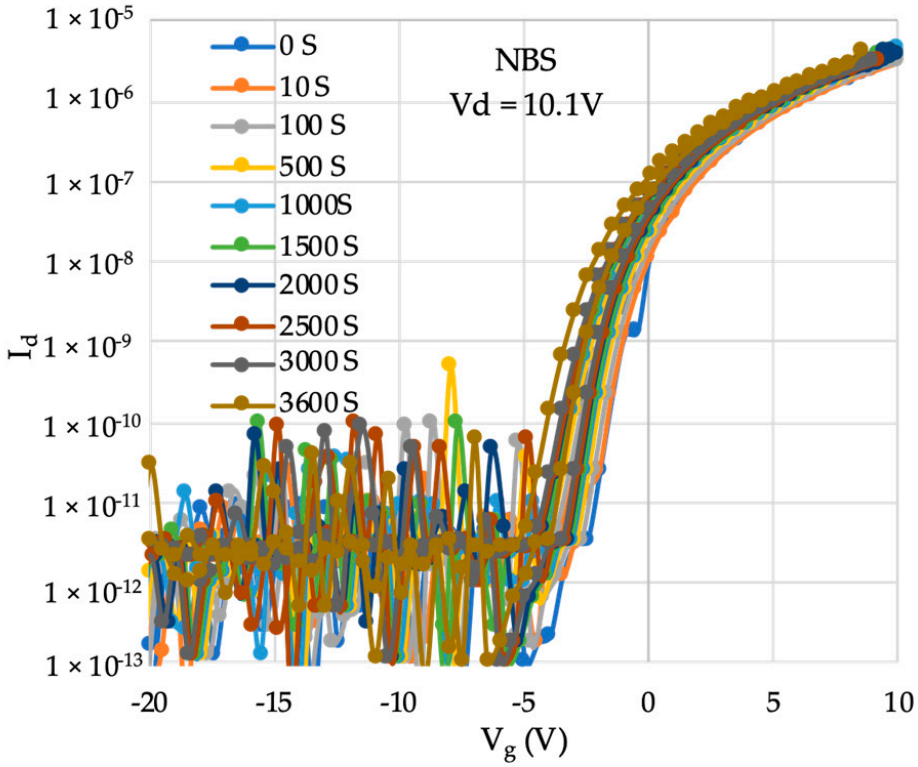


Figure 6. Changes in transfer characteristics under negative-bias temperature stress at the range of gate voltage from −20 V to 10 V.

Table 1. The electrical properties of IGZO TFTs.

S/D	μ_{FE} (cm^2/V-s)	μ_{SAT} (cm^2/V-s)	V_{th} (V)	I_{ON} (A)	*SS* (V/Decade)	Annealing Condition
Cu	9.2×10^{-5}	1.8×10^{-5}	5	1.6×10^{-9}	-	Before Post-annealing
Mo/Cu	12.3	11	1.2	3.2×10^{-6}	0.58	After Post-annealing

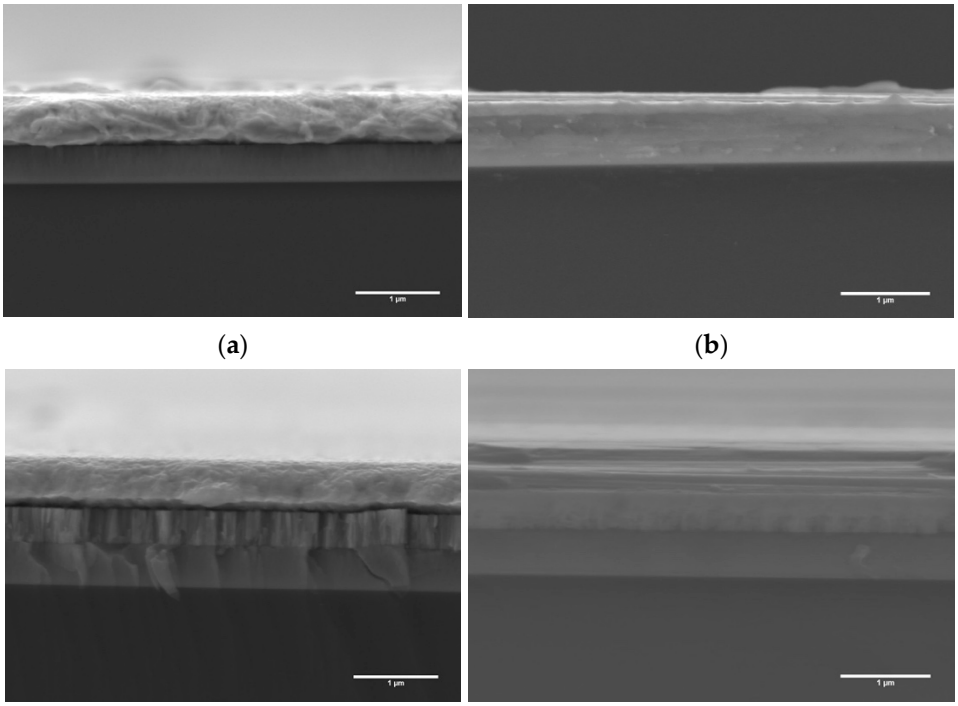


Figure 7. Scanning electron microscopy image of sample A (**a**) before post-annealing, (**b**) after post annealing, and sample B (**c**) before post-annealing, (**d**) after post annealing.

4. Conclusions

In summary, we have successfully fabricated a high mobility IGZO TFT with Mo-Cu S/D contact using a special non-acidic Cu etchant, which can etch Cu properly and avoid the damage to IGZO layer. The electrical properties of IGZO TFTs with Mo/Cu S/D ensure the selectivity of Cu etchant. Post-annealing treatment formed and improved the TFT characteristics, and the Mo interlayer prevented the Cu diffusion into active layer. The SEM image analysis clearly shows evidence of the prevention of Cu diffusion with the Mo layer. The mapping and spectrum analysis also clarify the diffusion mechanism. Thus, the TFT with Mo-Cu S/D exhibited proper switching characteristics with saturation mobility at 11 cm^2/V-s. The results suggested an effective fabrication method for fabricating high-mobility metal oxide TFT based on Cu S/D.

Supplementary Materials: The following are available online at https://www.mdpi.com/article/10.3390/pr9122193/s1, Figure S1: Output and transfer characteristics of IGZO TFT without passivation layer after annealing in N2 atmosphere for 1 hour. Figure S2: Mapping analysis of sample A before post annealing. Figure S3: Spectrum analysis of sample A before post annealing. Figure S4: Mapping analysis of sample A after post annealing. Figure S5: Spectrum analysis of sample A after post annealing. Figure S6: The EDX layered analysis of Sample B before post annealing. Figure S7: The EDX layered analysis and spectrum analysis of Sample B after post annealing.

Author Contributions: Conceptualization, R.K. and R.H.; methodology, R.K. and R.H.; software, R.K.; validation, formal analysis, R.K., M.A.B.M., M.O., J.T.S., T.I. and R.H.; investigation, R.K., M.A.B.M. and J.T.S.; resources, R.K. and R.H.; data curation, R.K. and M.A.B.M.; writing—original draft preparation, R.K.; writing—review and editing, R.H.; supervision, R.H. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: The data that support the findings of this study are available from the corresponding author upon reasonable request.

Acknowledgments: The support from Kyushu University and the Ministry of Education, Culture, Sports, Science, and Technology (MEXT), Japan, is highly appreciated.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Nomura, K.; Takagi, A.; Kamiya, T.; Ohta, H.; Hirano, M.; Hosono, H. Amorphous oxide semiconductors for high-performance flexible thin-film transistors. *Jpn. J. Appl. Phys.* **2006**, *45*, 4303. [CrossRef]
2. Nomura, K.; Ohta, H.; Takagi, A.; Kamiya, T.; Hirano, M.; Hosono, H. Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors. *Nature* **2004**, *432*, 488–492. [CrossRef]
3. Nomura, K.; Ohta, H.; Ueda, K.; Kamiya, T.; Hirano, M.; Hosono, H. Thin-film transistor fabricated in single-crystalline transparent oxide semiconductor. *Science* **2003**, *300*, 1269–1272. [CrossRef]
4. Park, J.S.; Maeng, W.J.; Kim, H.S.; Park, J.S. Review of recent developments in amorphous oxide semiconductor thin-film transistor devices. *Thin Solid Film.* **2012**, *520*, 1679–1693. [CrossRef]
5. Martins, J.; Bahubalindruni, P.; Rovisco, A.; Kiazadeh, A.; Martins, R.; Fortunato, E.; Barquinha, P. Bias stress and temperature impact on InGaZnO TFTs and circuits. *Materials* **2017**, *10*, 680. [CrossRef]
6. Fujimoto, Y.; Uenuma, M.; Ishikawa, Y.; Uraoka, Y. Analysis of thermoelectric properties of amorphous InGaZnO thin film by controlling carrier concentration. *AIP Adv.* **2015**, *5*, 097209. [CrossRef]
7. Khan, R.; Ohtaki, M.; Hata, S.; Miyazaki, K.; Hattori, R. Thermal conductivity of nano-crystallized indium-gallium-zinc oxide thin films determined by differential three-omega method. *Nanomaterials* **2021**, *11*, 1547. [CrossRef] [PubMed]
8. Sarswat, P.K.; Sarkar, S.; Yi, G.; Free, M.L. Phosphorus-doped SnTe-type needle-like crystals: Band structure modifications and electronic properties. *J. Phys. Chem. C* **2017**, *121*, 18263–18273. [CrossRef]
9. Oh, T. Analysis of surface current by quantum tunneling effect of thin film transistors with topological insulators. *Sci. Rep.* **2020**, *10*, 9509. [CrossRef]
10. Lee, S.H.; Oh, D.J.; Hwang, A.Y.; Han, D.S.; Kim, S.; Jeong, J.K.; Park, J.W. Improvement in device performance of a-InGaZnO transistors by introduction of Ca-doped Cu source/drain electrode. *IEEE Electron Device Lett.* **2015**, *36*, 802–804. [CrossRef]
11. Zhao, M.; Xu, M.; Ning, H.; Xu, R.; Zou, J.; Tao, H.; Wang, L.; Peng, J. Method for fabricating amorphous indium-zinc-oxide thin-film transistors with copper source and drain electrodes. *IEEE Electron Device Lett.* **2015**, *36*, 342–344. [CrossRef]
12. Arai, T. Oxide-TFT technologies for next-generation AMOLED displays. *J. Soc. Inf. Disp.* **2012**, *20*, 156–161. [CrossRef]
13. Kim, W.-S.; Moon, Y.-K.; Kim, K.-T.; Lee, J.-H.; Ahn, B.-D.; Park, J.-W. An investigation of contact resistance between metal electrodes and amorphous gallium-indium-zinc oxide (a-GIZO) thin-film transistors. *Thin Solid Film.* **2010**, *518*, 6357–6360. [CrossRef]
14. Yim, J.R.; Jung, S.Y.; Yeon, H.W.; Kwon, J.Y.; Lee, Y.J.; Lee, J.H.; Joo, Y.C. Effects of metal electrode on the electrical performance of amorphous In-Ga-Zn-O thin film transistor. *Jpn. J. Appl. Phys.* **2012**, *51*, 011401. [CrossRef]
15. Hu, S.; Fang, Z.; Ning, H.; Tao, R.; Liu, X.; Zeng, Y.; Yao, R.; Huang, F.; Li, Z.; Xu, M.; et al. Effect of post treatment for cu-cr source/drain electrodes on a-igzo tfts. *Materials* **2016**, *9*, 623. [CrossRef]
16. Youn, C.S.; Lee, D.G. Effects of post heat treatment on the mechanical properties of cold-rolled Ti/Cu clad sheet. *Metals* **2020**, *10*, 1672. [CrossRef]
17. Fisher, I.; Eizenberg, M. Copper ion diffusion in porous and nonporous SiO_2-based dielectrics using bias thermal stress and thermal stress tests. *Thin Solid Film.* **2008**, *516*, 4111–4121. [CrossRef]
18. Choi, K.-H.; Kim, H.-K. Correlation between Ti source/drain contact and performance of InGaZnO-based thin film transistors. *Appl. Phys. Lett.* **2013**, *102*, 052103. [CrossRef]
19. Lan, L.; Xu, M.; Peng, J.; Xu, H.; Li, M.; Luo, D.; Zou, J.; Tao, H.; Wang, L.; Yao, R. Influence of source and drain contacts on the properties of the indium-zinc oxide thin-film transistors based on anodic aluminum oxide gate dielectrics. *J. Appl. Phys.* **2011**, *110*, 103703. [CrossRef]
20. Hu, S.; Ning, H.; Lu, K.; Fang, Z.; Li, Y.; Yao, R.; Xu, M.; Wang, L.; Peng, J.; Lu, X. Mobility enhancement in amorphous in-Ga-Zn-O thin-film transistor by induced metallic in nanoparticles and Cu electrodes. *Nanomaterials* **2018**, *8*, 197. [CrossRef]
21. Toda, T.; Wang, D.; Jiang, J.; Hung, M.P.; Furuta, M. Quantitative analysis of the effect of hydrogen diffusion from silicon oxide etch-stopper layer into amorphous In-Ga-Zn-O on thin-film transistor. *IEEE Trans. Electron Devices* **2014**, *61*, 3762–3767. [CrossRef]
22. Çakır, O. Review of etchants for copper and its alloys in wet etching processes. *Key Eng. Mater.* **2007**, *364*, 460–465. [CrossRef]
23. Williams, K.R.; Gupta, K.; Wasilik, M. Etch rates for micromachining processing—Part II. *J. Microelectromech. Syst.* **2003**, *12*, 761–778. [CrossRef]
24. Georgiadou, M.; Alkire, R. Anisotropic chemical etching of copper foil: II. experimental studies on shape evolution. *J. Electrochem. Soc.* **1993**, *140*, 1348–1355. [CrossRef]
25. Noma, H.; Nakanishi, T. Etching process analysis based on etchant flow for high-density build-up substrate. In Proceedings of the 6th Electronics Packaging Technology Conference, EPTC 2004, Singapore, 8–10 December 2004. [CrossRef]

26. Hu, S.; Ning, H.; Lu, K.; Fang, Z.; Tao, R.; Yao, R.; Zou, J.; Xu, M.; Wang, L.; Peng, J. Effect of Al_2O_3 passivation layer and Cu electrodes on high mobility of amorphous IZO TFT. *IEEE J. Electron Devices Soc.* **2018**, *6*, 733–737. [CrossRef]
27. Hu, S.; Lu, K.; Ning, H.; Fang, Z.; Liu, X.; Xie, W.; Yao, R.; Zou, J.; Xu, M.; Peng, J. Effect of ITO serving as a barrier layer for Cu electrodes on performance of a-IGZO TFT. *IEEE Electron Device Lett.* **2018**, *39*, 504–507. [CrossRef]
28. Kim, L.Y.; Kwon, O.K. Effects of stacked Mo-Ti/Cu source and drain electrodes on the performance of amorphous In-Ga-Zn-O thin-film transistors. *IEEE Electron Device Lett.* **2018**, *39*, 43–46. [CrossRef]