energies

MDPI

Article

Enhancing the Filtering Capability and the Dynamic Performance of a Third-Order Phase-Locked Loop under Distorted Grid Conditions

Issam A. Smadi [1,*], Hanady A. Kreashan [1] and Ibrahem E. Atawi [2]

[1] The Department of Electrical Engineering, Jordan University of Science and Technology, P.O. Box 3030, Irbid 22110, Jordan
[2] The Department of Electrical Engineering, Faculty of Engineering, University of Tabuk, P.O. Box 741, Tabuk 47512, Saudi Arabia
* Correspondence: iasmadi@just.edu.jo

Abstract: This work proposes a structural enhancement and a new technique to design the loop filter (LF) of a third-order phase-locked loop (PLL) to enhance the PLL dynamic performance under abnormal grid conditions. The proposed PLL combines a moving average filter (MAF) and an arbitrarily delayed signal cancelation (ADSC) for structural enhancement to achieve DC-offset rejection and harmonics elimination. The window length of the MAF is selected to be one-sixth of the fundamental grid period to remove non-triple odd harmonics and speed up the PLL dynamic response. The triple harmonics are eliminated, adopting the line-to-line voltage concept, while the ADSC operator rejects the DC offset. The LF design is based on a modified third-order polynomial tuned using stochastic optimization to minimize the settling time of the frequency deviation, offering better dynamic performance over the symmetrical optimum method (SOM) and achieving synchronization within one grid cycle. The PLL mathematical model, small-signal model, and LF design based on the modified polynomial are discussed. Finally, the proposed PLL performance is verified numerically and experimentally with comparisons with other PLLs to demonstrate the effectiveness of the proposed work.

Keywords: arbitrarily delayed signal cancelation; moving average filter; phase-locked loop; loop filter; stochastic optimization; controller tuning

Citation: Smadi, I.A.; Kreashan, H.A.; Atawi, I.E. Enhancing the Filtering Capability and the Dynamic Performance of a Third-Order Phase-Locked Loop under Distorted Grid Conditions. *Energies* **2023**, *16*, 1472. https://doi.org/10.3390/en16031472

Academic Editors: Isabel Jesus and Ramiro Barbosa

Received: 22 December 2022
Revised: 22 January 2023
Accepted: 24 January 2023
Published: 2 February 2023

1. Introduction

The feasible control of the grid-connected converters is of prime importance when renewable energy sources are connected to the grid. Therefore, grid synchronization is of interest due to more and more renewable energy sources tied up to the grid using power electronic converters in recent years [1].

The phase-locked loop (PLL) is a technique that can effectively synchronize the phase, frequency, and amplitude of the grid-connected inverters with the grid [2,3]. By maintaining synchronization, PLL helps to ensure that the renewable energy source can be safely and efficiently integrated into the grid. Additionally, PLLs can also be used to optimize the power output of the renewable energy source, further increasing its efficiency [4]. Conventional PLLs work effectively in ideal conditions. However, PLLs face significant challenges in estimating the phase and frequency under abnormal conditions [5–10]. PLLs should keep up the synchronization process in the presence of disturbances such as DC offset, phase jump, frequency jump, and the harmonics and return to the steady state within two grid cycles [11]. Therefore, a robust and accurate PLL with high filtering capability to achieve grid synchronization has attracted much attention in the literature [12–17]. In addition, the PLL loop filter is responsible for both the system static noise and dynamic performance to be set while considering the constraints imposed by the other system

elements [18]. Hence, properly tuning the parameters of the loop filter (LF), including the proportional-integral (PI) controller's parameters, is one of the most important issues in the PLL design [19]. There are many methods to design the PLL's LF based on its small-signal model. If the system is third-order, one of the most used methods to design the LF is the symmetrical optimum method (SOM) [20–22], whereas if the system is a second-order system, the damping factor and natural frequency of a standard second-order system are used to design the gains [7,23,24]. An adaptive feedforward mechanism can adjust the filter gains according to the estimated grid frequency [25]. In general, the value of the gains is selected targeting a 2% criteria settling time. All the papers above rely on the small-signal model of the PLL to design the LF gains, giving a local nature to the solution. In contrast, the LF gains are designed in this paper based on the actual PLL model without approximations using stochastic optimization.

On the other hand, the filtering capability of DC offset and harmonics are associated with the MAF window length that can be used as a prefilter or as an in-loop filter [24,26]. The DC offset and harmonics are rejected if the window length is the same as the fundamental grid period, but this will add a delay. In [13], the MAF is used as a prefilter in the $\alpha\beta$-reference frame; this speeds up the response because no delay is introduced in the loop. However, under off-nominal frequencies, a phase shift is introduced; hence, a phase error correction must be created, increasing the system's complexity. Another choice of window length is half of the nominal period. In general, when the window length decreases, the speed of the response increases, affecting the filtering capability such that the DC offset cannot be rejected.

A quasi-type1 (QT1) PLL uses the MAF as an internal filter, although utilizing the filter inside the control loop decreases the response speed. The response can be enhanced by utilizing a P-controller with a feedforward term [14]. However, the performance of this PLL degrades under frequency drift with the presence of harmonics and takes more than two grid cycles to settle down. Another approach in [15], similar to [14], adopts the same window length for the MAF to remove the impact of the odd harmonics and uses $\alpha\beta$ delayed signal cancellation (DSC) with a fixed time delay to remove the effect of the DC offset and the even harmonics. Under frequency deviation, a phase shift is created; hence, phase error correction is needed. A combination of MAF and DSC in the paralleled filter (PF) is suggested in [16]. The MAF extracts the fundamental frequency negative sequence (FFNS) at 100 Hz and the fundamental frequency positive sequence (FFPS) at 0 Hz, while the modified DSC (MDSC) extracts the FFNS only. Thus, the PF benefit passes the FFNS through MAF and MDSC with a reversed phase. Finally, the FFNS can be removed by an arithmetic operation. The MAF can remove the other harmonics, where the window length equals one-sixth of the nominal period, speeding the response speed more than the previous techniques. However, this PLL suffers from oscillation in the estimated grid information under frequency drift; it also has no dc offset rejection capability.

This paper proposes a new approach to design the loop filter (LF) of a third-order phase-locked loop (PLL), offering contributions in terms of the structural improvement of the three-phase PLL and a method for the optimal loop filter design. Without loss of generality, the proposed PLL combines an MAF with an arbitrarily delayed signal cancellation (ADSC) for structural enhancement to achieve DC-offset rejection and harmonics elimination. The window length of the MAF is selected to be one-sixth of the fundamental grid period to remove non-triple odd harmonics and accelerate the PLL response. The triple harmonics are eliminated, adopting the line-to-line voltage concept, while the ADSC operator rejects the effect of the DC offset. Moreover, different optimization methods are adopted to design the gains of the LF targeting the 2% criterion settling time in grid frequency deviation. The effectiveness of the proposed PLL and the adopted loop filter design method is verified by comparing their performance with other related PLLs and verifying the offered improvements numerically and experimentally.

2. The Proposed Method

2.1. PLL Structure Enhancement

PLL structure improvement includes the phase-to-line voltage transformation to block the triple harmonics. The ADSC, which is not restricted to a specific time delay, blocks the DC offset and the MAF with a window length of one-sixth of the fundamental grid period to block the non-triple odd harmonics.

The schematic diagram of the proposed PLL is shown in Figure 1, where $v_{a\varphi}$, $v_{b\varphi}$, and $v_{c\varphi}$ are the phase voltages; v_{ab}, v_{bc}, and v_{ca} are the line voltages; ω_n is the nominal angular frequency; k_φ is the phase error correction; $\Delta\hat{\omega}_g$ is the deviation in the estimated grid frequency; $\hat{\theta}$ is the estimated phase angle; $\hat{\omega}_g$ is the estimated grid frequency.

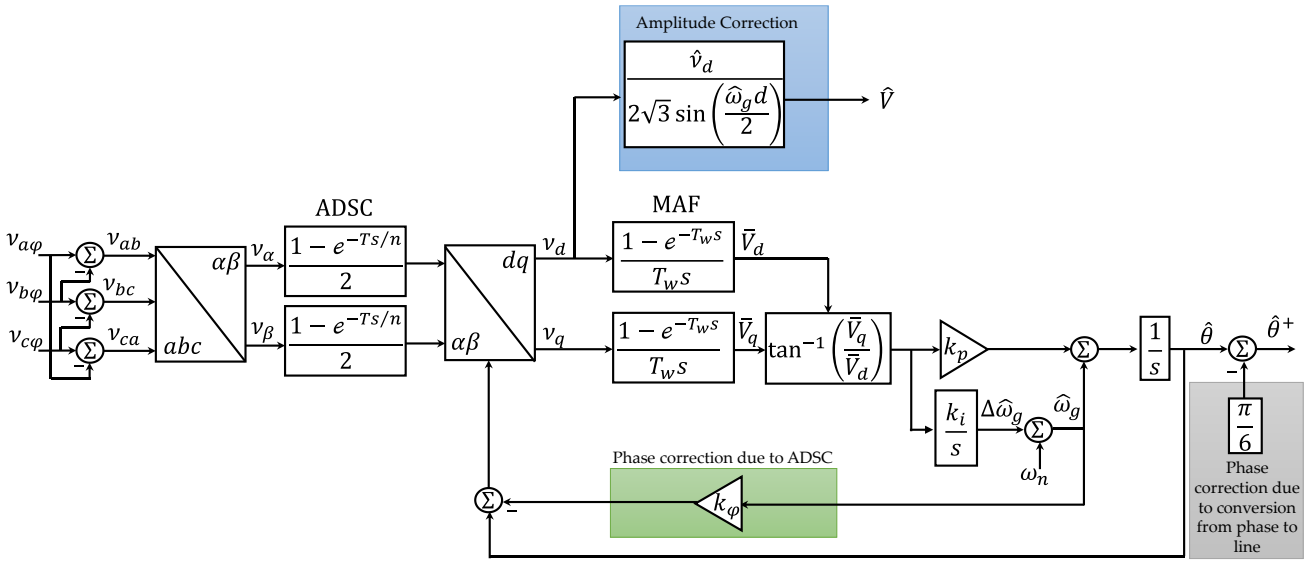


Figure 1. The block diagram of the proposed PLL.

2.1.1. Elimination of Odd Triple Harmonics

Typically, the grid-connected converters' phase at neutral voltage is a source of odd triple harmonics. Thus, a transformation to line voltage is adopted in the proposed PLL to eliminate the odd triple harmonics out of the box without any additional cost or complexity, allowing for the decrease in the MAF window length, hence speeding up the PLL dynamic response. To verify the elimination, assume the input voltages of three-phase has odd triple harmonics as:

$$v_{a\varphi} = V\sin(\theta) + \sum_{k=3,9,27,\ldots} V_k \sin(k\theta), \tag{1}$$

$$v_{b\varphi} = V\sin(\theta - \frac{2\pi}{3}) + \sum_{k=3,9,27,\ldots} V_k \sin\left(k\left(\theta - \frac{2\pi}{3}\right)\right), \tag{2}$$

$$v_{c\varphi} = V\sin(\theta + \frac{2\pi}{3}) + \sum_{k=3,9,27,\ldots} V_k \sin\left(k\left(\theta + \frac{2\pi}{3}\right)\right), \tag{3}$$

where θ is the phase, V is the amplitude of the grid voltage, and V_k is the amplitude of the odd triple harmonics. After some mathematical simplification, (1) to (3) can be written as shown in (4) to (6).

$$v_{ab} = \sqrt{3}V\sin\left(\theta + \frac{\pi}{6}\right), \tag{4}$$

$$v_{bc} = \sqrt{3}V\sin\left(\theta - \frac{\pi}{2}\right), \tag{5}$$

$$v_{ca} = \sqrt{3}V\sin\left(\theta + \frac{5\pi}{6}\right), \tag{6}$$

It can be noticed from (4) to (6) that the conversion from phase to line voltages eliminates the odd triple harmonics. However, it is worth mentioning that this conversation adds a phase shift of $\pi/6$ rad and scales the magnitude by $\sqrt{3}$.

2.1.2. Moving Average Filter (MAF)

The MAF is a linear phase filter that is deemed as a low-pass filter (LPF) [27,28]. Its transfer function can be written as in Equation (7):

$$G_{\mathrm{MAF}(s)} = \frac{1 - e^{-T_w s}}{T_w s}, \tag{7}$$

where T_w is the window length of the MAF; the block diagram of the MAF in the discrete domain is shown in Figure 2 [13].

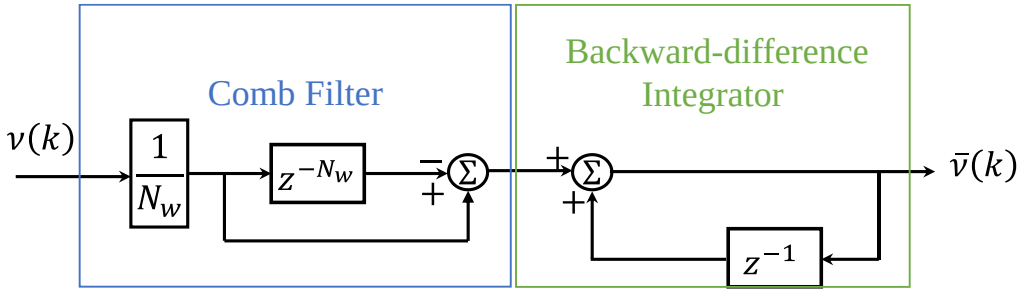


Figure 2. The block diagram of the MAF.

In Figure 2, $v(k)$ is the input signal, $\bar{v}(k)$ is the output signal, and N_w is the number of samples within the nominal period. The transfer function in the discrete domain can be expressed as:

$$G_{\mathrm{MAF}(\mathcal{Z})} = \frac{1}{N_w} \frac{1 - \mathcal{Z}^{-N_w}}{1 - \mathcal{Z}^{-1}}, \tag{8}$$

The magnitude and phase can be found by substituting ($s = j\omega$) into Equation (7)

$$G_{\mathrm{MAF}}(j\omega) = \left| \frac{sin\left(\frac{\omega T_w}{2}\right)}{\omega T_w/2} \right| \angle - \frac{\omega T_w}{2}, \tag{9}$$

The harmonic $(k \times f)$ positive-sequence harmonic in the $\alpha\beta$-frame is transformed into a $(k-1) \times f$ harmonics order in the dq-frame. In addition, the $(k \times f)$ negative-sequence harmonic in the $\alpha\beta$-frame is transformed into a $(k+1) \times f$ harmonic in the dq-frame, where k is the order of harmonics, and f is the nominal grid frequency. Therefore, the most common $\alpha\beta$ harmonics that appear in the input voltages of 5^{th}, 7^{th}, 11^{th}, 13^{th}, 17^{th}, and 19^{th} are transferred 6^{th}, 12^{th}, and 18^{th} in the dq-frame.

Based on Equation (9), the MAF has a unity gain at zero frequency and zero gains at frequencies $=2\pi k/T_w$, $(k = 1, 2, 3, \ldots)$. The harmonics rejection in the MAF is associated with its window length, which is adjusted to trade-off between noise reduction and response time, depending on the application's specific requirements. If the window length equals the nominal period, the DC-offset and the harmonics are rejected. In contrast, only odd harmonics are rejected if the window length is half the nominal period. The non-triple odd harmonics are rejected if the window length is adjusted to one-sixth of the nominal period [27]. This work adopts the window length of the sixth fundamental grid period allowing the PLL to block the non-triple odd harmonics while the line voltage blocks the triple harmonics.

2.1.3. Arbitrary Delayed Signal Cancellation (ADSC)

The ADSC blocks the DC offset in the αβ reference frame [11,23]. It is represented in (10) and shown in Figure 3.

$$\overline{v}_{\alpha\beta} = (v_{\alpha\beta}(t) - v_{\alpha\beta}(t-d))/2, \tag{10}$$

where $d = T/n$ is the time delay in s, T is the nominal grid period, and n is an arbitrary positive number. The transfer function of the ADSC can be expressed as in (11).

$$\text{ADSC}(s) = \frac{\overline{v}_{\alpha\beta}}{v_{\alpha\beta}} = \frac{1 - e^{-\frac{T}{n}s}}{2}, \tag{11}$$

which has the following magnitude and phase in the frequency domain:

$$\text{ADSC}(j\omega) = \left|\sin\left(\frac{\omega d}{2}\right)\right| \angle\left(\frac{\pi}{2} - \frac{\omega d}{2}\right), \tag{12}$$

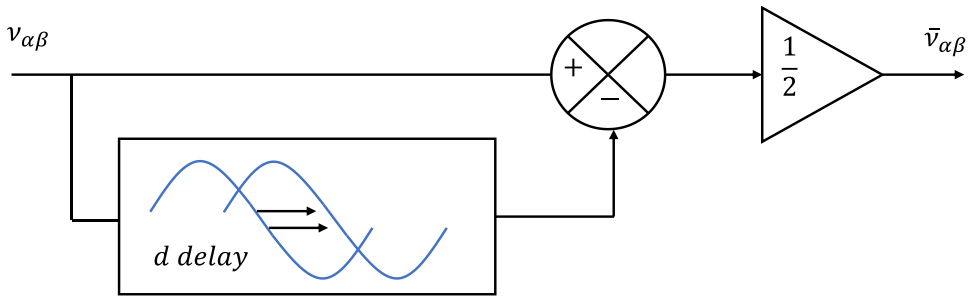


Figure 3. The block diagram of the ADSC operator.

2.1.4. Mathematical Model

The grid line voltages can be written as

$$\begin{bmatrix} v_{ab}(t) \\ v_{bc}(t) \\ v_{ca}(t) \end{bmatrix} = \sqrt{3}\left(\begin{bmatrix} V^+ \sin\left(\theta^+ + \frac{\pi}{6}\right) \\ V^+ \sin\left(\theta^+ - \frac{\pi}{2}\right) \\ V^+ \sin\left(\theta^+ + \frac{5\pi}{6}\right) \end{bmatrix} + \begin{bmatrix} V^- \sin\left(\theta^- + \frac{\pi}{6}\right) \\ V^- \sin\left(\theta^- + \frac{5\pi}{6}\right) \\ V^- \sin\left(\theta^- - \frac{\pi}{2}\right) \end{bmatrix} + \begin{bmatrix} V^0_{ab} \\ V^0_{bc} \\ V^0_{ca} \end{bmatrix} + \sum_{k=5,7,11\ldots}^{\infty} \begin{bmatrix} V^+_k \sin\left(\theta^+_k + \frac{\pi}{6}\right) \\ V^+_k \sin\left(\theta^+_k - \frac{\pi}{2}\right) \\ V^+_k \sin\left(\theta^+_k + \frac{5\pi}{6}\right) \end{bmatrix} + \sum_{k=5,7,11,\ldots}^{\infty} \begin{bmatrix} V^-_k \sin\left(\theta^-_k + \frac{\pi}{6}\right) \\ V^-_k \sin\left(\theta^-_k + \frac{5\pi}{6}\right) \\ V^-_k \sin\left(\theta^-_k - \frac{\pi}{2}\right) \end{bmatrix} \right), \tag{13}$$

where $\theta^+ = \omega_g t + \varphi^+$, $\theta^- = \omega_g t + \varphi^-$, $\theta^+_k = k\omega_g t + \varphi^+_k$, and $\theta^-_k = k\omega_g t + \varphi^-_k$. ω_g is the fundamental grid frequency; θ is the phase angle; φ^+ and φ^- are the initial phase angles of FFPS and FFNS, respectively; φ^+_k and φ^-_k are the initial phase angles of positive-sequence and negative-sequence harmonics, respectively; V^+ and V^- are the amplitudes of FFPS and FFNS, respectively; V^+_k and V^-_k are the amplitudes of positive-sequence and negative-sequence harmonics, respectively. V^0_{ab}, V^0_{bc}, and V^0_{ca} are the amplitudes of the DC offset components. Now, to convert from *abc*-frame to $\alpha\beta$-frame:

$$v_{\alpha\beta} = J_{\alpha\beta} \times v_{abc}(t), \tag{14}$$

where

$$J_{\alpha\beta} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}, \tag{15}$$

$$v_{\alpha\beta} = \sqrt{3}\left(\begin{bmatrix} V^+\sin\left(\theta+\frac{\pi}{6}\right) \\ -V^+\cos\left(\theta+\frac{\pi}{6}\right)\end{bmatrix} + \begin{bmatrix} V^-\sin\left(\theta+\frac{\pi}{6}\right) \\ V^-\cos\left(\theta+\frac{\pi}{6}\right)\end{bmatrix} + \frac{2}{3}\begin{bmatrix} V_{ab}^{dc} - \frac{1}{2}V_{bc}^{dc} - \frac{1}{2}V_{ca}^{dc} \\ 0 + \frac{\sqrt{3}}{2}V_{bc}^{dc} - \frac{\sqrt{3}}{2}V_{ca}^{dc}\end{bmatrix} + \sum_{k=5,7,11,\ldots}^{\infty}\begin{bmatrix} V_k^+\sin\left(\theta_k+\frac{\pi}{6}\right) \\ -V_k^+\cos\left(\theta_k+\frac{\pi}{6}\right)\end{bmatrix} + \sum_{k=5,7,11,\ldots}^{\infty}\begin{bmatrix} V_k^-\sin\left(\theta_k+\frac{\pi}{6}\right) \\ V_k^-\cos\left(\theta_k+\frac{\pi}{6}\right)\end{bmatrix}\right), \tag{16}$$

The DC components are canceled after using arbitrary delay signal cancellation (ADSC).

$$\overline{v}_{\alpha\beta} = \left(v_{\alpha\beta}^o(t) - v_{\alpha\beta}^o(t-d)\right) - \left(v_{\alpha\beta}^{dc} - v_{\alpha\beta}^{dc}\right) = v_{\alpha\beta}^o(t) - Y(\omega_g\tau)v_{\alpha\beta}^o(t), \tag{17}$$

where $v_{\alpha\beta}^{dc}$ is the DC-offset component, and $v_{\alpha\beta}^o$ are the other components of $v_{\alpha\beta}$.

Now, to convert from $\alpha\beta$-frame to dq-frame:

$$\begin{bmatrix} v_d \\ v_q\end{bmatrix} = Y(\theta+\theta_0)\begin{bmatrix} v_\alpha^o \\ v_\beta^o\end{bmatrix} - Y\left(\theta+\theta_0+\omega_g d\right)\begin{bmatrix} v_\alpha^o \\ v_\beta^o\end{bmatrix}, \tag{18}$$

where

$$Y(\theta) = \begin{bmatrix} \cos(\theta) & \sin(\theta) \\ -\sin(\theta) & \cos(\theta)\end{bmatrix}, \tag{19}$$

$$\begin{bmatrix} v_d \\ v_q\end{bmatrix} = 2\sqrt{3}\sin\left(\frac{\omega_g d}{2}\right)\left(V^+\begin{bmatrix} 1 \\ 0\end{bmatrix} + V^-\begin{bmatrix} -\cos(2\theta) \\ \sin(2\theta)\end{bmatrix} + \sum_{5,7,11\ldots}^{\infty}V_k^+\begin{bmatrix} \cos(\theta-\theta_k) \\ -\sin(\theta-\theta_k)\end{bmatrix} + \sum_{5,7,11\ldots}^{\infty}V_k^-\begin{bmatrix} -\cos(\theta+\theta_k) \\ \sin(\theta+\theta_k)\end{bmatrix}\right), \tag{20}$$

$Y(\theta)$ is the transformation matrix, and $\theta_0 = -\frac{\omega_g d}{2} - \frac{\pi}{6}$. Based on Equation (20), v_q is zero and the amplitude is scaled by $2\sqrt{3}\sin\left(\frac{\omega_g d}{2}\right)$. Moreover, the ADSC introduces a phase shift that can be corrected through feedback. In addition to that, the line-to-line transformation introduces a phase of $\frac{\pi}{6}$ that can be simply subtracted from the estimated phase to compensate for it, as shown in Figure 1. The v_d is multiplied by $\frac{1}{2\sqrt{3}\sin\left(\frac{\hat{\omega}_g d}{2}\right)}$ to compensate for the amplitude.

2.1.5. Small-Signal Model

The small-signal model can be written using $\hat{\theta}$ and substituting $\hat{\theta}_0 = -\frac{\hat{\omega}_g d}{2} - \frac{\pi}{6}$ into (20).

$$\begin{bmatrix} v_d \\ v_q\end{bmatrix} = Y\left(\hat{\theta} - \frac{\hat{\omega}_g d}{2}\right)\begin{bmatrix} v_\alpha^o \\ v_\beta^o\end{bmatrix} - Y\left(\hat{\theta} - \frac{\hat{\omega}_g d}{2} + \omega_g d\right)\begin{bmatrix} v_\alpha^o \\ v_\beta^o\end{bmatrix}, \tag{21}$$

After some approximations, with some trigonometric identities and using the MAF transfer function, $\nu_q(t)$ can be expressed as in Equation (22).

$$\hat{v}_q = 2V^+\sin\left(\frac{\omega_n d}{2}\right)\left[\left(-\frac{\Delta\omega_g d}{2}\right) + \left(\frac{\Delta\hat{\omega}_g d}{2}\right) + \left(\Delta\theta - \Delta\hat{\theta}\right)\right] \times G_{\mathrm{MAF}}(s), \tag{22}$$

$$\hat{v}_q = V^+\left(2\sin\left(\frac{\omega_n d}{2}\right)\right)\left[\underbrace{\frac{\left(1+e^{-ds}\right)}{2}}_{\mathrm{ADSC}(s)}\Delta\theta(s) - \Delta\hat{\theta}(s) + \frac{\Delta\hat{\omega}_g d}{2}\right]\underbrace{\frac{1-e^{-T_w s}}{T_w s}}_{\mathrm{MAF}(s)}, \tag{23}$$

$$\hat{v}_q = \left[\underbrace{\frac{\left(1+e^{-ds}\right)}{2}}_{\mathrm{ADSC}(s)}\Delta\theta(s) - \Delta\hat{\theta}(s) + \frac{\Delta\hat{\omega}_g d}{2}\right]\underbrace{\frac{1}{\frac{T_w}{2}s+1}}_{\mathrm{MAF}(s)}, \tag{24}$$

The small-signal model of the proposed method is shown in Figure 4.

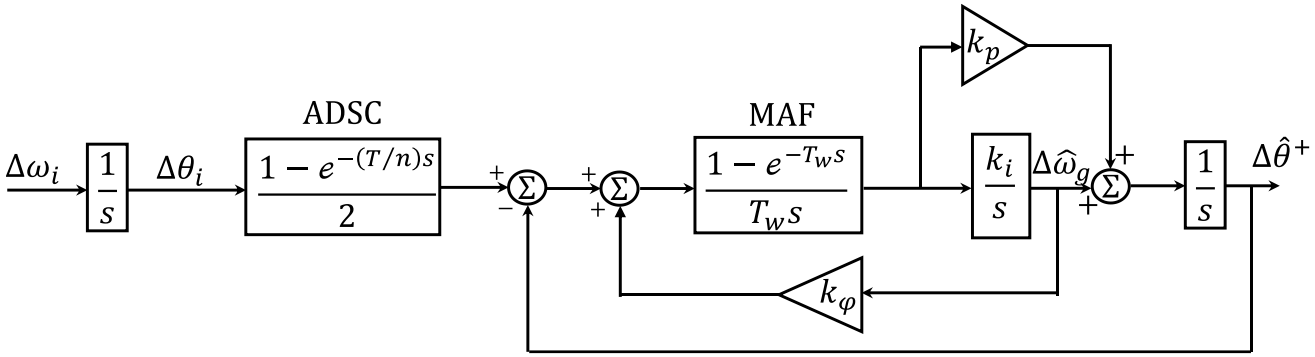


Figure 4. The block diagram of the small-signal model for the proposed PLL.

2.2. The Loop Filter Design

The LF is designed based on a modified third-order polynomial (25), in which the polynomial coefficients are tuned using stochastic optimization with the objective function and constraints to minimize the settling time of the frequency deviation.

$$s^3 + a_2\omega_0 s^2 + a_1\omega_0^2 s + \omega_0^3 = 0 \tag{25}$$

The stability of the modified polynomial is determined using the Routh–Hurwitz criterion, from which the coefficients of the modified polynomial must obey the following conditions:

$$\omega_0 > 0, \tag{26}$$

$$a_2 > 0, \tag{27}$$

$$a_2 a_1 > 1, \tag{28}$$

Based on the small-signal model, the closed-loop transfer function is shown in (29):

$$\frac{\Delta\hat{\theta}}{\Delta\theta_i} = \frac{1-e^{-Ts/n}}{2}\frac{k_p s + \frac{2}{T_w}k_i}{s^3 + \frac{2}{T_w}s^2 + \frac{2}{T_w}\left(k_p - k_i\frac{d}{2}\right)s + \frac{2}{T_w}k_i}, \tag{29}$$

Comparing (25) with the characteristic equation of (29), k_p and k_i can be rewritten in terms of the coefficients of the modified polynomial as:

$$k_i = \frac{4}{T_w^2 a_2^3}, \tag{30}$$

$$k_p = \frac{2}{T_w a_2^2}\left(\frac{d}{T_w a_2} + a_1\right), \tag{31}$$

where $T_w = T/6$ is the window length, d is the phase delay, and a_1 and a_2 determine the optimum parameter of the LF proportional-integral (PI)-gains. The optimization formulation is shown in (32). The flowchart that summarizes the optimization process is shown in Figure 5.

$$\begin{aligned} &\text{Min } J(a_1,\ a_2) = t_{ss} \\ &\text{subject to} \begin{cases} OS < 2\% \\ a_1 a_2 > 1 \\ a_2 > 0 \\ (a_1)_{min} \le a_1 \le (a_1)_{max} \\ (a_2)_{min} \le a_2 \le (a_2)_{max} \end{cases} \end{aligned}, \tag{32}$$

where the objective function (J) is the settling time (t_{ss}) of the frequency deviation, OS is the overshoot, and $(a)_{min}$ and $(a)_{max}$ are the coefficients' boundaries that are selected to be $1 \le a_1 \le 20$ and $1 \le a_2 \le 20$.

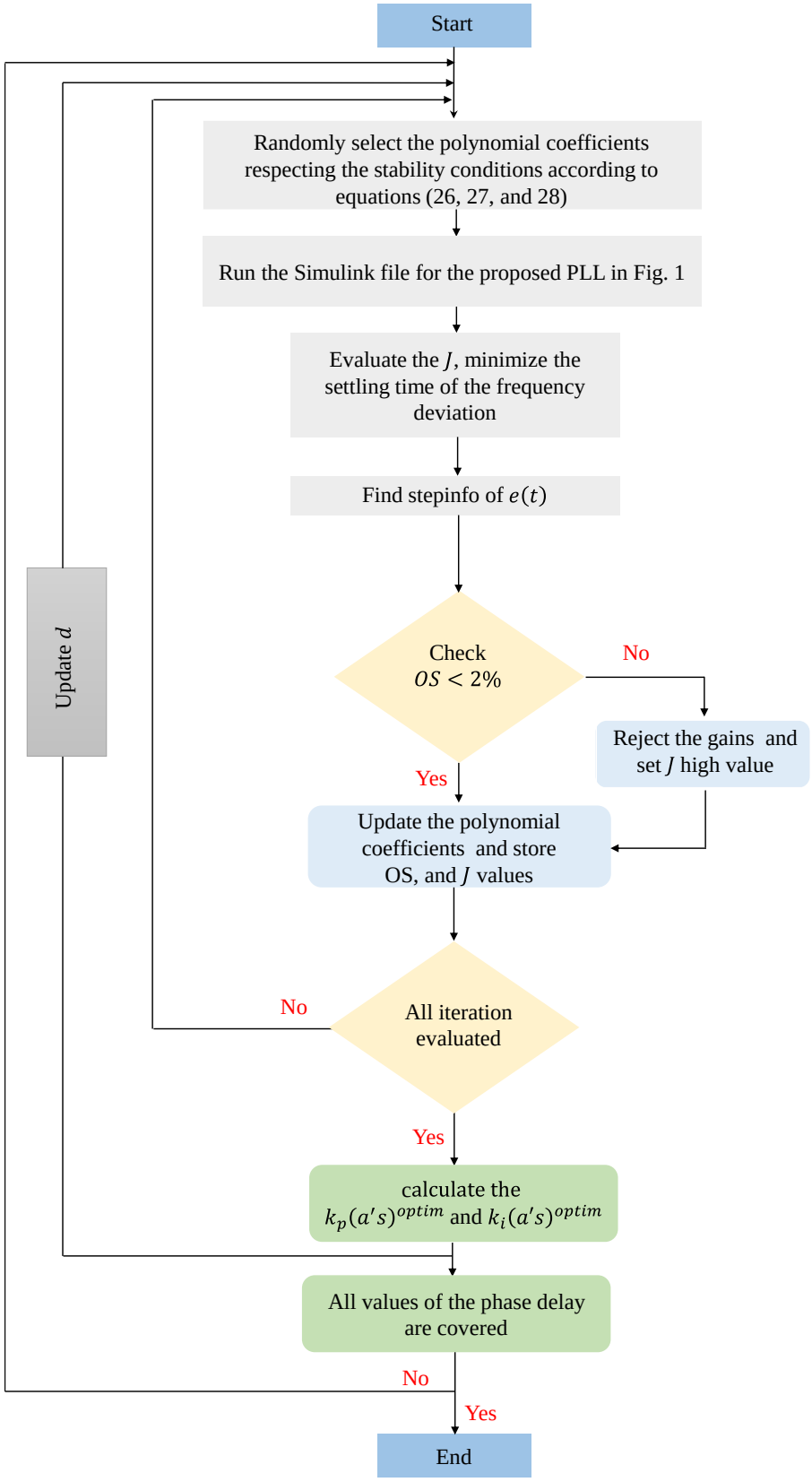


Figure 5. Flow chart of the optimization method.

Different optimization methods were investigated for the selection of the coefficients a_1 and a_2: Particle swarm optimization (PSO), genetic algorithm (GA), bee algorithm (BA),

and cuckoo optimization algorithm (COA) [29–31]. The results of the aforementioned optimization methods are shown in Table 1.

Table 1. Optimization method comparison.

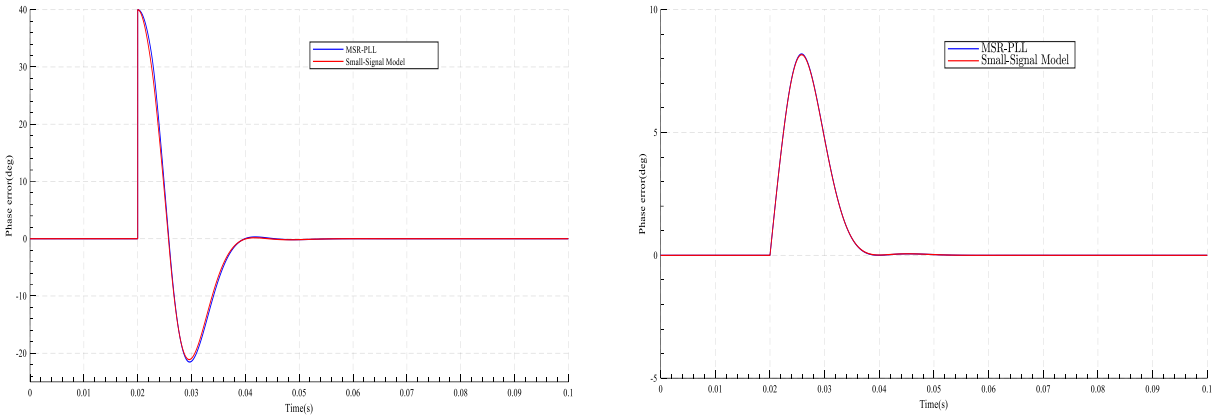
Method	a_1	a_2	J	OS
GA	2.2776	2.0026	0.0165	0.0625
PSO	2.2531	1.9532	0.0159	0.0675
BA	2.24531	1.9668	0.0156	0.0660
COA	2.27480	2.0444	0.0164	0.0586

The results of the COA optimum parameters are adopted without loss of generality. The corresponding PI-controller gains for all d values are listed in Table 2. It can be noticed that k_i is constant for any d. This is because (30) depends on the window length and the coefficient a_2 only, which is a constant independent of d.

Table 2. The optimum PI-controller.

d	k_p	k_i
$T/2$	537.22	42,131
$T/4$	431.89	42,131
$T/8$	379.22	42,131
$T/10$	368.69	42,131
$T/12$	361.67	42,131
$T/16$	352.89	42,131
$T/32$	339.73	42,131

Figure 6 shows the response of the actual model along with its small-signal model under a 40° phase jump and a 6 Hz frequency jump from a 50 Hz grid frequency, validating the small-signal model in predicting the response of the actual PLL at a distinct phase delay.



(**a**) (**b**)

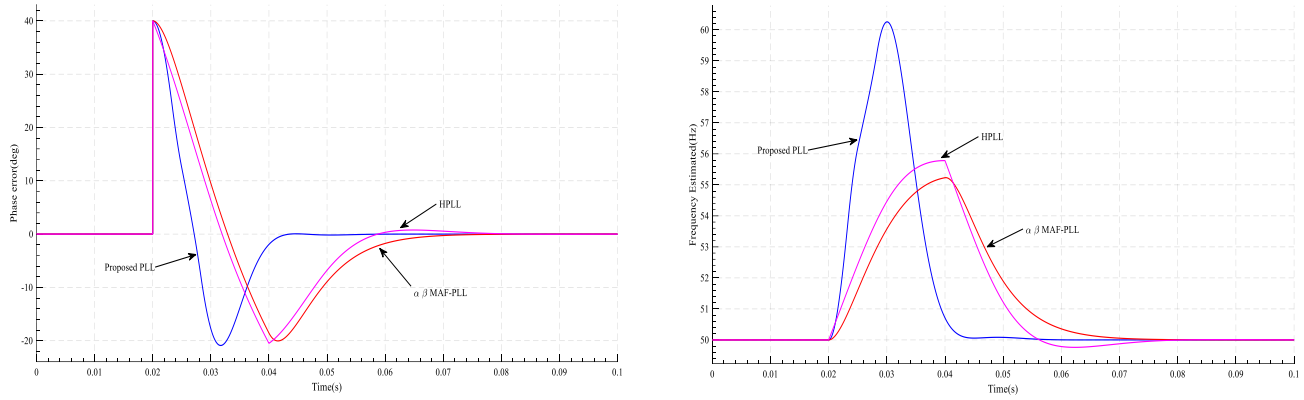
Figure 6. The proposed PLL and its small-signal model at t = 0.02 s under (**a**) + 40° at $d = T/8$ and (**b**) +6 Hz at $d = T/8$.

3. Simulation Results

The performance of the utilized PLL adopting the proposed third-order optimized polynomial with DC-offset and harmonics rejection is verified using numerical simulation. It is compared with $\alpha\beta$MAF-PLL [13] and hybrid-PLL (HPLL) [15]. The nominal grid

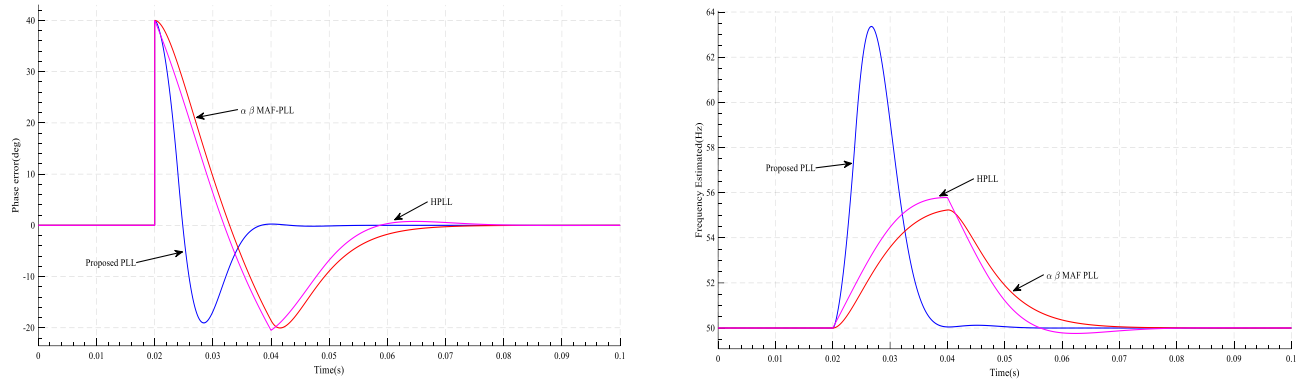
frequency is $f_n = 50$ Hz, and the parameters of the compared PLLs are summarized in Table 3, while the grid harmonics are listed in Table 4. Several case studies were considered for a fair comparison, as shown below:

Case 1: A phase jump of 40° at 0.02 s and $d = T/4,\ T/16$, and $T/32$. The results are shown in Figures 7–9, respectively, and summarized in Table 5.
Case 2: A frequency jump in the grid from 50 to 56 Hz at 0.02 s and $d = T/4,\ T/16$, and $T/32$. The results are shown in Figures 10–12, respectively, and summarized in Table 6.
Case 3: Only DC-offset is added to the grid voltage by 0.1 pu of phase a, -0.1 of phase b, and 0.05 of phase c at 0.02 s, and $d = T/4,\ T/16$, and $T/32$. The results are shown in Figures 13–15, respectively, and summarized in Table 7.
Case 4: A frequency jump of 5 Hz with DC-offsets similar to case three with harmonics, listed in Table 4, is added at 0.02 s for $d = T/4,\ T/16$, and $T/32$. The results are shown in Figures 16–18, respectively, and summarized in Table 8.



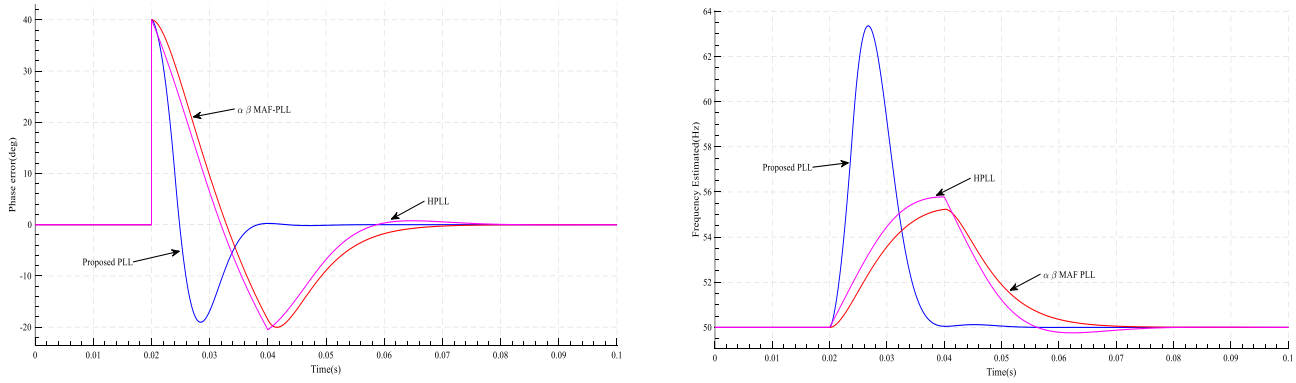
(**a**) (**b**)

Figure 7. The results of case 1 at $d = T/4$ and at t = 0.02 s: (**a**) PLL's phase error; (**b**) the frequency estimated by PLL.



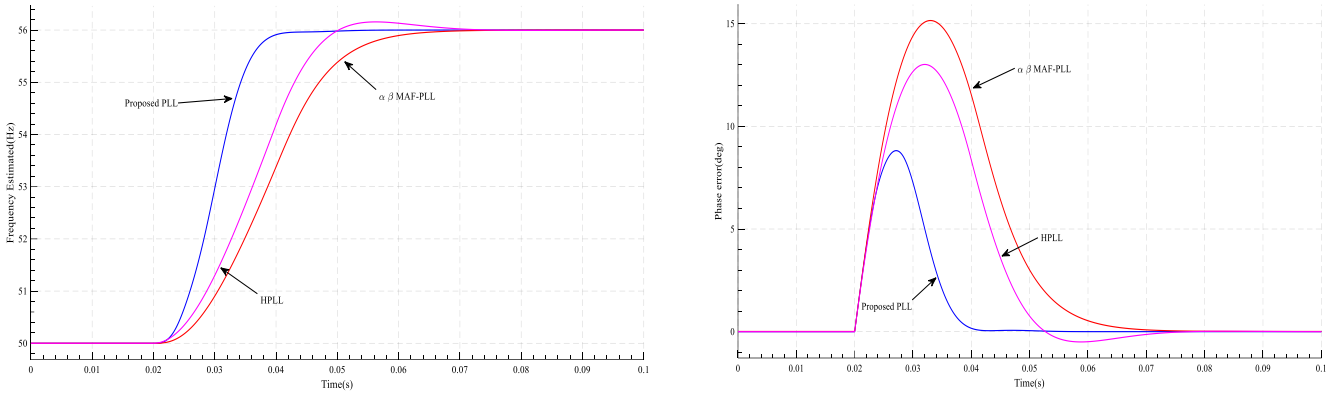
(**a**) (b)

Figure 8. The results of case 1 at $d = T/16$ and at t = 0.02 s: (**a**) PLL's phase error; (**b**) the frequency estimated by PLL.



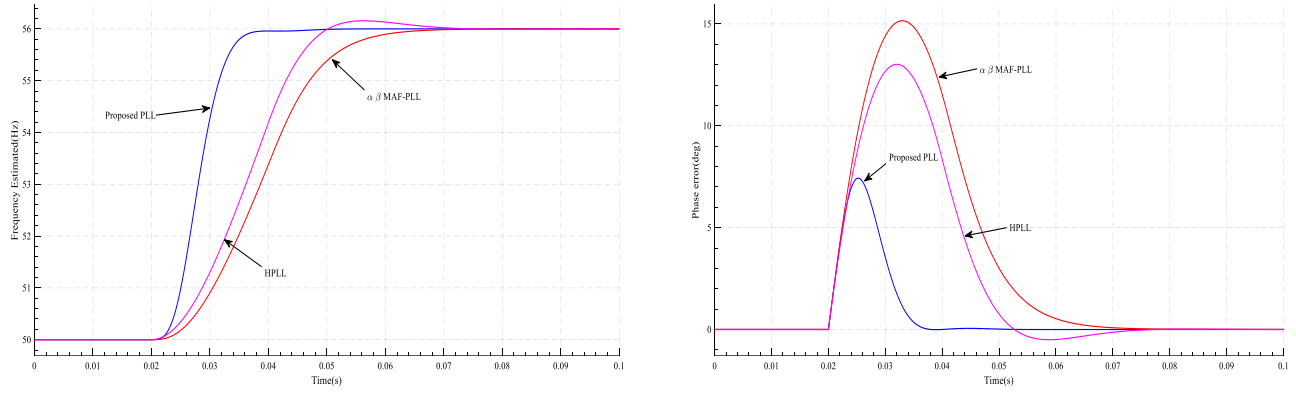
(**a**) (**b**)

Figure 9. The results of case 1 at $d = T/32$ and at t = 0.02 s: (**a**) PLL's phase error: (**b**) the frequency estimated by PLL.



(**a**) (**b**)

Figure 10. The results of case 2 at $d = T/4$ and at t = 0.02 s: (**a**) the frequency estimated by PLL; (**b**) PLL's phase error.

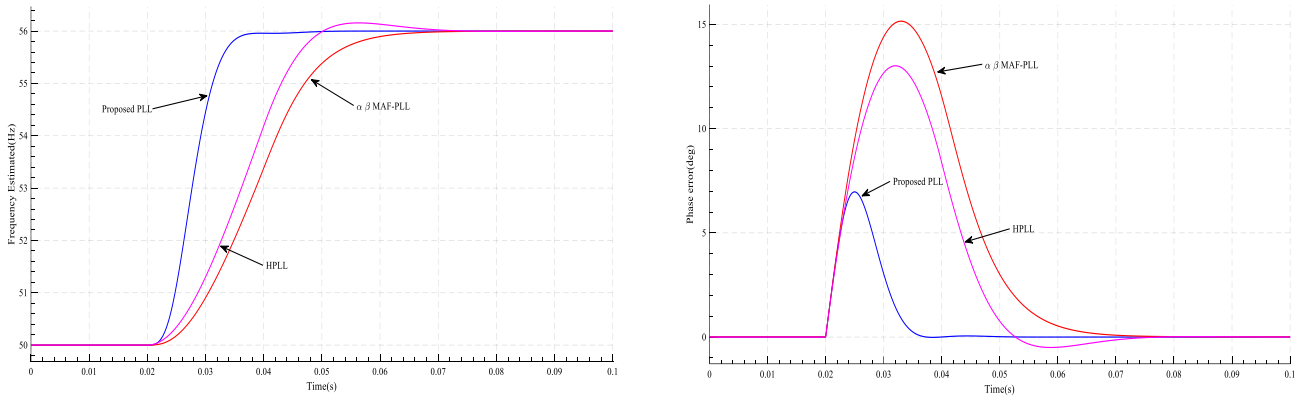


(**a**) (**b**)

Figure 11. The results of case 2 at $d = T/16$ and at t = 0.02 s: (**a**) the frequency estimated by PLL; (**b**) PLL's phase error.

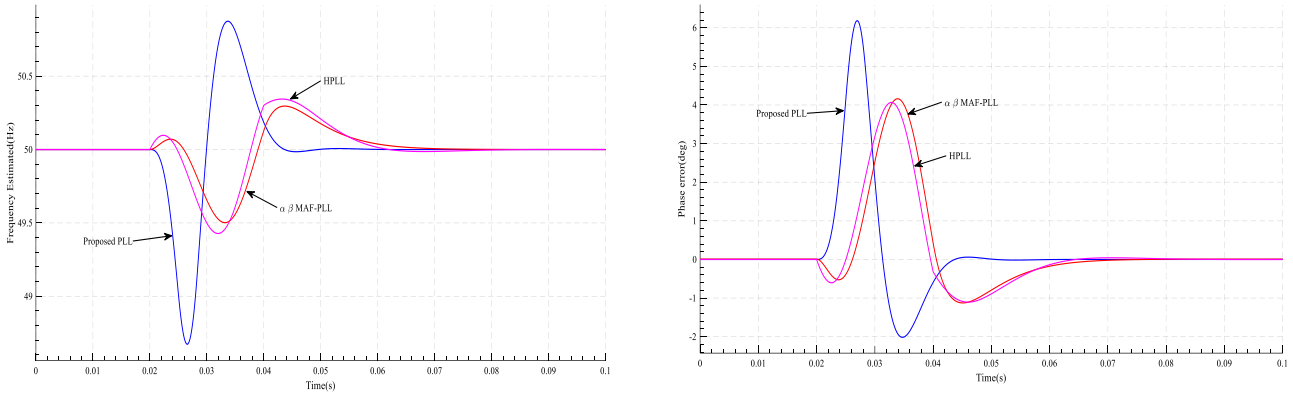
Table 3. Control parameter values.

Method	k_p	k_i
HPLL	94	-
$\alpha\beta$MAF-PLL	439.6	48,312



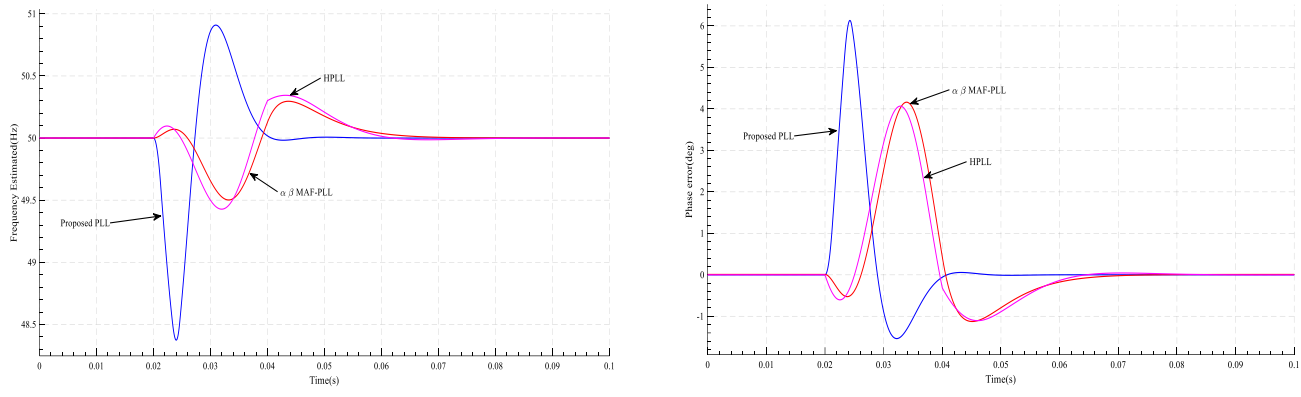
(**a**) (**b**)

Figure 12. The results of case 2 at $d = T/32$ and at t = 0.02 s: (**a**) the frequency estimated by PLL; (**b**) PLL's phase error.



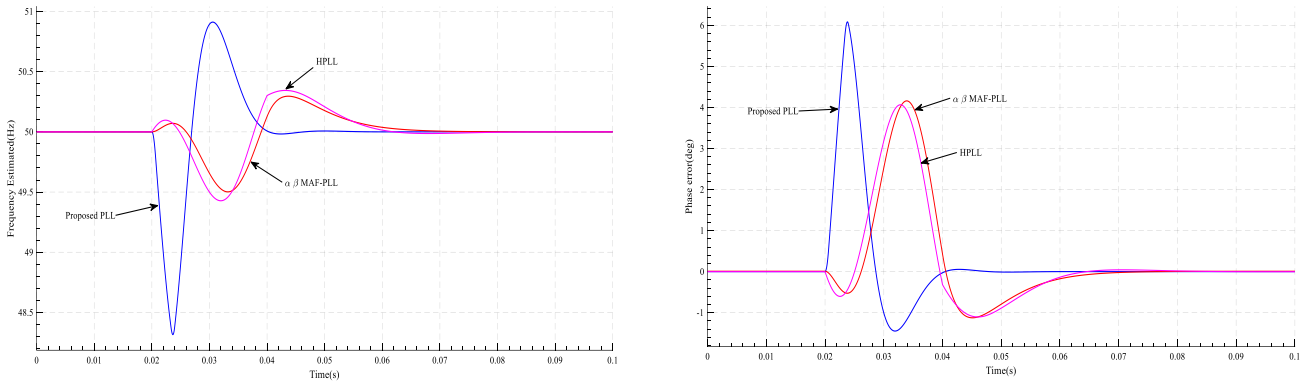
(**a**) (**b**)

Figure 13. The results of case 3 at $d = T/4$ and at t = 0.02 s; (**a**) the frequency estimated by PLL; (**b**) PLL's phase error.



(**a**) (**b**)

Figure 14. The results of case 3 at $d = T/16$ and at t = 0.02 s: (**a**) the frequency estimated by PLL; (**b**) PLL's phase error.

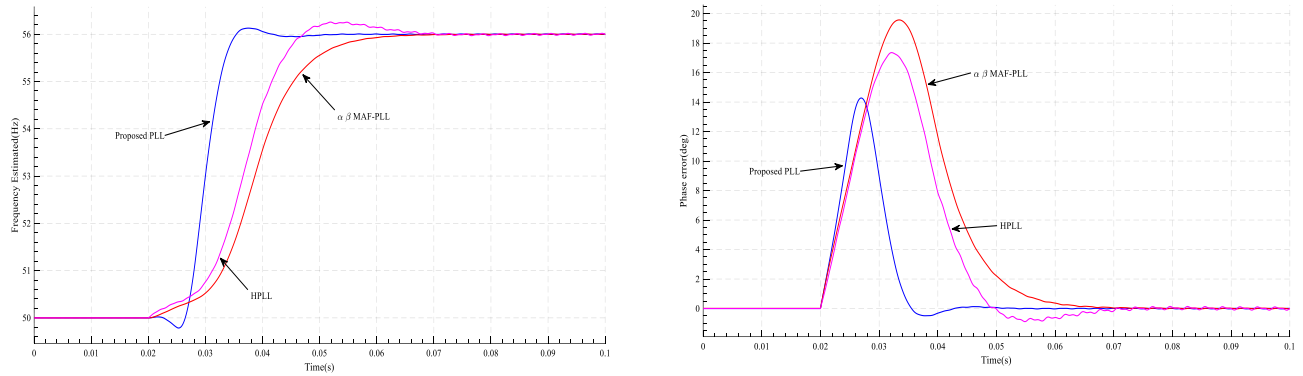


(**a**) (**b**)

Figure 15. The results of case 4 at $d = T/32$ and at t = 0.02 s: (**a**) the frequency estimated by PLL; (**b**) PLL's phase error.

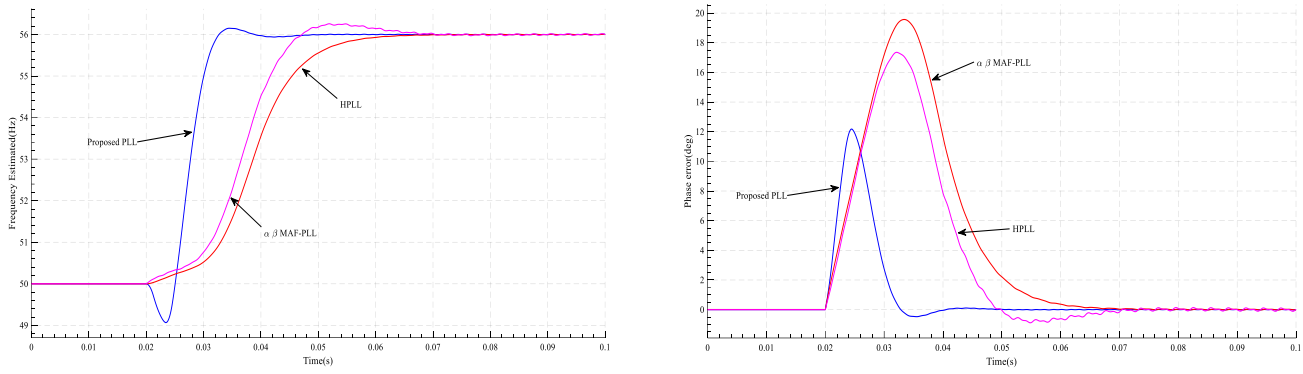
Table 4. Parameters of distortion in input voltage.

Component	−1	−3	+5	+7	+9	+11	+13	+27
Amplitude (p.u.)	0.01	0.05	0.01	0.01	0.05	0.01	0.01	0.05
THD ≈ 9%								



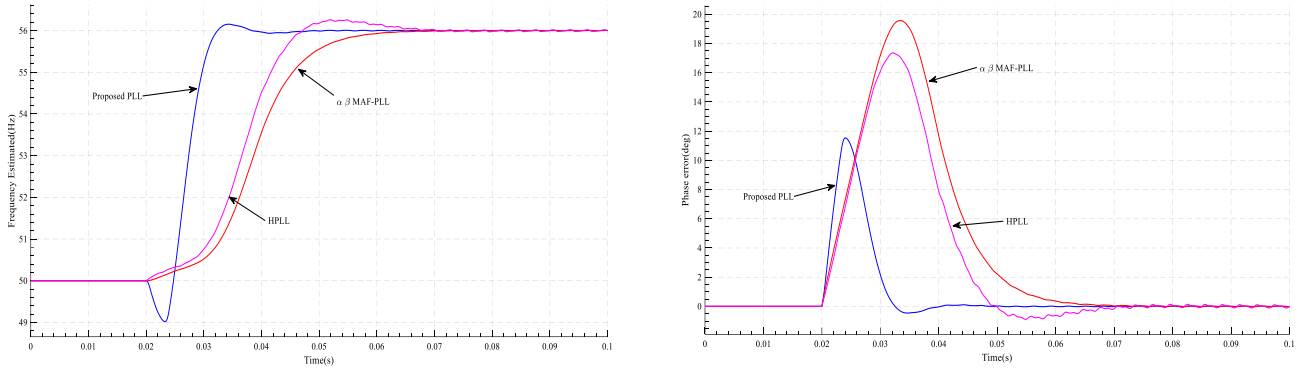
(**a**) (**b**)

Figure 16. The results of case 4 at $d = T/4$ and t = 0.02 s: (**a**) the frequency estimated by PLL; (**b**) PLL's phase error.



(**a**) (**b**)

Figure 17. The results of case 4 at $d = T/16$ and t = 0.02 s: (**a**) the frequency estimated by PLL; (**b**) PLL's phase error.



(**a**) (**b**)

Figure 18. The results of case 4 at $d = T/32$ and t = 0.02 s: (**a**) the frequency estimated by PLL; (**b**) PLL's phase error.

Table 5. The results of case 1 (Phase Jump).

	The Proposed PLL				
	n				
	32	**16**	**4**	**$\alpha\beta$MAF-PLL**	**HPLL**
40 deg phase jump					
Phase settling time (ms)	16.8	17.3	21.3	44.4	36.7
Overshoot (%)	47.62	49.95	52.23	50.13	51.24
Peak frequency error (Hz)	13.36	13.1	10.25	5.23	5.78

Table 6. The results of case 2 (Frequency Jump).

	The Proposed PLL				
	n				
	32	**16**	**4**	**$\alpha\beta$MAF-PLL**	**HPLL**
6 Hz frequency jump					
2% frequency settling time (ms)	15.6	16	19.3	39.3	40.9
Overshoot (%)	0	0	0	0	2.61
Peak phase error (°)	6.96	7.43	8.82	15.16	13.02

Table 7. The results of case 3 (DC-Offset).

	The Proposed PLL				
	n				
	32	**16**	**4**	**$\alpha\beta$MAF-PLL**	**HPLL**
DC-offset					
Phase settling time (ms)	19	19.4	22.4	44.6	41.4
Peak frequency error (Hz)	0.91	0.91	0.87	0.3	0.34
Peak phase error (°)	6.08	6.13	6.18	4.16	4.06

Table 8. The results of case 4 (Frequency Jump with Harmonics and DC-Offset).

	The Proposed PLL				
	n				
	32	**16**	**4**	**$\alpha\beta$MAF-PLL**	**HPLL**
6 Hz frequency jump with harmonics and DC-offset					
2% frequency settling time(ms)	14.8	15.7	18.1	37.1	41.1
Peak phase error (°)	11.53	12.8	14.57	19.57	17.35
Peak frequency error (Hz)	0.15	0.15	0.13	0	0.26

4. Discussion

Tables 5–8 summarize the performance comparisons between the proposed PLL, the αβMAF-PLL, and HPLL. The comparison is made considering the phase settling time, the frequency settling time, the overshoot, the estimated frequency peak, and the phase error peak. In the first case, it can be noticed that the proposed PLL has the fastest dynamic response reaching the steady state in less than 0.02 s for any delay factor except $\tau = T/4$ for which it needs about 1.1 grid cycles, while the other PLLs need about two grid cycles to settle down. The phase percent overshoot is slightly better than those of the other methods. In the case of frequency jump, the proposed PLL has the fastest dynamic response and reaches the steady state in less than one grid cycle without overshooting for any delay factor. Concerning DC offset, the proposed method rejects the DC offset two times faster than the other methods. The peak frequency and phase errors are almost the same as the other methods. In the last case—the frequency jump with DC-offset and harmonics—the proposed PLL achieves the fastest response with less peak phase error with respect to other methods, synchronizing with the grid in a fraction of a grid cycle.

5. Experimental Verification

To demonstrate the performance enhancement of the proposed PLL and the LF design with comparisons to HPLL and $\alpha\beta$MAF-PLL, digital implementation of all the PLLs is made utilizing the DE2-115 development and education board from Altera. An AC power supply is used to generate the voltage signal. The experiment maintains the grid voltage amplitude (V) and sampling frequency (f_S) at 1 pu and 10 kHz, respectively. The nominal grid frequency is 50 Hz. The results are captured using RIGOL MSO5354 mixed-signal oscilloscopes. Two cases are considered adopting $d = T/4$ without loss of generality.

Case A: From the ideal grid condition, three disturbances occur simultaneously, including the dominant harmonics listed in Table 4 with DC-offset (0.1 pu to phase a, -0.1 pu to phase b, and 0.05 pu to phase c) and a frequency jump by 6 Hz. The results of the phase error and the estimated grid frequency of all the PLLs are shown in Figure 19.

Case B: The frequency jump in case A is replaced by a phase jump of 45° while keeping the harmonic and DC-offset. The results of the phase error and the estimated grid frequency of all the compared PLLs are shown in Figure 20.

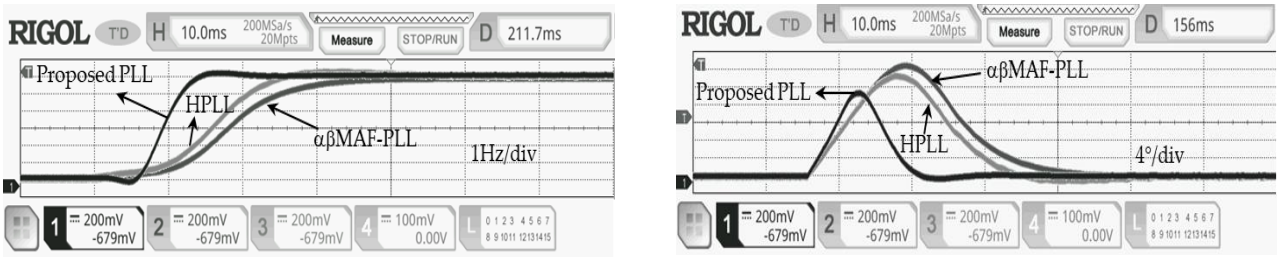


Figure 19. The results under case A: (**a**) the phase error and (**b**) the estimated grid frequency.

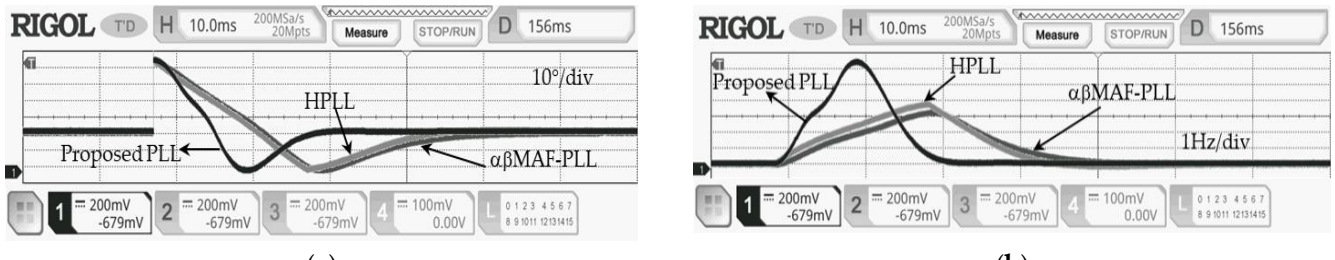


Figure 20. The results of case B: (**a**) PLL's phase error and (**b**) the estimated grid frequency.

The experimental results agree with the simulation, which validates the proposed method.

6. Conclusions

A new approach for designing the loop filter of a third-order phase-locked loop is proposed in this paper. The proposed PLL consists of a moving average filter and an arbitrarily delayed signal cancelation. The arbitrary delay signal cancelation blocks the DC offset. In contrast, the moving average filter, with a window length of one-sixth of the fundamental grid period, blocks non-triple odd harmonics. The remaining triple harmonics are blocked utilizing the line voltage. The loop filter design is based on a modified third-order polynomial derived from stochastic optimization with the settling time of the frequency deviation as the objective function. The effectiveness of the proposed PLL and the adopted loop filter design method is verified by comparing their performance with other related PLLs, demonstrating the offered improvements. The simulation and experimental results show that the proposed PLL achieves synchronization within one grid cycle two times faster than the other PLLs. Therefore, the proposed PLL can be used to ensure that the renewable energy source can be safely and efficiently integrated into the grid.

Author Contributions: Conceptualization, I.A.S.; Software, H.A.K.; Validation, I.A.S. and H.A.K.; Investigation, H.A.K. and I.E.A.; Writing—Original Draft, H.A.K.; Writing—Review and Editing, I.A.S. and I.E.A.; Visualization, I.E.A.; Supervision, I.A.S.; Funding Acquisition, I.E.A. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Data Availability Statement: Not applicable.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Yang, L.; Cao, T.; Chen, H.; Dong, X.; Zhang, S. Robust Control and Optimization Method for Single-Phase Grid-Connected Inverters Based on All-Pass-Filter Phase-Locked Loop in Weak Grid. *Energies* **2022**, *15*, 7355. [CrossRef]
2. Stojić, D. Improved observer-based quadrature signal generator. *Electr. Eng.* **2021**, *103*, 3063–3073. [CrossRef]
3. Luhtala, R.; Alenius, H.; Roinila, T. Practical Implementation of Adaptive SRF-PLL for Three-Phase Inverters Based on Sensitivity Function and Real-Time Grid-Impedance Measurements. *Energies* **2020**, *13*, 1173. [CrossRef]
4. Chahine, K.; Tarnini, M.; Moubayed, N.; El Ghaly, A. Power Quality Enhancement of Grid-Connected Renewable Systems Using a Matrix-Pencil-Based Active Power Filter. *Sustainability* **2023**, *15*, 887. [CrossRef]
5. Aldbaiat, B.; Nour, M.; Radwan, E.; Awada, E. Grid-Connected PV System with Reactive Power Management and an Optimized SRF-PLL Using Genetic Algorithm. *Energies* **2022**, *15*, 2177. [CrossRef]
6. Wang, Z.; Fu, P.; Huang, L.; Chen, X.; He, S.; Zhang, X.; Yang, J. Performance improvement of a three-phase PLL under distorted grid conditions based on frequency adaptive hybrid prefiltering. *IET Power Electron.* **2022**, *5*, 1429–1440. [CrossRef]
7. Luo, W.; Wei, D. A frequency-adaptive improved moving-average-filter-based quasi-type-1 PLL for adverse grid conditions. *IEEE Access* **2020**, *8*, 54145–54153. [CrossRef]
8. Wang, J.; Liang, J.; Gao, F.; Zhang, L.; Wang, Z. A method to improve the dynamic performance of moving average filter-based PLL. *IEEE Trans. Power Electron.* **2014**, *30*, 5978–5990. [CrossRef]
9. Smadi, I.A.; Fawaz, B.H.B. Phase-locked loop with DC offset removal for single-phase grid-connected converters. *Electr. Power Syst. Res.* **2021**, *194*, 106980. [CrossRef]
10. Garg, R.; Mahajan, P. Control of Grid Integrated Photovoltaic system using new Variable Step Size Least Mean Square adaptive filter. *Electr. Eng.* **2021**, *103*, 2945–2959.
11. Smadi, I.A.; Sultan, W. A phase-locked loop with an improved dynamic response under abnormal grid conditions. *Comput. Electr. Eng.* **2022**, *97*, 107645. [CrossRef]
12. Xie, M.; Zhu, C.; He, L.; Wen, H. An experimental study of MAF-SRF-PLL with comb compensator. In Proceedings of the 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), Tampa, FL, USA, 26–30 March 2017; pp. 1310–1313.
13. Li, J.; Wang, Q.; Xiao, L.; Hu, Y.; Wu, Q.; Liu, Z. An αβ-Frame Moving Average Filter to Improve the Dynamic Performance of Phase-Locked Loop. *IEEE Access* **2020**, *8*, 180661–180671. [CrossRef]
14. Golestan, S.; Freijedo, F.D.; Vidal, A.; Guerrero, J.M.; Doval-Gandoy, J. A quasi-type-1 phase-locked loop structure. *IEEE Trans. Power Electron.* **2014**, *29*, 6264–6270. [CrossRef]
15. Golestan, S.; Guerrero, J.M.; Abusorrah, A.M.; Al-Turki, Y. Hybrid synchronous/stationary reference-frame-filtering-based PLL. *IEEE Trans. Ind. Electron.* **2015**, *62*, 5018–5022. [CrossRef]

16. He, X.; Liu, M.; Li, Y.; Hong, F.; Yang, J.; Jiang, F. Synchronous Reference Frame Paralleled MAF/DSC-Based PLL. In Proceedings of the 2020 Asia Energy and Electrical Engineering Symposium (AEEES), Chengdu, China, 29–31 May 2020; pp. 361–364.
17. Golestan, S.; Guerrero, J.M.; Vasquez, J.C. A nonadaptive window-based pll for single-phase applications. *IEEE Trans. Power Electron.* **2017**, *33*, 24–31. [CrossRef]
18. Wanchana, S.; Benjanarasuth, T.; Komine, N.; Ngamwiwit, J. PLL equivalent augmented system incorporated with state feedback designed by LQR. *Int. J. Control Autom. Syst.* **2007**, *5*, 161–169.
19. Niu, X.; Li, B.; Ziedan, N.I.; Guo, W.; Liu, J. Analytical and simulation-based comparison between traditional and Kalman filter-based phase-locked loops. *GPS Solut.* **2017**, *21*, 123–135. [CrossRef]
20. Hamed, H.A.; Abdou, A.F.; Bayoumi, E.; EL-Kholy, E.E. Effective design and implementation of GSS-PLL under voltage dip and phase interruption. *IET Power Electron.* **2018**, *11*, 1018–1028. [CrossRef]
21. Golestan, S.F.; Freijedo, F.D.; Guerrero, J.M. A systematic approach to design high-order phase-locked loops. *IEEE Trans. Power Electron.* **2014**, *30*, 2885–2890. [CrossRef]
22. Smadi, I.A.; Bany Fawaz, B.H. DC offset rejection in a frequency-fixed second-order generalized integrator-based phase-locked loop for single-phase grid-connected applications. *Prot. Control Mod. Power Syst.* **2022**, *7*, 1. [CrossRef]
23. Smadi, I.A.; Issa, M.B. Phase Locked Loop with DC-Offset Removal for Grid Synchronization. In Proceedings of the IECON 2019—45th Annual Conference of the IEEE Industrial Electronics Society, Lisbon, Portugal, 14–17 October 2019; Volume 1, pp. 4669–4673.
24. Golestan, S.; Guerrero, J.M.; Vidal, A.; Yepes, A.G.; Doval-Gandoy, J. PLL with MAF-based prefiltering stage: Small-signal modeling and performance enhancement. *IEEE Trans. Power Electron.* **2015**, *31*, 4013–4019. [CrossRef]
25. Kathiresan, A.C.; PandiaRajan, J.; Sivaprakash, A.; Sudhakar Babu, T.; Islam, M.R. An Adaptive Feed-Forward Phase Locked Loop for Grid Synchronization of Renewable Energy Systems under Wide Frequency Deviations. *Sustainability* **2020**, *12*, 7048. [CrossRef]
26. Hui, N.; Wang, D.; Li, Y. A novel hybrid filter-based PLL to eliminate effect of input harmonics and DC offset. *IEEE Access* **2018**, *6*, 19762–19773. [CrossRef]
27. Mellouli, M.S.; Hamouda, M.; Slama, J.B.H.; Al Haddad, K. A third-order MAF Based QT1-PLL that is robust against harmonically distorted grid voltage with frequency deviation. *IEEE Trans. Energy Convers.* **2021**, *36*, 1600–1613. [CrossRef]
28. Golestan, S.; Guerrero, J.M.; Vasquez, J.C. Three-phase PLLs: A review of recent advances. *IEEE Trans. Power Electron.* **2016**, *32*, 1894–1907. [CrossRef]
29. De Melo Menezes, B.A.; Herrmann, N.; Kuchen, H.; Buarque de Lima Neto, F. High-Level Parallel Ant Colony Optimization with Algorithmic Skeletons. *Int. J. Parallel Program.* **2021**, *49*, 776–801. [CrossRef]
30. Panag, T.S.; Dhillon, J.S. A novel random transition based PSO algorithm to maximize the lifetime of wireless sensor networks. *Wirel. Pers. Commun.* **2018**, *98*, 2261–2290. [CrossRef]
31. Roni, M.H.K.; Rana, M.S.; Pota, H.R.; Hasan, M.M.; Hussain, M.S. Recent trends in bio-inspired meta-heuristic optimization techniques in control applications for electrical systems: A review. *Int. J. Dyn. Control* **2022**, *10*, 999–1011. [CrossRef]