energies

MDPI

Review

A Comparative Review on Single Phase Transformerless Inverter Topologies for Grid-Connected Photovoltaic Systems

Md. Faruk Kibria [1,2,*], Ahmed Elsanabary [3,4], Kok Soon Tey [5], Marizan Mubin [1] and Saad Mekhilef [1,3,6,*]

1 Power Electronics and Renewable Energy Research Laboratory (PEARL), Department of Electrical Engineering, University of Malaya, Kuala Lumpur 50603, Malaysia
2 Department of Electrical and Electronic Engineering, Hajee Mohammad Danesh Science and Technology University, Dinajpur 5200, Bangladesh
3 Institute of Power Engineering (IPE), Universiti Tenaga Nasional, Kajang 43000, Malaysia
4 Department of Electrical Engineering, Port Said University, Port Said 42526, Egypt
5 Faculty of Computer Science and Information Technology, University of Malaya, Kuala Lumpur 50603, Malaysia
6 School of Science, Computing and Engineering Technologies, Swinburne University of Technology, Hawthorn, VIC 3122, Australia
* Correspondence: mfkibria.eee@hstu.ac.bd (M.F.K.); saad@um.edu.my (S.M.)

Abstract: The uses of grid-connected photovoltaic (PV) inverters are increasing day by day due to the scarcity of fossil fuels such as coal and gas. On the other hand, due to their superior efficiency, lower cost, smaller size, and lighter weight when compared to inverters with transformers, transformerless inverters for low-voltage single-phase grid-tied photovoltaic (PV) systems have recently attracted more interest. However, there are some specific challenges, especially leakage current issues, which must be adequately addressed to ensure the safety standards of the grid codes. A variety of topologies has been presented in the literature to eliminate the leakage current using the decoupling or clamping technique. However, choosing an appropriate topology after comparison is challenging because each topology has a unique set of parameters. In this paper, the authors have selected a common set of parameters and simulated all the selected eighteen well-known topologies in MATLAB/Simulink to fairly analyze and compare their common mode characteristics and other output parameters. In addition, the power loss distribution of every switch of each of the eighteen topologies was calculated and presented to better understand the insight of the topologies.

Keywords: AC decoupling; DC decoupling; grid-connected inverter; leakage current; mid-point clamping; solidly clamping; total common mode voltage; transformerless inverter

check for updates

Citation: Kibria, M.F.; Elsanabary, A.; Tey, K.S.; Mubin, M.; Mekhilef, S. A Comparative Review on Single Phase Transformerless Inverter Topologies for Grid-Connected Photovoltaic Systems. *Energies* **2023**, *16*, 1363. https://doi.org/10.3390/en16031363

Academic Editor: Md Rasheduzzaman

Received: 28 November 2022
Revised: 15 January 2023
Accepted: 17 January 2023
Published: 28 January 2023

Copyright: © 2023 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https://creativecommons.org/licenses/by/4.0/).

1. Introduction

Photovoltaic (PV) solar panels are now the most promising source of renewable energy. This source is now extensively used around all over the world. Solar energy installation is expected to cross the terawatts level globally by 2022 [1]. Better performance, reduced expenses, and lower weight are just a few of the benefits of a solar PV system [2]. According to the 2021 annual report of the International Energy Agency-Photovoltaic Power Systems Program (IEA-PVPS) [3], China and the USA contributed 45.6% of the total installed PV capacity of 767.2 GW globally up to 2020. Solar PV system output power, on the other hand, is intermittent and heavily reliant on the irradiance and temperature of solar systems. In solar PV systems, a cascaded inverter can provide maximum power point tracking (MPPT) and control the dc-link voltage. A power inverter is used in a solar system to convert the dc power taken from PV modules into equivalent ac power for an ac load. The grid-tied inverter links PV modules to the electricity grid, and the magnitude of the inverter's output voltage and frequency varies depending on grid conditions [4–8].

In comparison to grid-connected PV systems, the percentage of standalone PV power is relatively low [9]. The PV power can be integrated into the grid in two ways: using

a transformer or without a transformer. When the transformer is used with an inverter, galvanic isolation is developed between the PV and the grid. However, the system is bulky due to the use of a transformer. The other technique is to use an inverter without a transformer, which is called a transformerless inverter. There are two ways to connect this transformerless inverter to the grid: one is a single-stage structure, and the other is a two-stage structure. The single-stage structure and two-stage structure are shown in Figure 1. Transformer-less grid-tied inverters have emerged as a sensible future industrial choice for solar power generating systems in the scale of low to medium due to a number of advantages such as reduced inverter cost, higher conversion efficiency, and smaller size/weight [10–14].

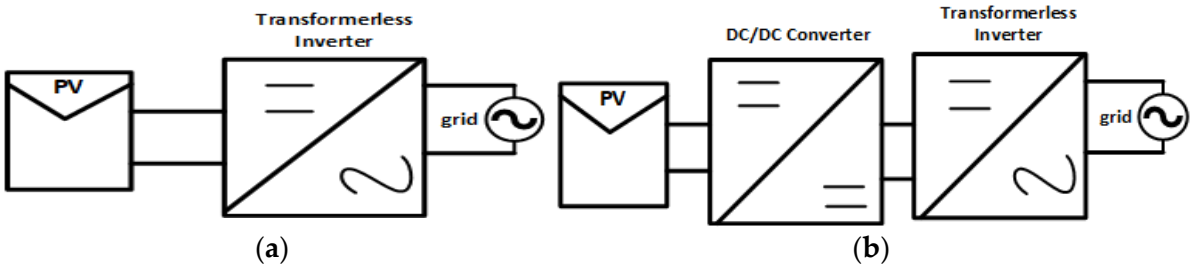


Figure 1. Structure of transformerless inverter: (**a**) single stage; (**b**) two-stage.

There are some challenges to it despite its many benefits. One of these is the leakage current that passes through the electrical grid and the PV panels' parasitic capacitor [4–9], which results in grid current harmonics, electromagnetic interference, and device losses, all of which increase grid current ripple and can cause safety problems such as electric shock [15–22].The total harmonic distortion (THD), a steady state disturbance that affects the power quality in low voltage networks [23], is the other concern. THD has a detrimental impact on various grid-connected equipment, including the operation of motors and electronic devices [24]. Additionally, harmonic distortion lowers the efficiency and reliability of power networks [25].

There are some grid codes and standards provided by different concerned authorities that must be followed by any inverter connected with the grid [26–35]. As the leakage current issue is crucial due to the absence of transformer galvanic isolation, to reduce the leakage current, numerous topologies have been proposed. Two main techniques have been employed to address this issue. They are decoupling and clamping. The common mode behavior of transformerless inverters has been improved using DC or AC decoupling techniques in [36–45]. The mid-point clamping technique has been employed to stabilize the total common mode voltage in [46–51]. Using the solidly clamped topology, transformerless inverters' common mode performance was enhanced in [52–60]. Keeping the value as constant as possible or lowering the total common mode voltage value are the two basic ways to reduce leakage current [61–66]. The majority of solidly clamped topologies [52–60] may keep the total common mode voltage at zero or, at the very least, constant values, which reduces leakage current. However, they require special arrangements for a solid connection between the negative terminals of the grid and the PV. The total common mode voltage can be clamped to a nearly constant value using the topologies based on mid-point clamping [46–51], but they cannot completely prevent the flow of leakage current on the zero voltage state. Zero state decoupled topologies [36–45] can prevent leakage current during the zero state, but they cannot maintain a constant total common mode voltage.

The overall analysis and comparison were made in some review papers [67–71] in different ways. In this paper, a critical review of all the topologies based on common mode behavior was performed. Eighteen well-known topologies based on the same parameters for fair comparison were simulated by the authors after being divided into three primary categories, and they were then compared and their results examined. In addition, the loss distribution across different switches, and the maximum efficiency of all the selected

topologies were calculated for better understanding. The paper's novel contribution is as follows:

- Comparing performance indicators based on simulation results using a common set of simulation parameters.
- Highlighting the switching loss and conduction loss of each switch in each topology using a common set of switches that depicts the advantages and disadvantages of each topology in terms of loss distribution.

The rest of the paper is organized as follows: Common mode behavior, grid requirements, and loss analysis related to transformerless inverters are discussed in Section 2. Section 3 includes the classification, analysis, and simulation results of common mode behavior of all the selected well-known topologies. Comparative analysis, discussion, and future trends are presented in Section 4. Finally, Section 5 concludes the paper.

2. Common Mode Behavior, Grid Requirements, and Loss Analysis

2.1. Common Mode Behavior of TransformerlessInverter

Figure 2 shows the parts of a single phase grid-connected PV system with a transformerless inverter. When a transformerless inverter is connected to the PV and the grid, the leakage current is its primary concern. The leakage current flowing path is identified in Figure 3. The output terminals, A and B, of the transformerless inverter generate the pulsed voltage source V_{AN} and V_{BN}, respectively. They are the main sources of leakage current that flows through the grid to the PV that is shown in Figure 4. The effect of filter inductance remains active, but the effect of the filter capacitor and grid may be neglected [72,73]. Then the final common mode model is shown in Figure 5. The total common mode voltage (V_{tCM}) is the final combined source of leakage current (I_{LC}) that flows through the filter inductance and parasitic capacitance (C_{PV}) of the PV.

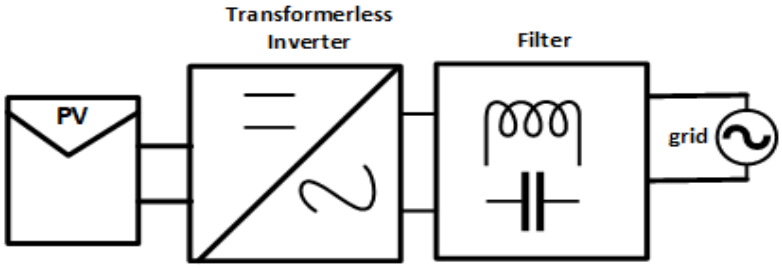


Figure 2. Single-phase grid-connected PV systems with transformerless inverter.

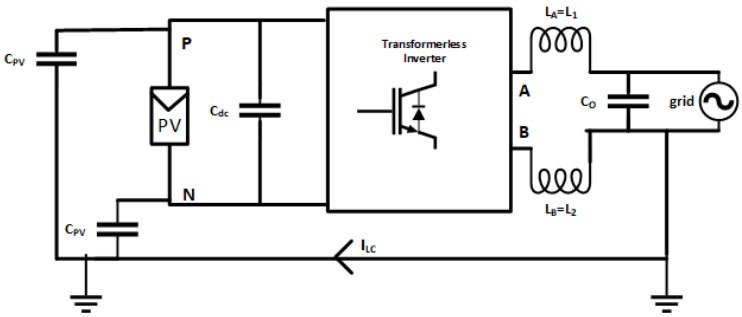


Figure 3. Primary common mode model of single-phase grid-connected PV with transformerless inverter.

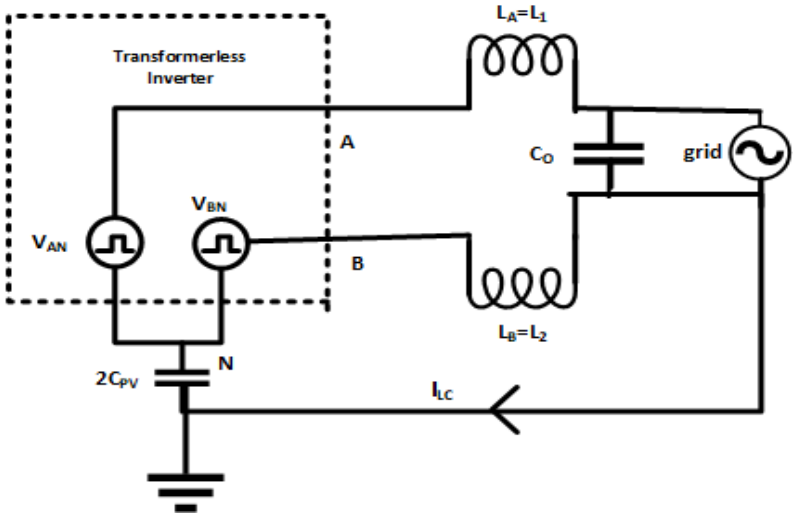


Figure 4. Simplified common mode model of single-phase grid-connected PV with transformerless inverter.

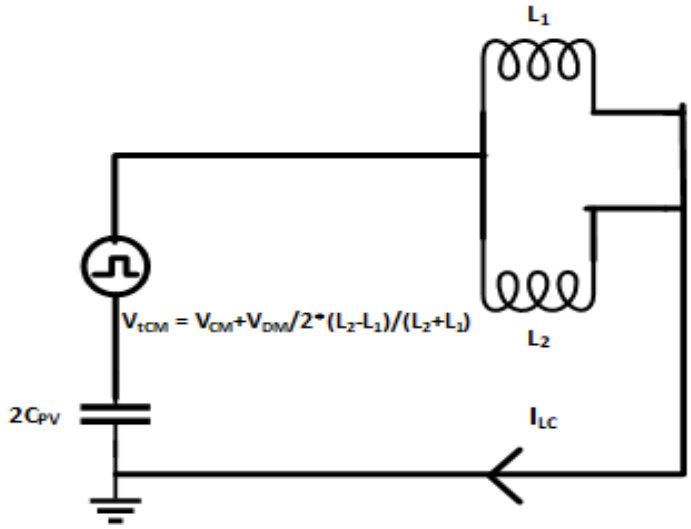


Figure 5. Final common mode model of single-phase grid-connected PV with transformerless inverter.

The common mode voltage (V_{CM}) and differential mode voltage (V_{DM}) can be defined as [17,72–81]

$$V_{CM} = \frac{V_{AN} + V_{BN}}{2} \quad (1)$$

$$V_{DM} = V_{AN} - V_{BN} \quad (2)$$

Rearranging (1) and (2), V_{AN} and V_{BN} can be expressed, respectively, in terms of V_{CM} and V_{DM}:

$$V_{AN} = V_{CM} + \frac{V_{DM}}{2} \quad (3)$$

$$V_{BN} = V_{CM} - \frac{V_{DM}}{2} \quad (4)$$

Now, if the two sources are converted into a single source of V_{tCM}, then the total common mode voltage is

$$V_{tCM} = V_{CM} + \frac{V_{DM}}{2}\frac{L_B - L_A}{L_A + L_B} \quad (5)$$

where, L_A and L_B are the filter inductors connected to the A and B terminals of the inverter, respectively.

If $L_A = L_B$, then Equation (5) becomes [49]

$$V_{tCM} = V_{CM} = \frac{V_{AN} + V_{BN}}{2} \quad (6)$$

However, if $L_B = 0$, then Equation (5) can be written as

$$V_{tCM} = V_{CM} - \frac{V_{DM}}{2} \quad (7)$$

In this paper, the total common mode voltage (V_{tCM}) was generated in the MATLAB/Simulink environment using Equations (6) and (7) considering the design of the filter.

2.2. Grid Requirements

Different types of grid codes and standards are recognized globally. In the case of transformerless inverters, the leakage current is the main concern. The standard called VDE 0126-1-1 [26] for the leakage current issue is shown in Table 1. From this standard, the PV system with the transformerless inverter must discontinue its service if the leakage current value of 100 mA can persist up to 0.04 s.

Table 1. Leakage current values and their corresponding disconnection times listed in the VDE 0126-1-1 standard [26].

Leakage Current Value (mA)	Disconnection Time (s)
30	0.3
60	0.15
100	0.04

The other issues related to the grid-connected system, i.e., the upper limit of THD, the DC current injection limit, the grid frequency limit, and the power factor requirement covered by different standards originated by different countries, are shown in Table 2 [19,27,28,30–35,82–84]. The THD limit of all standards is below 5%, but the DC current injection limit and the power factor requirement are not identical. The minimum DC current injection limit is either 0.25% of the rated output current or 0.22 ampere, corresponding to a 50 W half-wave rectifier. The power factor must be greater than or equal to 0.8 if the PV system can maintain at least a minimum standard.

Table 2. Grid codes and grid-connected PV system standards [19,27,28,30–35,82–84].

Standard Name and Origin	(THD Limit; Grid Frequency Limit in Hz; Power Factor Limit; DC Current Injection Limit)
IEEE 1547 [27], USA (IEEE)	(<5%; 57 to 60.5; 0.9–0.97; <0.5% of rated value of output current)
IEEE 929-2000 [30], USA (IEEE)	(<5%; 59.3 to 60.5;>0.85; <0.5% of rated value of output current)
IEC 61727 [82], Swiss (IEC)	(<5%; 49 to 51;>0.90; <1% of rated value of output current)
AS4777 [83–85], Australia	(<5%; 48 to 52; 0.8–0.95; <0.5% of rated output current/phase)
EN 61000-3-2 [32], England	(<5%; 47.5 to 50.2; NA; <0.22 A corresponding to a 50 W half wave rectifier)
EREC G83 [31], England	(<5%; 49 to 51; 0.95; 0.25% of AC current rating/phase)
VDE 4105 [28], Germany	(<5%; 47.5 to 51.5; 0.89–0.95; <1 A; maximum trip time 0.2 s)
BDEW [33], Germany	(<5%; 47.5 to 51.5(−5% to +3%); 0.95; NA)
GB/T 19964-2012 [34], China	(<5%; 48 to 50.5; 0.95; <1% of rated output current)
JEAC 9701-2012 [35], Japan	(<5%; 47.5 to 51.5 (Eastern Japan)/57 to 61.8 (Western Japan); 0.9–0.95; NA)

2.3. Loss Analysis

In PV systems, switching loss and conduction loss are the two main types of losses. In practical cases, when an IGBT operates, a certain voltage called saturation voltage ($V_{CE(SAT)}$) drops across this switch. Hence the conduction loss across the IGBT can be calculated by [49,76,79–81]

$$P_{CONIGBT} = V_{CE(SAT)} I_C D \tag{8}$$

where, I_C = on state current, and D = duty cycle.

When a diode operates, a certain voltage called saturation voltage V_F drops across this switch. Hence the conduction loss across the diode can be calculated by [49,76,79–81]

$$P_{CONDIODE} = V_F I_F D \tag{9}$$

where, I_F = on state current, and D = duty cycle.

In the case of unipolar SPWM, when the switch is operated on a switching frequency, and the reference signal is greater than the carrier signal, then the duty cycle is

$$D = M \sin \omega t \tag{10}$$

When the carrier signal is greater than the reference signal, then the duty cycle is

$$D = 1 - M \sin \omega t \tag{11}$$

where, M = modulation index. Then total conduction loss is

$$P_{CONTOT} = P_{CONIGBT} + P_{CONDIODE} \tag{12}$$

There are two types of switching losses in IGBT, i.e., turn on switching loss and turn off switching loss. Switching losses can be calculated as follows [86]:

Turn-on switching loss:

$$SW_{ON} = E_{ON} f V_{DC} / V_{DCDATASHEET} \tag{13}$$

Turn-off switching loss:

$$SW_{OFF} = E_{OFF} f V_{DC} / V_{DCDATASHEET} \tag{14}$$

where, E_{ON} and E_{OFF} are the turn on and turn off energy losses, respectively, given in the datasheet, V_{DC} is the actual DC voltage, and $V_{DCDATASHEET}$ is the voltage at which E_{ON} and E_{OFF} are calculated on the datasheet.

Now, the total switching loss of IGBT is

$$SW_{TOT} = SW_{ON} + SW_{OFF} \tag{15}$$

Finally, total loss (TL) in PV systems is

$$TL = SW_{TOT} + P_{CONTOT} \tag{16}$$

In this paper, for calculating the loss across each switch and efficiency, the IGBT called IKW30N65ET7 and the diode called IDC08D120T6M were used.

3. Classification and Analysis of Single Phase Transformerless Inverters

In the literature, numerous single-phase transformerless inverter topologies have been proposed. However, there are some topologies from the beginning to now that can be considered the major topologies in this area.

In this paper, eighteen major topologies were selected and classified into three categories. The classification of the topologies is shown in Figure 6. Then all the selected

eighteen topologies were simulated on MATLAB/Simulink software based on the simulation parameters provided in Table 3 for fair comparison and analysis. In this section, circuit structures for each topology are shown along with their benefits and drawbacks based on simulations of total common mode voltage (V_{tCM}) and leakage current (I_{LC}). The analysis also takes into account the authors' calculated efficiency for each of the topologies they selected. For consistent comparison, IGBTs are treated as switches for all topologies.

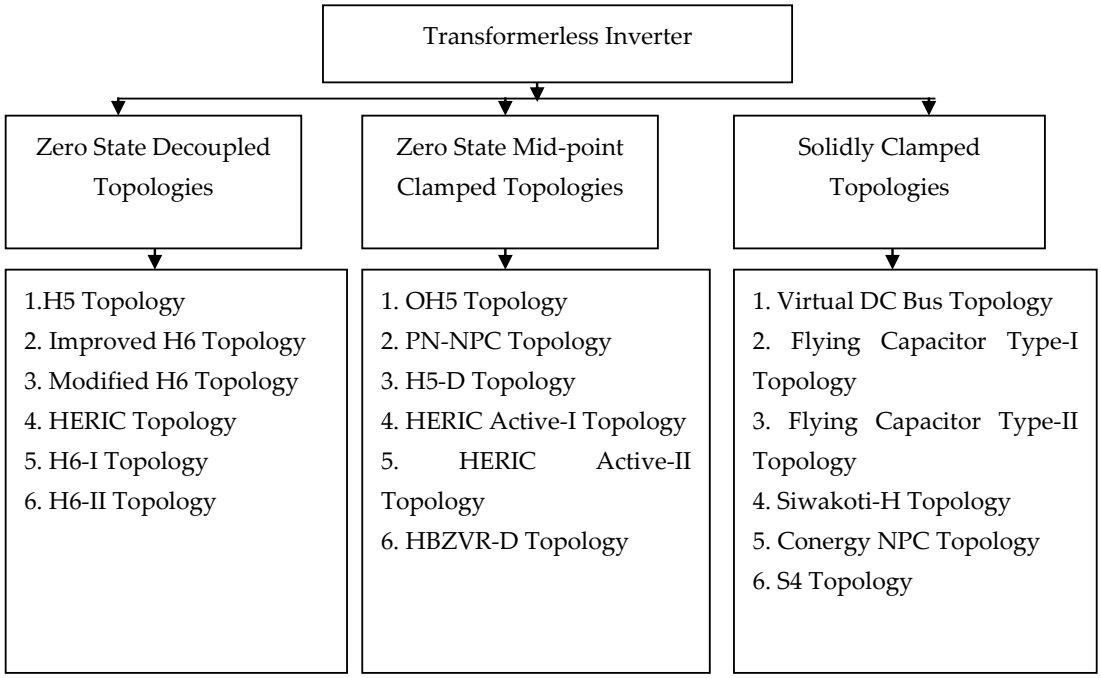


Figure 6. Classification of selected major single-phase transformerless inverter topologies.

Table 3. Parameters for simulations and comparisons.

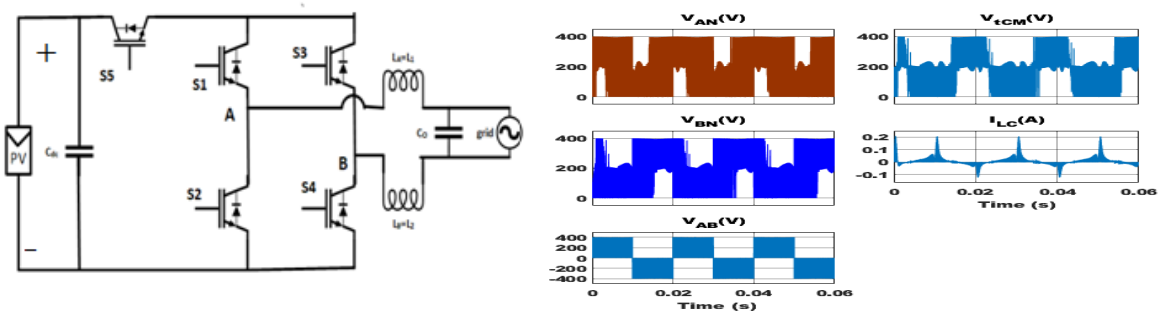
Parameters	Value
AC output voltage	230 V
Line frequency	50 Hz
AC output current	4.34 A
DC input voltage (except Conergy NPC topology)	400 V
DC input voltage (for Conergy NPC topology)	800 V
Output load	53 Ω
Rated power	998.2 W
Switching frequency	24 kHz
DC bus capacitor ($C_{dc} = C_{dc1}/2 = C_{dc2}/2$)	940 µF
Flying capacitor ($C_F = C_1 = C_2$)	1880 µF
Filter capacitor (C_o)	0.68 µF
Filter inductor ($L_1 = L_2$)	2 mH
Parasitic capacitor ($C_{PV} = C_{PV1} = C_{PV2}$)	75 nF
Modulation technique	Unipolar SPWM

3.1. Zero State Decoupled Topologies

In this category, the best performed six topologies were selected for analysis and comparison purposes. They applied the dc or ac decoupling technique at the zero state to improve the common mode behavior. They are as follows:

3.1.1. H5 Topology

The H5 topology is shown in Figure 7a. This topology was first proposed in [36]. Using advanced modulation techniques in [87] and the bidirectional clamping approach in [88], the reactive power control of this topology was further enhanced. The switching loss of the H5 topology was reduced using a soft switching strategy in [89] and new modulation techniques in [90]. In terms of filter settings and switching frequency, the H5 topology design was optimized in [91]. Moreover, the full bridge topology was modified to make the structure of this topology. One extra switch, S_5, was added for disconnecting the grid from the PV side in the zero state of voltage for the purpose of reducing leakage current. The upper two switches of the full bridge were operated on the line frequency, and the lower two switches on the switching frequency. Figure 7b shows the simulation results of this topology. The advantages of the topology were realized, namely, its higher efficiency, a lower rms value of leakage current, and improved THD in the simulation results. However, the simulation results showed that the peak value of the leakage current was around 200 mA, where the rms value was only 13.23 mA, and the total common mode voltage (V_{tCM}) oscillated from 0 V to 400 V.

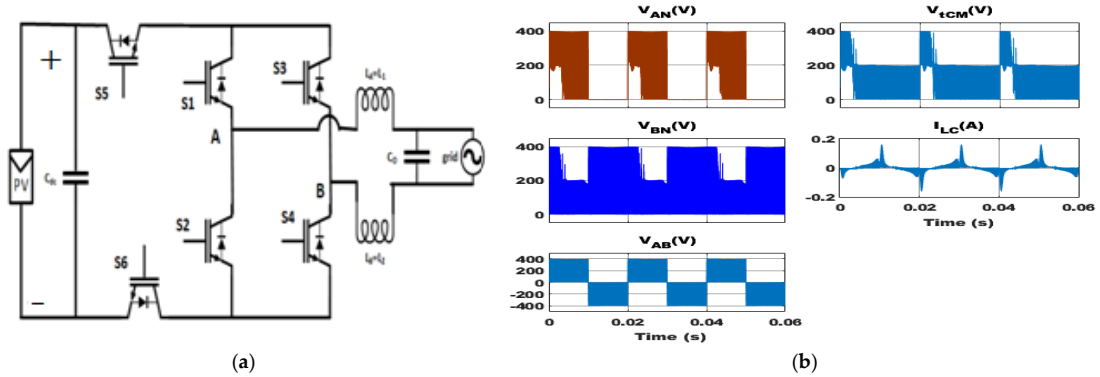


(**a**) (**b**)

Figure 7. H5 topology: (**a**) circuit structure; (**b**) simulation results.

3.1.2. ImprovedH6 Topology

An improved H6 topology was proposed in [37]. In Figure 8a, the topology is shown, and Figure 8b shows the simulation results of this topology. The H5 topology was modified by adding an extra switch in the neutral side of the PV panel to lower the leakage current compared to that of the H5 topology. Here, the left bridge side was operated on the line frequency and right bridge side on the switching frequency. The disconnecting switches were kept on for a half cycle in an alternate manner to avoid more switching loss. The merits of the topology are lower THD and lower leakage current than that of the H5 obtained by simulation. However, the total common mode voltage swung between 0 V and 400 V with a different nature from H5, the peak leakage current was around 150 mA, and the computed efficiency was lower than that of H5 due to the increased number of switches.

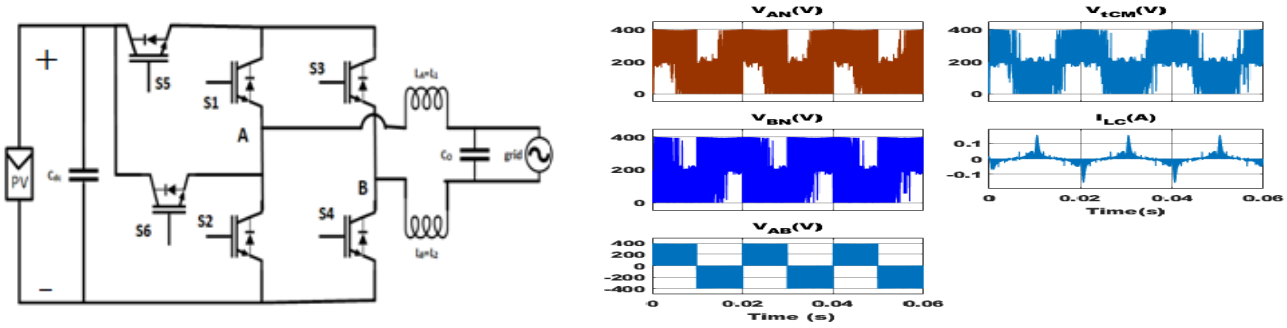


(**a**) (**b**)

Figure 8. Improved H6 topology: (**a**) circuit structure; (**b**) simulation results.

3.1.3. Modified H6 Topology

A modified H6 topology was proposed in [38]. The topology is shown in Figure 9a, and the simulation results of this topology are depicted in Figure 9b. This topology disconnects the PV side from the grid on the free-wheeling mode. The left side of the bridge is operated on the line frequency, and the other four switches are operated on the switching frequency. The nature of the total common mode voltage is evident from the minimal value of leakage current (rms = 12.05 mA, peak = 130 mA), which was somewhat better than that of H5 and the improved H6 topology. The calculated efficiency was higher than the improved H6 but the same as H5. However, in the simulation, the THD was greater than the H5 and the improved H6 topology.

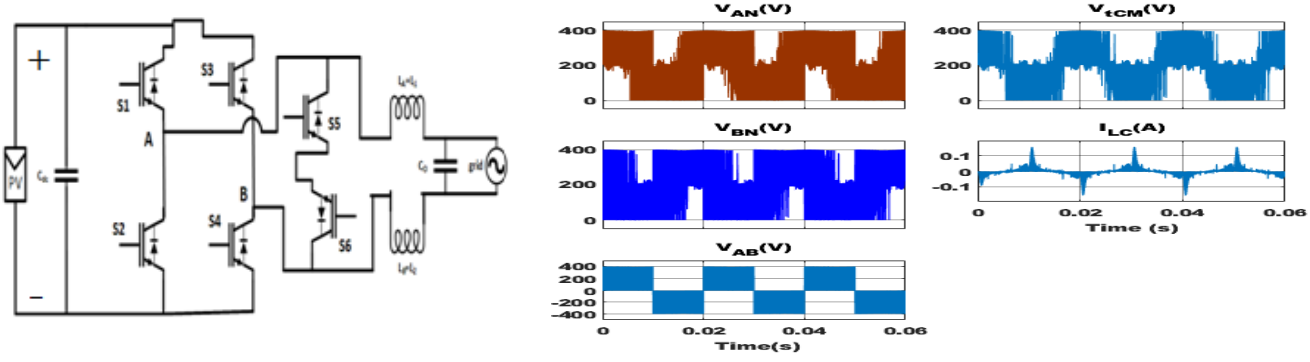


(**a**) (**b**)

Figure 9. Modified H6 topology: (**a**) circuit structure; (**b**) simulation results.

3.1.4. HERIC Topology

The HERIC topology was first proposed in [39]. The topology is drawn in Figure 10a. By utilizing the bidirectional clamping approach in [88] and the advanced modulation technique in [87], this topology's reactive power capacity was further increased. By using soft switching techniques in [92,93], and enhanced modulation techniques in [94], this topology's efficiency was raised. Figure 10b displays the simulation results of this topology. Throughout the entire cycle, a portion of the grid current circled through the S5 and S6, progressively reducing the leakage current. By functioning on the line frequency, the S5 and S6 switches serve as ac decoupling switches in the zero and non-zero states. The other four switches are run on the switching frequency. The excellent operation of S5 and S6 makes the topology the most efficient of all decoupling topologies. The simulation results showed the rms leakage current as 12.09 mA, but the peak value was around 125 mA, and the total common mode voltage was also oscillating. The THD of voltage was higher than that of H5 and the improved H6.

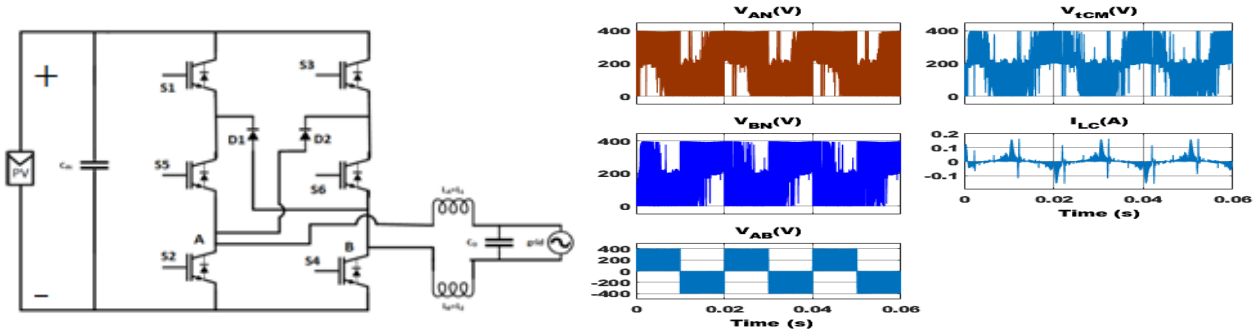


(**a**) (**b**)

Figure 10. HERIC topology: (**a**) circuit structure; (**b**) simulation results.

3.1.5. H6-I Topology

The H6-I topology was primarily proposed in [76]. Figure 11a depicts the topology. Using an advanced hybrid modulation technique, this topology's capacity to inject reactive power was further improved in [95,96]. By using a new control strategy, the common mode voltage behavior was enhanced in [97]. Figure 11b shows the simulation results of this topology. In this topology, S5 and S6 switches were operated on both active and free-wheeling modes. The diodes were used to flow the free-wheeling current. The other switches were operated on switching frequency. The efficiency of this topology was higher than that of the improved H6 topology due to the lesser switching loss of switches S5 and S6. Its rms leakage current was recorded as 14.94 mA, and the peak was about 150 mA. The THD performance was worse than that of other selected zero state decoupled topologies except for H6-II. This topology's total common mode voltage oscillated as well.

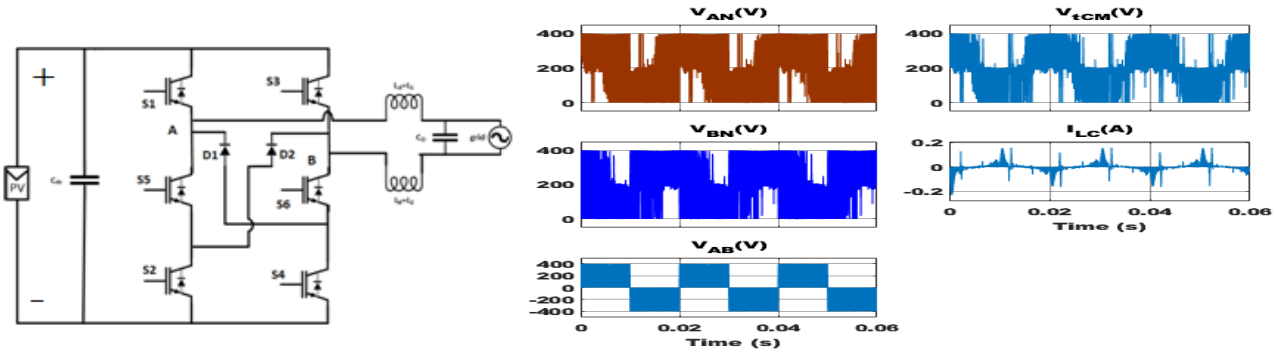


(**a**) (**b**)

Figure 11. H6-I topology: (**a**) circuit structure; (**b**) simulation results.

3.1.6. H6-II Topology

The H6-II topology was firstly proposed in [79]. The topology is sketched in Figure 12a. The reactive power capability was further improved using advanced modulation techniques in [88,98]. Figure 12b shows the simulation results of this topology. S5 and S6 switches were operated in this topology in both active and free-wheeling modes, similar to the H6-I topology. The diodes were used to flow the free-wheeling current. The other switches were operated on the switching frequency. The efficiency of this topology was the same as the H6-I topology due to the same number of switching elements and similar operation principles. The main difference between H6-II and H6-I could be identified from the location of the output terminal of the inverter. Its THD performance and common mode behavior were worse than those of other chosen zero state decoupled topologies.



(**a**) (**b**)

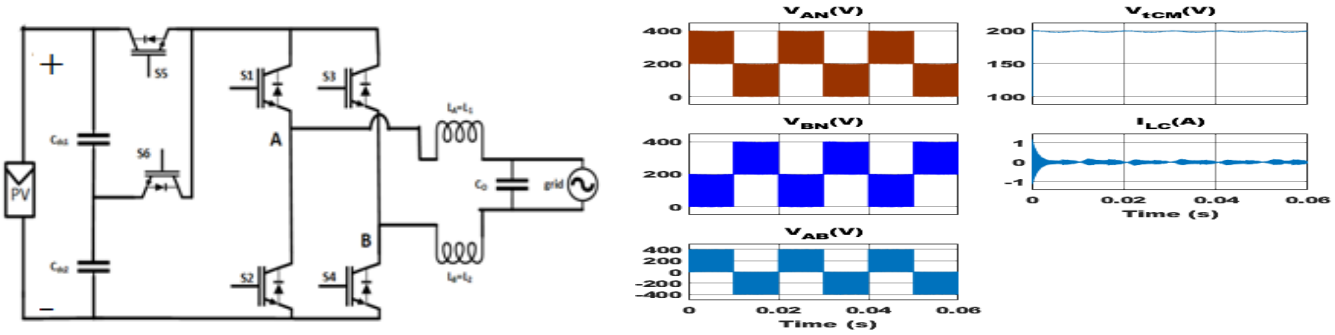
Figure 12. H6-II topology: (**a**) circuit structure; (**b**) simulation results.

3.2. Zero State Mid-Point Clamped Topologies

The top six topologies in this category were selected for analysis and comparison. To enhance common mode behavior, they used the mid-point clamping approach at the zero state. They are as follows:

3.2.1. OH5 Topology

The OH5 topology was proposed in [46]. The topology is shown in Figure 13a, and Figure 13b demonstrates the simulation results of this topology. The upper two switches of the bridge were selected for free-wheeling mode current flowing. The total common mode voltage was now roughly constant at 200 V due to the effective use of switch S6 in the zero state or free-wheeling mode. However, because both the inductor and the capacitor impact leakage current, when the first half of the cycle was ignored, simulation results showed a continuous leakage current of 65.05 mA without a peak. However, this topology's efficiency was the lowest among those in this category due to the running of more switches at the switching frequency.

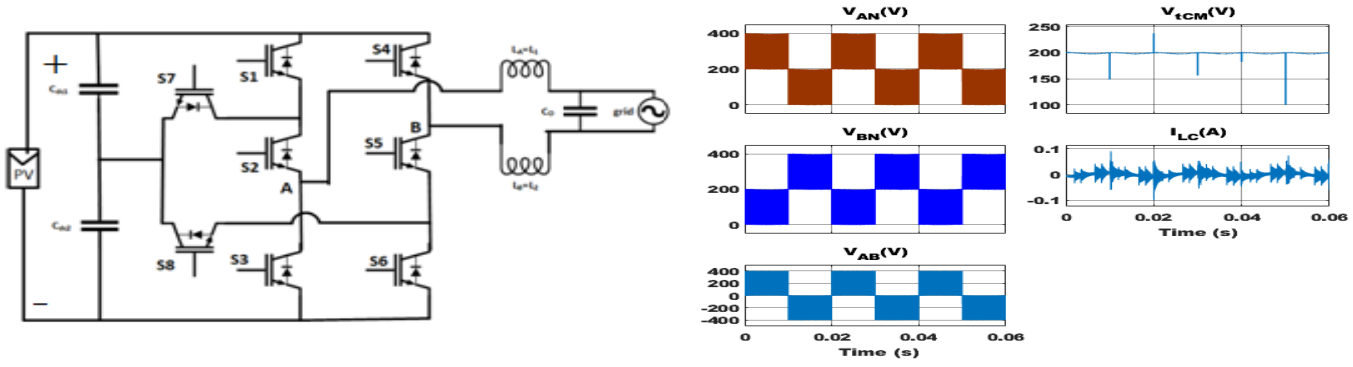


(**a**) (**b**)

Figure 13. OH5 topology: (**a**) circuit structure; (**b**) simulation results.

3.2.2. PN-NPC Topology

The PN-NPC topology was proposed in [47]. Figure 14a depicts a topology drawing, and Figure 14b displays simulation results of this topology. Eight switches were utilized in this topology, four of which were operated on line frequency and the remaining four on the switching frequency. Switches S7 and S8 were selected for the clamping function on the zero state as well as on the active state. When compared to the other zero state mid-point clamping topologies, its THD performance was ranked second. The standard efficiency was maintained by running the four switches on the line frequency. Although only 13.29 mA rms value of leakage current was present, simulation results showed a 100 mA spike at an incorrect clamping point.

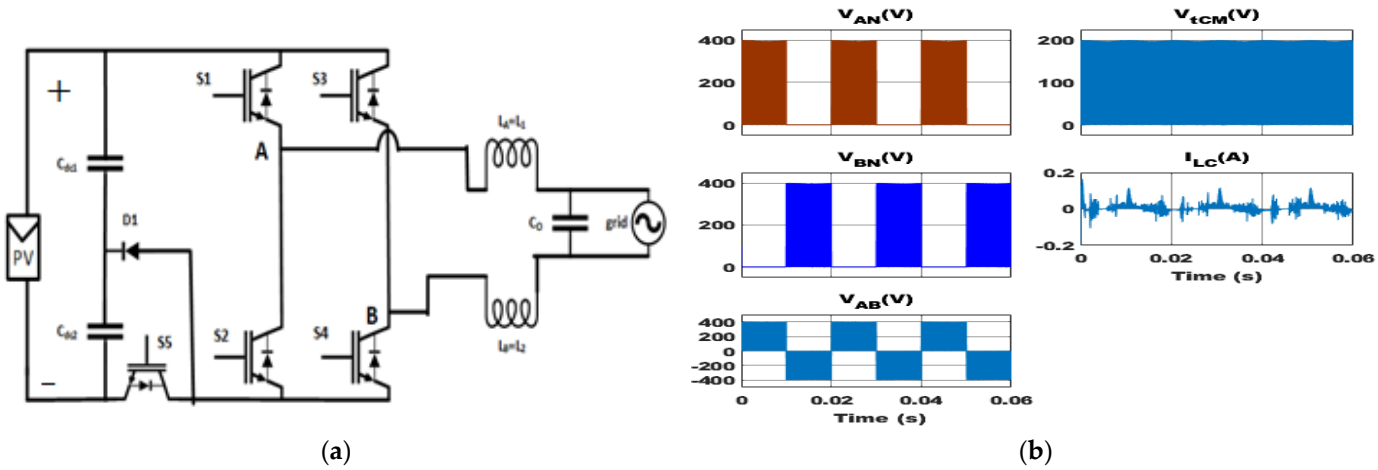


(**a**) (**b**)

Figure 14. PN-NPC topology: (**a**) circuit structure; (**b**) simulation results.

3.2.3. H5-D Topology

The H5-D topology was proposed in [48]. The topology is shown in Figure 15a. Figure 15b shows the simulation results of this topology. In this topology, diode D1 was used for clamping purposes. Switches S2 and S4 were turned on during the free-wheeling mode. Despite not obtaining a single stable common mode voltage, the swing was restricted to 0 V to 200 V. The rms leakage current was 13.88 mA, although simulations showed 100 mA peaks due to incorrect clamping. However, the THD performance was the best among the chosen zero state mid-point clamping topologies. The estimated efficiency was higher than OH5 at 97.3%.

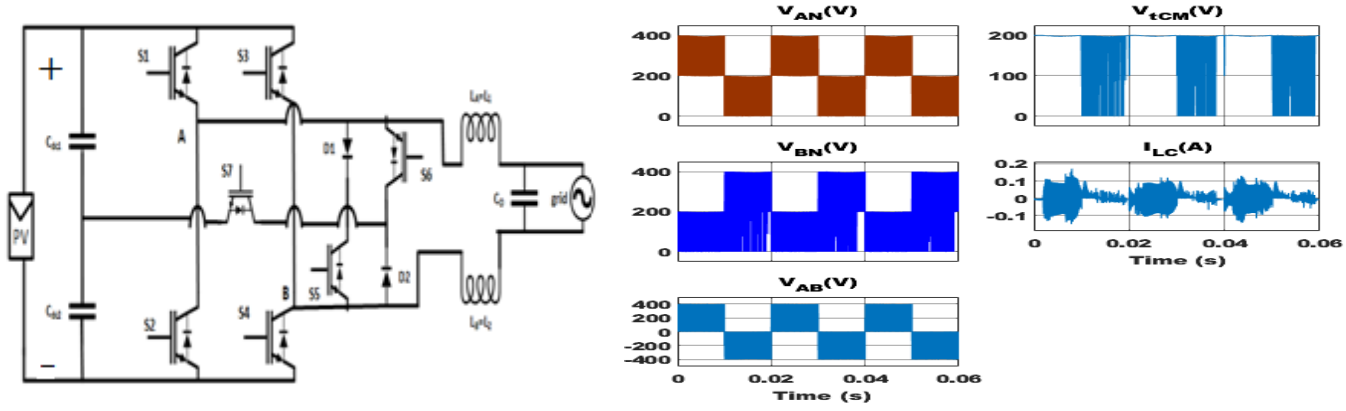


(**a**) (**b**)

Figure 15. H5-D topology: (**a**) circuit structure; (**b**) simulation results.

3.2.4. HERIC Active-I Topology

The HERIC Active-I topology was proposed in [69]. Figure 16a sketches out the topology, and Figure 16b shows the simulation results of this topology. Switch S7 solely clamped the midpoint voltage in the positive half cycle's zero state. S5 and S6 were operated on the line frequency to create an extra free-wheeling path using the ac decoupling technique. The efficiency of this topology was the highest among the selected topologies under this category due to lower conduction losses. The rms leakage current was 41.41 mA, and the peak value was about 120 mA. Because only the positive half cycle was clamped, there was a relatively higher leakage current.

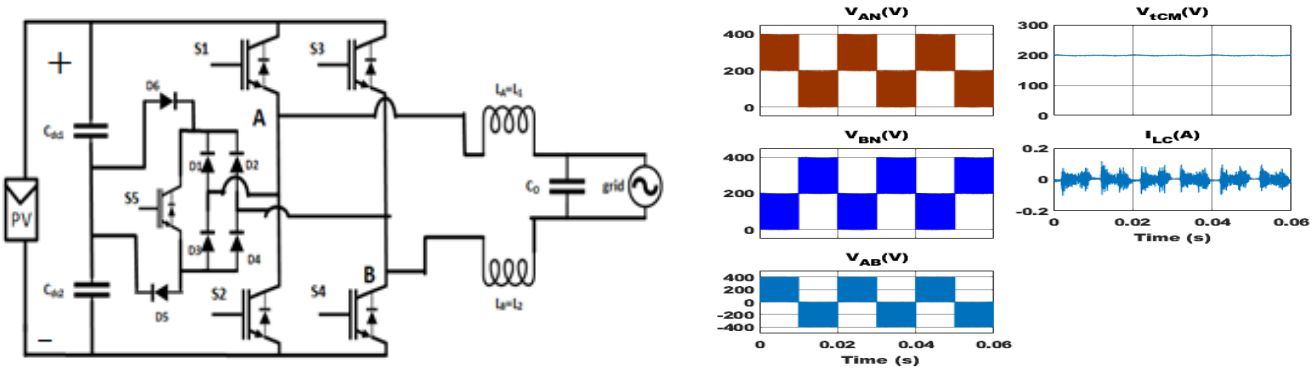


(**a**) (**b**)

Figure 16. HERIC Active-I topology: (**a**) circuit structure; (**b**) simulation results.

3.2.5. HERIC Active-II Topology

The HERIC Active-II topology was proposed in [69]. The topology is shown in Figure 17a, and the simulation results of this topology are depicted in Figure 17b. Switch S7 was used for clamping purposes, and it was operated on the switching frequency on the zero voltage state. For the purpose of ac decoupling, switches S5 and S6 were operated at the line frequency. The efficiency of this topology was higher than that of H5-D and PN-NPC topologies. The leakage current's peak value was restricted to 100 mA, despite the fact that the leakage current rms value was somewhat greater than that of other chosen topologies in this category.

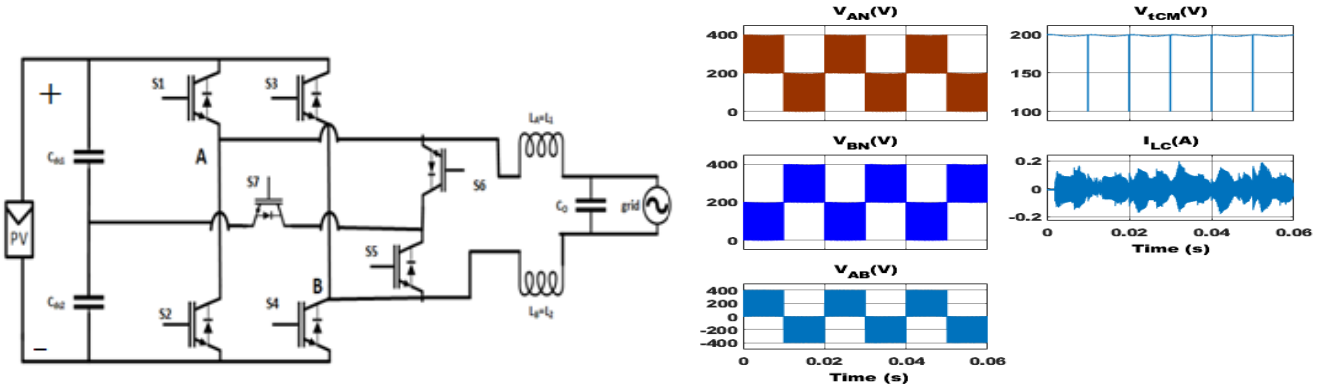


(**a**) (**b**)

Figure 17. HERIC Active-II topology: (**a**) circuit structure; (**b**) simulation results.

3.2.6. HBZVR-D Topology

The HBZVR-D topology was proposed in [49]. Figure 18a shows a drawing of the topology, and Figure 18b shows the simulation results of this topology. Two diodes, D5 and D6, were employed for clamping the mid-point voltage. Switch S5 was used for creating the free-wheeling path during the zero state. The free-wheeling path was made possible by the anti-parallel diodes D1–D4. The rms leakage current was 22.75 mA, and the total common mode voltage was about a constant 200 V. This topology's computed efficiency was 97.6%, which was higher than that of the OH5 and H5-D topologies. However, the leakage current's peak value was about 110 mA.



(**a**) (**b**)

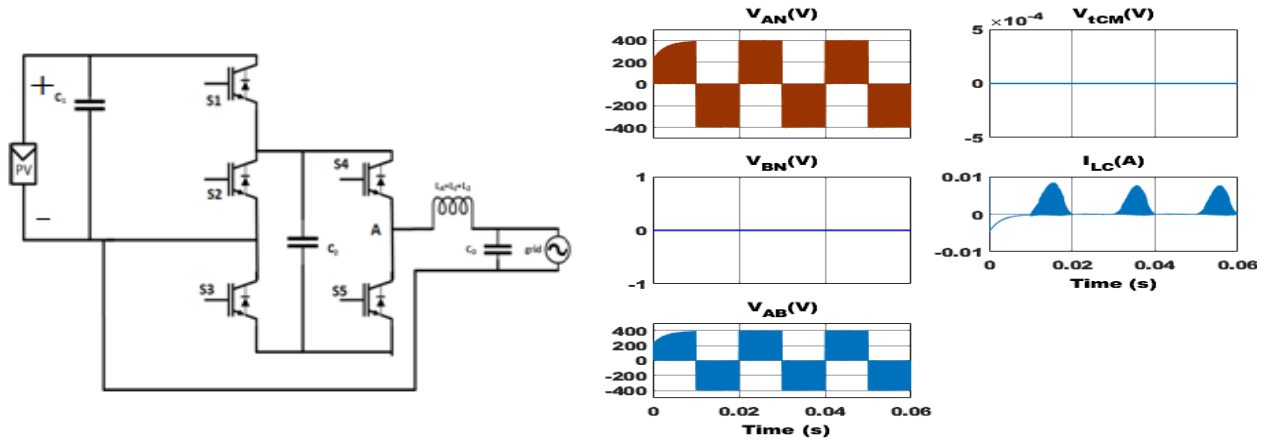
Figure 18. HBZVR-D topology: (**a**) circuit structure; (**b**) simulation results.

3.3. Solidly Clamped Topologies

In this category, the most optimum six topologies were selected for analysis and comparison purposes. They used a solid connection from the grid negative terminal to either the PV neutral or the mid-point of two series dc link capacitors to improve the common mode behavior. They are as follows:

3.3.1. Virtual DC Bus Topology

The Virtual DC Bus topology was proposed in [52]. The topology is shown in Figure 19a, and the simulation results of this topology are sketched in Figure 19b. The capacitor C_2 was charged during the positive half cycle to create a virtual DC bus for the negative half cycle. The S3 and S5 switches were activated during the positive half cycle free-wheeling mode, while the S2 and S4 switches were activated during the negative half cycle free-wheeling mode. This topology's total common mode voltage was about 0 V because the grid's negative terminal was directly connected to the PV side's neutral. The rms leakage current was only 0.75 mA, but the leakage current peak value was roughly 7.5 mA. The efficiency was only 96.8% due to high conduction losses.

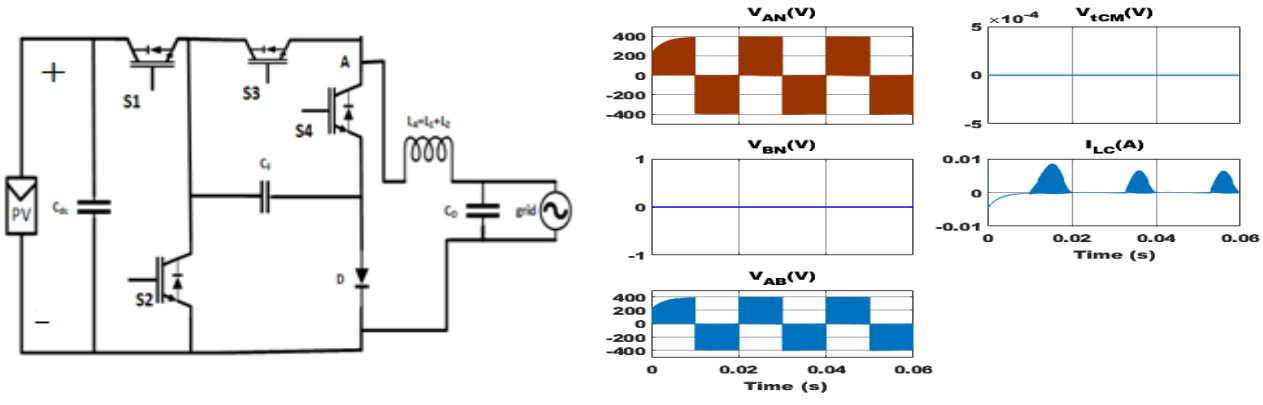


(**a**) (**b**)

Figure 19. Virtual DC Bus topology: (**a**) circuit structure; (**b**) simulation results.

3.3.2. Flying Capacitor Type-I topology

The Flying Capacitor Type-I topology was proposed in [53]. Figure 20a shows a sketch of the topology, and Figure 20b shows the simulation results of this topology. The flying capacitor C_F was charged during the whole positive half cycle, and it acted as the source for the negative half cycle through discharging. Although all switches functioned at the switching frequency, because the length was only half a cycle, switching loss was cut in half. Although capacitor charging caused additional conduction loss, the efficiency was still quite high at 97.2%. Since it is evident from the simulation that the total common mode voltage was set at zero volts, the rms leakage current was only 0.58 mA. However, starting the leakage current's peak value at 8.5 mA, it decreased over time. Furthermore, the output voltage's THD was 4.2%.

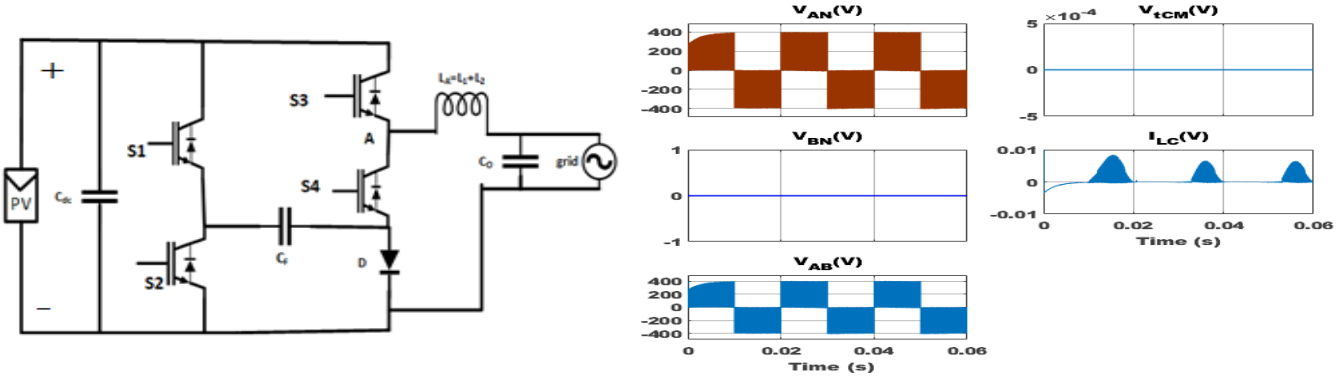


(**a**) (**b**)

Figure 20. Flying Capacitor Type-I topology: (**a**) circuit structure; (**b**) simulation results.

3.3.3. Flying Capacitor Type-II Topology

The Flying Capacitor Type-II topology was proposed in [54]. The topology is drawn in Figure 21a, and the simulation results of this topology are shown in Figure 21b. Throughout the entirety of the positive half cycle, the flying capacitor C_F was charged through switch S1 and diode D. The grid was powered by the charged capacitor C_F during the negative half cycle. To lower the switching loss, switches S1 and S4 were activated during the free-wheeling mode for a half-cycle period on the line frequency and another half-cycle on the switching frequency. The total common mode voltage was confirmed by simulation results to be 0 V, and as a result, the rms leakage current was just 0.58 mA. Although the leakage current's peak value starting from 8 mA diminishes with time. The obtained efficiency of this topology was the same as that of the Flying Capacitor Type-I topology at 97.2%, and the voltage THD was 4.2%.

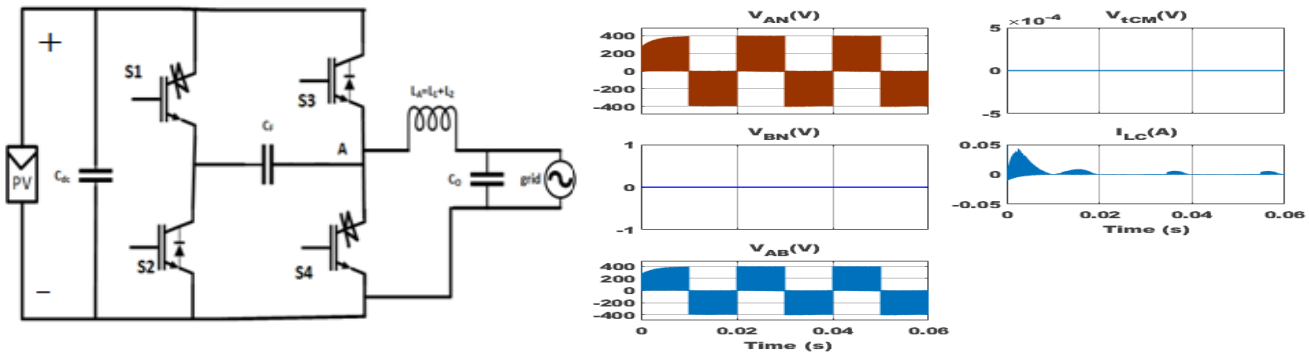


(**a**) (**b**)

Figure 21. Flying Capacitor Type-II topology: (**a**) circuit structure; (**b**) simulation results.

3.3.4. Siwakoti-H Topology

The Siwakoti-H topology was first proposed in [55]. The topology is represented in Figure 22a. The nonlinear behavior of this topology was properly addressed using a discrete-time state feedback control scheme in [99], and using a direct model predictive control scheme in [100]. Figure 22b shows the simulation results of this topology. Two switches called S1 and S4 were reverse blocking IGBT (RB-IGBT), and they were operated on the zero state to charge the flying capacitor C_F. This fully charged capacitor was used as the source of the negative active half cycle. The positive active half cycle was controlled by switch S3. The total common mode voltage was observed as 0 V from the simulation, and hence the rms leakage current value was only 0.47 mA. However, the 40 mA leakage current peak was seen in the first cycle. The computed efficiency was second in this category at 98.1%, and the simulation showed a voltage THD of 4.3%.

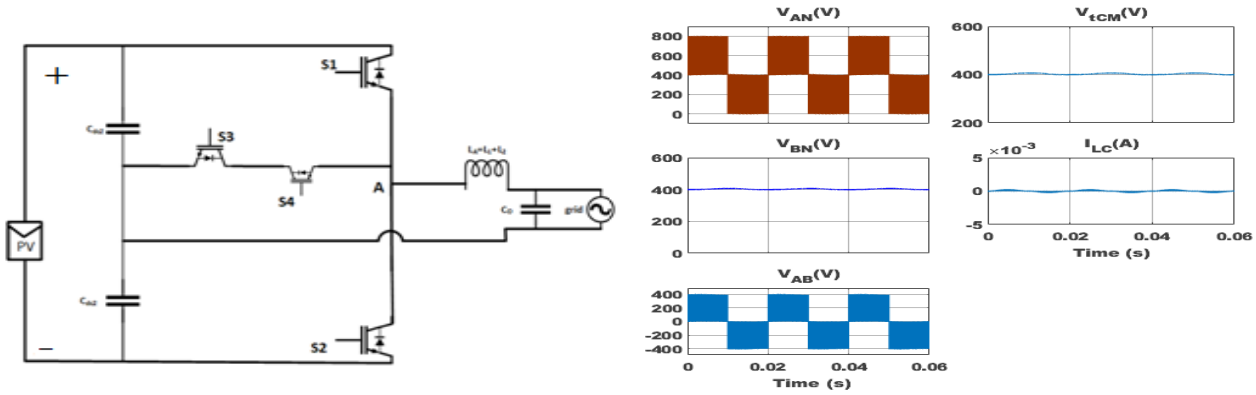


(**a**) (**b**)

Figure 22. Siwakoti-H topology: (**a**) circuit structure; (**b**) simulation results.

3.3.5. Conergy NPC Topology

The Conergy NPC topology was primarily proposed in [56]. The topology is redrawn in Figure 23a. According to switching frequency and filter parameters, this topology with SiC switches was designed optimally in [91]. Figure 23b shows the simulation results of this topology. The negative terminal of the grid was directly attached to the middle point of two equal-series dc link capacitors. To flow the current in the free-wheeling mode, switches S3 and S4 were operated in the zero state in the opposite way. Although the total common mode voltage was about 400 V, nevertheless, the leakage current rms value was limited to 0.14 mA with no noticeable peaks due to its solid connection and constant V_{tCM}. Due to its extremely low conduction loss, this topology had the highest efficiency among those in this category. The voltage THD was also 1%. However, the input voltage requirement of this topology was twice than that of other topologies.

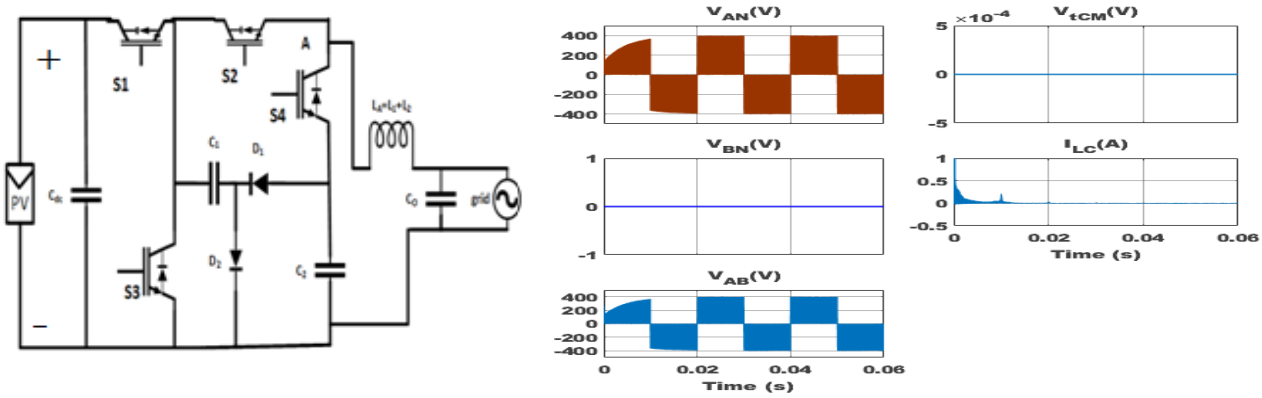


(**a**) (**b**)

Figure 23. Conergy NPC topology: (**a**) circuit structure; (**b**) simulation results.

3.3.6. S4 Topology

The S4 topology was proposed in [57]. Figure 24a depicts the topology, and the simulation results of this topology are depicted in Figure 24b. In the positive half cycle active mode, C_1 charged through diode D_2, and then C_2 charged from the discharge of C_1 through D_1 in the positive zero state. In the negative half cycle, C_2 provided power to the grid. The total common mode voltage was 0 V, and hence the rms leakage current was only 0.56 mA. Because switching frequency was used the majority of the time to run all switches, efficiency was impacted, and the computed efficiency was only 96.2%. Furthermore, compared to other chosen topologies, the voltage THD was worse.



(**a**) (**b**)

Figure 24. S4 topology: (**a**) circuit structure; (**b**) simulation results.

4. Comparative Analysis, Discussion, and Future Trends

Transformerless inverter topologies are categorized into three groups in this paper. MATLAB/Simulink was used for analysis and comparison purposes to simulate a total of 18 topologies, 6from each category, using the parameters shown in Table 3. Using the equations provided in Section 2.3, the loss distribution across all switches, and the maximum efficiency of all topologies were computed. The simulation results of the common mode behavior of each topology were discussed thoroughly in Section 3. In order to compare the topologies fairly, Table 4 was created based on the simulation results, computed efficiency, and physical parameters of the topologies. The loss distribution over each switch of the 18 topologies is shown in Figure 25.

Table 4. Comparison of the selected topologies based on simulation results and physical parameters.

Category	Topology Name	No. of Input Capacitor	Input DC Voltage	Modulation Index	No. of IGBTs	No. of Diodes	No. of Filter Inductors	No. of Filter Capacitors	Simulation Results			Calculated Maximum Efficiency@ 998.2 W
									Total Common Mode Voltage (V_{tCM})	RMS Leakage Current (I_{LC})	THD of Voltage	
Zero state decoupled topologies	H5 [36,87–91]	1	400 V	0.82	5	0	2	1	(0–400) V, Floating	13.23 mA	0.68%	97.8%
	Improved H6 [37]	1	400 V	0.82	6	0	2	1	(0–400) V, Floating	12.77 mA	0.60%	97.1%
	Modified H6 [38]	1	400 V	0.82	6	0	2	1	(0–400) V, Floating	12.05 mA	1%	97.8%
	HERIC [39,87,88,92–94]	1	400 V	0.82	6	0	2	1	(0–400) V, Floating	12.09 mA	1%	98%
	H6-I [76,95–97]	1	400 V	0.82	6	2	2	1	(0–400) V, Floating	14.94 mA	4.9%	97.8%
	H6-II [79,88,98]	1	400 V	0.82	6	2	2	1	(0–400) V, Floating	15.19 mA	5%	97.8%
Zero state mid-point clampedtopologies	OH5 [46]	2	400 V	0.79	6	0	2	1	200 V, Constant	65.05 mA	3.3%	97.2%
	PN-NPC [47]	2	400 V	0.82	8	0	2	1	(100–230) V, Semi-floating	13.29 mA	1.7%	97.4%
	H5-D [48]	2	400 V	0.795	5	1	2	1	(0–200) V, Floating	13.88 mA	1.3%	97.3%
	HERIC Active-I [69]	2	400 V	0.795	7	2	2	1	200 V, Constant (half cycle); (0–200) V Floating (half cycle)	41.41 mA	3.5%	97.8%
	HERIC Active-II [69]	2	400 V	0.79	7	0	2	1	(100–200) V, Semi-floating	71.48 mA	3.7%	97.6%
	HBZVR-D [49]	2	400 V	0.78	5	6	2	1	200 V, Constant	22.75 mA	4%	97.6%
Solidly clamped topologies	Virtual DC Bus [52]	2	400 V	0.775	5	0	1	1	0 V, Constant	0.75 mA	5.1%	96.8%
	Flying Capacitor Type-I [53]	2	400 V	0.782	4	1	1	1	0 V, Constant	0.58 mA	4.2%	97.2%
	Flying Capacitor Type-II [54]	2	400 V	0.782	4	1	1	1	0 V, Constant	0.58 mA	4.2%	97.2%
	Siwakoti-H [55,99,100]	2	400 V	0.80	4	0	1	1	0 V, Constant	0.47 mA	4.3%	98.1%
	Conergy NPC [56,91]	2	800 V	0.815	4	0	1	1	400 V, Constant	0.14 mA	1%	98.2%
	S4 [57]	2	400 V	0.795	4	2	1	1	0 V, Constant	0.56 mA	9.2%	96.2%

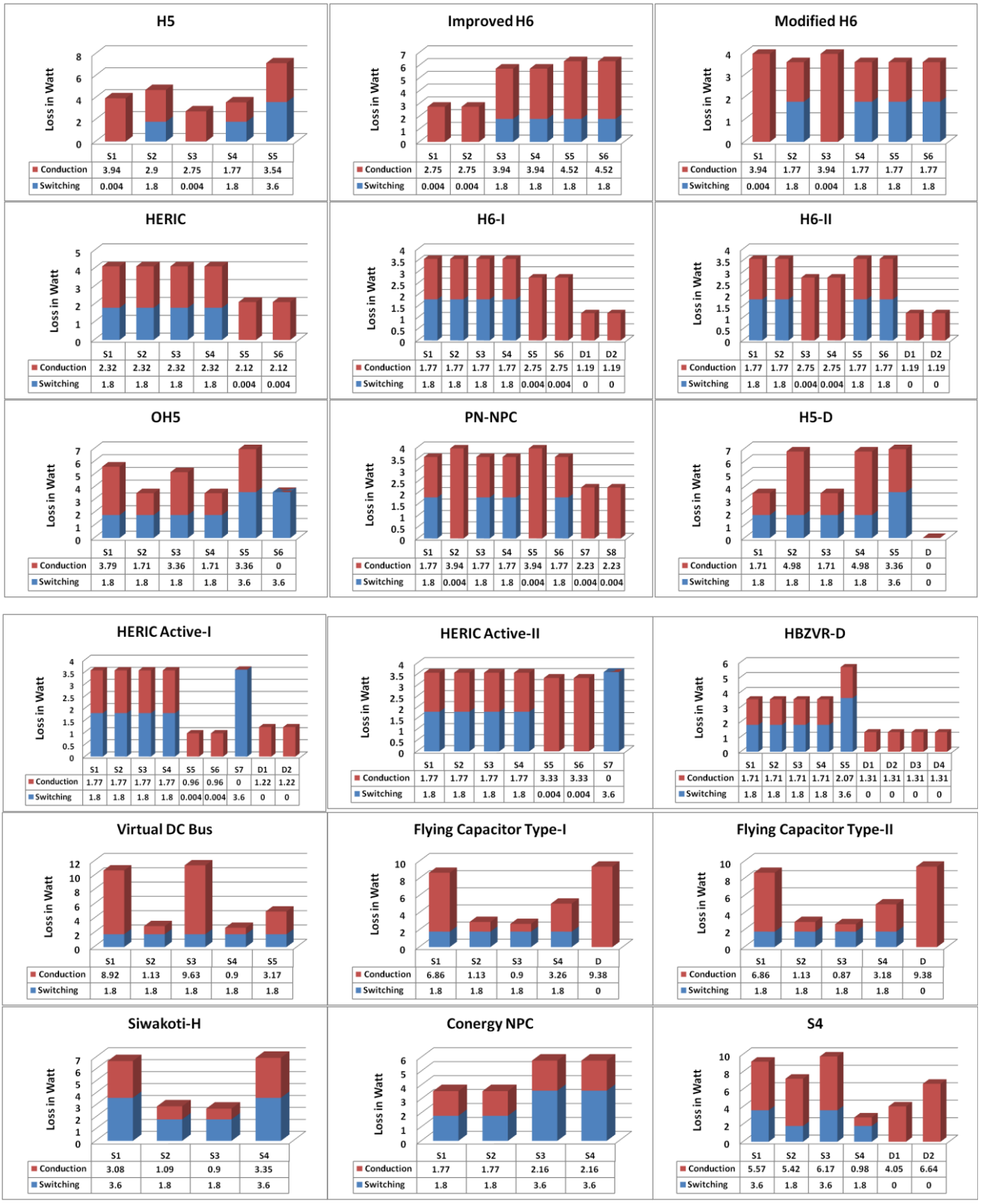


Figure 25. Power loss distribution across each of the switches of all the chosen eighteen topologies for output power of 998.2 W.

In Figure 26, the output power versus efficiency curve for three chosen topologies—one from each category—is displayed.

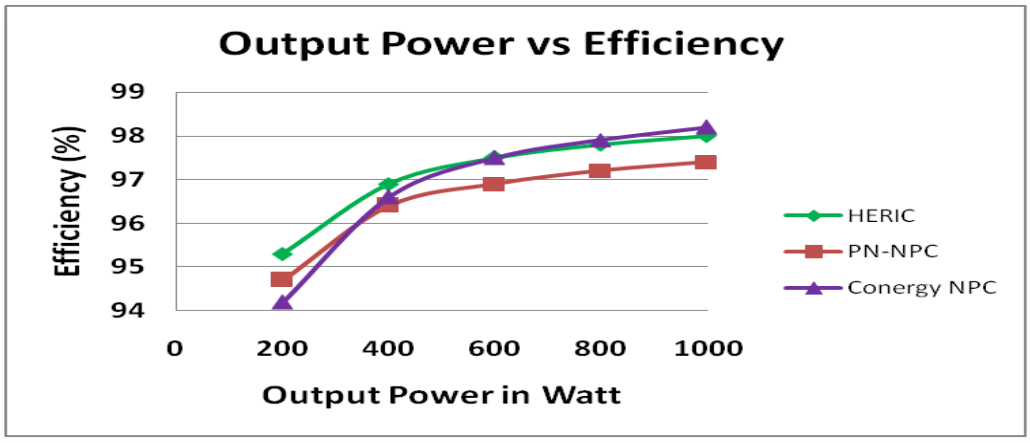


Figure 26. Output power versus efficiency curves for three chosen topologies, one from each category.

In the case of the zero state decoupled topologies category, the circuit structure is comparatively simple due to absence of a clamping branch. The total common mode voltages for all six topologies fluctuate between 0 V and 400 V. Under this category, the HERIC topology displays the highest efficiency. Even though this group's rms leakage current ranges from 12 to 15 mA, the concerns associated with their peak leakage current are detailed in Section 3. In comparison to other topologies in this group, the loss distribution across various switches is best in modified H6. HERIC can be selected as this group's best topology after considering all the factors, even though H5 performs well.

In the case of zero state mid-point clamped topologies, the leakage current's peak value is comparatively smaller than that of zero state decoupled topology, but the topological arrangement is more complex. The constant total common mode voltages are guaranteed by the OH5 and HBZVR-D topologies. Other topologies in this group have semi-floating or partially total constant common mode voltages. Although this group's average rms leakage current is higher than that of the zero state decoupled topologies group, the average peak value of leakage current of this category is lower due to the mid-point clamping technique. HERIC Active-I is the most efficient topology in this group in terms of efficiency, and PN-NPC performs best in terms of leakage current.

HERIC Active-II is best in terms of loss distribution among switches. However, PN-NPC can be regarded as this group's best topology when all the factors are taken into account.

All solidly clamped topologies guarantee the rms leakage current less than 1 mA, but the topological construction is the most complicated, since a solid connection between the electrical grid and the PV is necessary. Due to a strong solid connection between the grid and the PV negative terminal, the total common mode voltage of this category, with the exception of Conergy NPC topology, is zero. In the Conergy NPC topology, the negative terminal of the grid side is connected to the halfway point of two series dc link input capacitors; therefore, the topology's total common mode voltage is not zero volts. However, because of the strong connection between the PV side and the grid side and the constant V_{tCM}, this topology only has a leakage current of 0.14 mA. Siwakoti-H operates most effectively in this group for 400 V input. Conergy NPC topology, however, can be regarded as the best topology in this category when all factors are taken into account.

However, choosing the best topology among the three groupings is challenging. The solidly clamped topologies perform the best regarding the leakage current problem, but the circuit configuration and control system are more complicated than those of other groups. Each group has unique benefits and drawbacks. Thus, the optimum topology may be selected based on requirements and consideration of all parameters.

Future research on various control strategies that can be used with the major topologies discussed in the paper to enhance reactive power control has significant opportunities. Different advanced modulation schemes can be suggested for improving the efficiency

of the selected topologies. Using novel or improved modulation techniques will lower the leakage current and total harmonic distortion. Additionally, to further improve the reliability of the inverter system, fault-tolerant techniques can be incorporated into the already-existing topologies.

5. Conclusions

Transformerless inverters are the choice of the future due to their many benefits, such as minimal weight, low cost, and outstanding efficiency. However, there are certain obstacles to overcome. Leakage current and complexity in topology and control systems are two. In this paper, every topology is extensively simulated using a common set of parameters to evaluate and fairly examine its common mode characteristics and other output characteristics.

In Figure 25, the loss distribution across each switch is also displayed to highlight the topologies' strengths and weaknesses in terms of loss spread. Table 4 offers a comparative analysis of all selected topologies of single-phase transformerless inverters, especially in regard to their key properties based on simulation and theoretical calculation, as a summary of this evaluation. Additionally, based on simulation and theoretical research, the top three topologies, one from each category, were chosen. The authors hope that this review will be useful for researchers, engineers, manufacturers, and users related to the academy and industry as a resource on transformerless grid-connected PV inverters. In the future, each selected topology of this paper can be verified experimentally based on the same parameters for best understanding of the insights of the topologies.

Author Contributions: Conceptualization, M.F.K., A.E. and S.M.; methodology, M.F.K., A.E., K.S.T. and M.M.; software, M.F.K. and A.E.; validation, M.F.K., K.S.T., M.M. and S.M.; formal analysis, M.F.K., A.E, M.M. and S.M.; investigation, M.F.K., A.E., K.S.T. and S.M.; resources, K.S.T., M.M. and S.M.; data curation, M.F.K., A.E. and K.S.T.; writing—original draft preparation, M.F.K.; writing—review and editing, A.E., K.S.T., M.M. and S.M.; visualization, M.F.K. and S.M.; supervision, K.S.T., M.M. and S.M.; project administration, K.S.T., M.M. and S.M; funding acquisition, K.S.T., M.M. and S.M.; All authors have read and agreed to the published version of the manuscript.

Funding: The authors would like to thank the Ministry of Higher Education, Malaysia, for providing financial support under the Large Research Grant Scheme (LRGS): LRGS/1/2019/UKM/01/6/3 and the Universiti Tenaga Nasional grant no. IC6-BOLDREFRESH2025 (HCR) under the BOLD2025 Program.

Data Availability Statement: Not Applicable.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Chamarthi, P.K.; El Moursi, M.S.; Khadkikar, V.; Al Hosani, K.H.; El-Fouly, T.H.M. Novel Step-Up Transformerless Inverter Topology for 1-Φ Grid-Connected Photovoltaic System. *IEEE Trans. Ind. Appl.* **2021**, *57*, 2801–2815. [CrossRef]
2. Yang, Y.; Blaabjerg, F. Overview of Single-Phase Grid-Connected Photovoltaic Systems. *Electr. Power Components Syst.* **2015**, *43*, 1352–1363. [CrossRef]
3. Masson, G.; Kaizuka, I.; Bosch, E.; Lindahl, J.; Blokken, E. *Trends 2021 in Photovoltaic Applications*; IEA PVPS Task 1; IEA: Paris, France, 2021; ISBN 9783906042916.
4. Khan, M.N.H.; Siwakoti, Y.P.; Scott, M.J.; Li, L.; Khan, S.A.; Lu, D.D.C.; Barzegarkhoo, R.; Sidorski, F.; Blaabjerg, F.; Hasan, S.U. A Common Grounded Type Dual-Mode Five-Level Transformerless Inverter for Photovoltaic Applications. *IEEE Trans. Ind. Electron.* **2021**, *68*, 9742–9754. [CrossRef]
5. Islam, M.; Mekhilef, S. An Improved Transformerless Grid Connected Photovoltaic Inverter with Reduced Leakage Current. *Energy Convers. Manag.* **2014**, *88*, 854–862. [CrossRef]
6. Lopez-Erauskin, R.; Gonzalez, A.; Petrone, G.; Spagnuolo, G.; Gyselinck, J. Multi-Variable Perturb and Observe Algorithm for Grid-Tied PV Systems with Joint Central and Distributed MPPT Configuration. *IEEE Trans. Sustain. Energy* **2021**, *12*, 360–367. [CrossRef]
7. Xiao, H. Overview of Transformerless Photovoltaic Grid-Connected Inverters. *IEEE Trans. Power Electron.* **2021**, *36*, 533–548. [CrossRef]
8. Xuan, Z.; Dong, J.; Jianan, C.; Zewei, S.; Qiao, L. Leakage Current Suppression with Capacitor Voltage Control of Three-Level Flying Capacitor Grid-Connected Inverters. *IEEE Trans. Ind. Electron.* **2022**, *69*, 2191–2201.

9. IRENA. *RE Thinking Energy 2017: Accelerating the Global Energy Transformation*; International Renewable Energy Agency: Abu Dhabi, United Arab Emirates, 2017.
10. Sonti, V.; Jain, S.; Bhattacharya, S. Analysis of the Modulation Strategy for the Minimization of the Leakage Current in the PV Grid-Connected Cascaded Multilevel Inverter. *IEEE Trans. Power Electron.* **2017**, *32*, 1156–1169. [CrossRef]
11. Dutta, S.; Debnath, D.; Chatterjee, K. A Grid-Connected Single-Phase Transformerless Inverter Controlling Two Solar PV Arrays Operating under Different Atmospheric Conditions. *IEEE Trans. Ind. Electron.* **2018**, *65*, 374–385. [CrossRef]
12. Gunsal, I.; Stone, D.A.; Foster, M.P. Suppressing Leakage Current for Cascaded H-Bridge Inverters in Renewable Energy and Storage Systems. *IEEE Trans. Ind. Electron.* **2021**, *68*, 11035–11043. [CrossRef]
13. Ozkan, Z.; Hava, A.M. A Survey and Extension of High Efficiency Grid Connected Transformerless Solar Inverters with Focus on Leakage Current Characteristics. In Proceedings of the 2012 IEEE Energy Conversion Congress and Exposition (ECCE), Raleigh, NC, USA, 15–20 September 2012; pp. 3453–3460. [CrossRef]
14. Kerekes, T.; Teodorescu, R.; Borup, U. Transformerless Photovoltaic Inverters Connected to the Grid. In Proceedings of the APEC 07—Twenty-Second Annual IEEE Applied Power Electronics Conference and Exposition, Anaheim, CA, USA, 25 February–1 March 2007; pp. 1733–1737.
15. Srinivas, V.L.; Singh, B.; Mishra, S. Enhanced Power Quality PV Inverter with Leakage Current Suppression for Three-Phase SECS. *IEEE Trans. Ind. Electron.* **2022**, *69*, 5756–5767. [CrossRef]
16. Jahan, HK A New Transformerless Inverter with Leakage Current Limiting and Voltage Boosting Capabilities for Grid-Connected PV Applications. *IEEE Trans. Ind. Electron.* **2020**, *67*, 10542–10551. [CrossRef]
17. Cavalcanti, M.C.; De Oliveira, K.C.; De Farias, A.M.; Neves, F.A.S.; Azevedo, G.M.S.; Camboim, F.C. Modulation Techniques to Eliminate Leakage Currents in Transformerless Three-Phase Photovoltaic Systems. *IEEE Trans. Ind. Electron.* **2010**, *57*, 1360–1368. [CrossRef]
18. Qiu, J.; He, Y.; Lei, C.; Jiao, Q.; Liu, J. An Improved LMSVM Method for Leakage Current Suppression and Neutral-Point Voltage Control in Transformerless NPC Three-Level Inverters. *IEEE J. Emerg. Sel. Top. Power Electron.* **2022**, *10*, 3100–3113. [CrossRef]
19. López, Ó.; Freijedo, F.D.; Yepes, A.G.; Fernández-Comesaña, P.; Malvar, J.; Doval-Gandoy, J.; Teodorescu, R. Eliminating Ground Current in a Transformerless Photovoltaic Application. *IEEE Trans. Energy Convers.* **2010**, *25*, 140–147. [CrossRef]
20. Jahan, S.; Kibria, M.F.; Biswas, S.P.; Islam, M.R.; Rahman, M.A.; Muttaqi, K.M. H9 and H10 Transformer-Less Solar Photovoltaic Inverters for Leakage Current Suppression and Harmonic Current Reduction. *IEEE Trans. Ind. Appl.* **2022**. [CrossRef]
21. Hasanzadeh, A.; Edrington, C.S.; Leonard, J. Reduced Switch NPC-Based Transformerless PV Inverter by Developed Switching Pattern. In Proceedings of the 2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, FL, USA, 5–9 February 2012; pp. 359–363. [CrossRef]
22. Kibria, M.F.; Biswas, M.; Biswas, S.P.; Islam, M.R. A New H8 Transformer-Less Single Phase Grid-Tied Solar PV Inverter to Supress Leakage Current. In Proceedings of the 2021 IEEE 4th International Conference on Computing, Power and Communication Technologies (GUCON), Kuala Lumpur, Malaysia, 24–26 September 2021; pp. 4–8. [CrossRef]
23. Dolara, A.; Leva, S. Power Quality and Harmonic Analysis of End User Devices. *Energies* **2012**, *5*, 5453–5466. [CrossRef]
24. Kumar, D.; Zare, F. Harmonic Analysis of Grid Connected Power Electronic Systems in Low Voltage Distribution Networks. *IEEE J. Emerg. Sel. Top. Power Electron.* **2016**, *4*, 70–79. [CrossRef]
25. Yaghoobi, J.; Zare, F.; Rehman, T.; Rathnayake, H. Analysis of High Frequency Harmonics in Distribution Networks: 9–150 KHz. In Proceedings of the 2019 IEEE International Conference on Industrial Technology (ICIT), Melbourne, VIC, Australia, 13–15 February 2019; pp. 1229–1234. [CrossRef]
26. *Eigenerzeugungsanlagen Am Niederspannungsnetz*; Document VDE V0126-1-1; VDE: Berlin, Germany, 2006.
27. *Standard 1547.1-2005*; EEE Standard Conformance Test Procedures for Equipment Interconnecting Distributed Resources with Electric Power Systems. IEEE: Piscataway, NJ, USA, 2005; pp. 1–54.
28. *Power Generation Systems Connected to the Low-Voltage Distribution Network-Technical Minimum Requirements for the Connection to and Parallel Operation with Low-Voltage Distribution Networks*; Document VDE-AR-N 4105-2011; VDE: Berlin, Germany, 2011.
29. *IEC 61727-2004*; Photovoltaic (PV) Systems-Characteristics of the Utility Interface. International Electrotechnical Commission (IEC): Geneva, Switzerland, 2004.
30. *IEEE Standard 929-2000*; Recommended Practice for Utility Interface of Photovoltaic Systems. IEEE: Piscataway, NJ, USA, 2000.
31. *Recommendations for the Connection of Type Tested Small-Scale Embedded Generators (Up to 16A Per Phase) in Parallel with Low-Voltage Distribution Systems*; Document Engineering Rec. G83 2-2012; Energy Networks Association (ENA): London, UK, 2012.
32. *Guideline to the Standard EN 61000-3-2*; European Power Supply Manufacturers Association EPSMA: Nuremberg, Germany, 2010.
33. *Guideline for Generating Plants' Connection to and Parallel Operation with the Medium-Voltage Network*; BDEW: Berlin, Germany, 2008.
34. *GB/T 19964-2012*; Technical Requirements for Connecting Photovoltaic Power Station to Power System. Standardization Administration of the PRC: Beijing, China, 2012.
35. *Grid-Interconnection Code*; Document JEAC 9701-2012; Japan Electric Association: Tokyo, Japan, 2012.
36. Victor, M.; Greizer, F.; Bremicker, S.; Hübler, U. Method of Converting a Direct Current Voltage from a Source of Direct Current Voltage, More Specifically from a Photovoltaic Source of Direct Current Voltage, into a Alternating Current Voltage. U.S. Patent 411802B2, 12 August 2008.
37. Yang, B.; Li, W.; Gu, Y.; Cui, W.; He, X. Improved Transformerless Inverter with Common-Mode Leakage Current Elimination for a Photovoltaic Grid-Connected Power System. *IEEE Trans. Power Electron.* **2012**, *27*, 752–762. [CrossRef]

38. Rahman, M.M.; Hossain, M.S.; Talukder, M.S.I.; Uddin, M.N. Transformerless Six-Switch (H6)-Based Single-Phase Inverter for Grid-Connected Photovoltaic System with Reduced Leakage Current. *IEEE Trans. Ind. Appl.* **2022**, *58*, 974–985. [CrossRef]
39. Schmidt, H.; Siedle, C.; Ketterer, J. DC/AC Converter to Convert Direct Electric Voltage into Alternating Voltage or into Alternating Current. U.S. Patent 7 046 534, 16 May 2006.
40. Islam, M.; Mekhilef, S. H6-type Transformerless Single-phase Inverter for Grid-tied Photovoltaic System. *IET Power Electron.* **2015**, *8*, 636–644. [CrossRef]
41. Islam, M.; Afrin, N.; Mekhilef, S. Efficient Single Phase Transformerless Inverter for Grid-Tied PVG System with Reactive Power Control. *IEEE Trans. Sustain. Energy* **2016**, *7*, 1205–1215. [CrossRef]
42. Tey, K.S.; Mekhilef, S. A Reduced Leakage Current Transformerless Photovoltaic Inverter. *Renew. Energy* **2016**, *86*, 1103–1112. [CrossRef]
43. Islam, M.; Mekhilef, S. Efficient Transformerless MOSFET Inverter for a Grid-Tied Photovoltaic System. *IEEE Trans. Power Electron.* **2016**, *31*, 6305–6316. [CrossRef]
44. Kibria, M.F.; Jahan, S.; Biswas, S.P.; Islam, M.R.; Rahman, M.A.; Muttaqi, K.M. H9 and H10 Transformer-Less Solar Photovoltaic Inverters for Leakage Current Suppression and Harmonic Current Reduction. In Proceedings of the Conference Record—IAS Annual Meeting (IEEE Industry Applications Society), Vancouver, BC, Canada, 10–14 October 2021; Volume 2021, pp. 6–11. [CrossRef]
45. Kibria, M.F.; Biswas, M.; Biswas, S.P.; Islam, M.R. An Efficient Single-Phase Transformer-Less Grid-Tied Photovoltaic Inverter to Reduce Leakage Current and Improve Power Quality. In Proceedings of the 2021 IEEE 4th International Conference on Computing, Power and Communication Technologies (GUCON), Kuala Lumpur, Malaysia, 24–26 September 2021; pp. 1–6. [CrossRef]
46. Xiao, H.; Xie, S.; Chen, Y.; Huang, R. An Optimized Transformerless Photovoltaic Grid-Connected Inverter. *IEEE Trans. Ind. Electron.* **2011**, *58*, 1887–1895. [CrossRef]
47. Zhang, L.; Sun, K.; Feng, L.; Wu, H.; Xing, Y. A Family of Neutral Point Clamped Full-Bridge Topologies for Transformerless Photovoltaic Grid-Tied Inverters. *IEEE Trans. Power Electron.* **2013**, *28*, 730–739. [CrossRef]
48. Li, H.; Zeng, Y.; Zhang, B.; Zheng, T.Q.; Hao, R.; Yang, Z. An Improved H5 Topology with Low Common-Mode Current for Transformerless PV Grid-Connected Inverter. *IEEE Trans. Power Electron.* **2019**, *34*, 1254–1265. [CrossRef]
49. Freddy, T.K.S.; Rahim, N.; Hew, W.-P.; Che, H.S. Comparison and Analysis of Single-Phase Transformerless Grid-Connected PV Inverters. *IEEE Trans. Power Electron.* **2014**, *29*, 5358–5369. [CrossRef]
50. Kerekes, T. Analysis and Modeling of Transformerless Photovoltaic Inverter Systems. Ph.D. Thesis, Aalborg University, Aalborg, Denmark, 2009.
51. Khan, M.N.H.; Siwakoti, Y.P.; Li, L.; Blaabjerg, F. H-Bridge Zero-Voltage Switch-Controlled Rectifier Transformerless Midpoint-Clamped Inverter for Photovoltaic Applications. *IEEE J. Emerg. Sel. Top. Power Electron.* **2020**, *8*, 4382–4394. [CrossRef]
52. Gu, Y.; Li, W.; Zhao, Y.; Yang, B.; Li, C.; He, X. Transformerless Inverter with Virtual DC Bus Concept for Cost-Effective Grid-Connected PV Power Systems. *IEEE Trans. Power Electron.* **2013**, *28*, 793–805. [CrossRef]
53. Siwakoti, Y.P.; Blaabjerg, F. A Novel Flying Capacitor Transformerless Inverter for Single-Phase Grid Connected Solar Photovoltaic System. In Proceedings of the 2016 IEEE 7th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), Vancouver, BC, Canada, 27–30 June 2016. [CrossRef]
54. Siwakoti, Y.P.; Blaabjerg, F. Common-Ground-Type Transformerless Inverters for Single-Phase Solar Photovoltaic Systems. *IEEE Trans. Ind. Electron.* **2018**, *65*, 2100–2111. [CrossRef]
55. Siwakoti, Y.P.; Blaabjerg, F. H-Bridge Transformerless Inverter with Common Ground for Single-Phase Solar-Photovoltaic System. In Proceedings of the 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), Tampa, FL, USA, 26–30 March 2017; pp. 2610–2614. [CrossRef]
56. Knaup, P. International Patent Application. WO Patent 048 420 A1, 3 May 2007.
57. Ardashir, J.F.; Sabahi, M.; Hosseini, S.H.; Blaabjerg, F.; Babaei, E.; Gharehpetian, G.B. A Single-Phase Transformerless Inverter with Charge Pump Circuit Concept for Grid-Tied PV Applications. *IEEE Trans. Ind. Electron.* **2017**, *64*, 5403–5415. [CrossRef]
58. TofighAzary, M.; Sabahi, M.; Babaei, E.; Abbasi AghdamMeinagh, F. Modified Single-Phase Single-Stage Grid-Tied Flying Inductor Inverter With MPPT and Suppressed Leakage Current. *IEEE Trans. Ind. Electron.* **2018**, *65*, 221–231. [CrossRef]
59. Karschny, D. Flying Inductor Topology. DE Patent 196 42 522 C1, 23 April 1998.
60. Gao, N.; Member, A.; Jin, Z.; Wang, H.; Wu, W.; Koutroulis, E.; Member, S.; Chung, H.S. MOSFET-Switch-Based Transformerless Single-Phase Grid-Tied Inverter for PV Systems. *IEEE J. Emerg. Sel. Top. Power Electron.* **2022**, *10*, 3830–3839. [CrossRef]
61. Manoj, P.; Kirubakaran, A.; Somasekhar, V.T. A Single-Stage Quasi-Z-Source Based 5-Level Grid-Tied PV Inverter with Reduced Leakage Current. *IEEE J. Emerg. Sel. Top. Power Electron.* **2022**. [CrossRef]
62. Heydari-doostabad, H.; Pourmahdi, M.; Jafarian, M.; Keane, A.; Member, S.; Donnell, T.O.; Member, S. Three-Switch Common Ground Step-Down and Step-Up Single-Stage Grid-Connected PV Inverter. *IEEE Trans. Power Electron.* **2022**, *37*, 7577–7589. [CrossRef]
63. Iturriaga-Medina, S.; Martinez-Rodriguez, P.R.; Escobar-Valderrama, G.; Vazquez-Guzman, G.; Langarica-Cordoba, D.; Rosas-Caro, J.C.; Sosa-Zuniga, J.M.; Mayo-Maldonado, J.C. Leakage-Ground Currents Compensation in a Transformerless HB-NPC Topology Using a DC-Link-Tied LC Filter for Photovoltaic Applications. *IEEE J. Emerg. Sel. Top. Power Electron.* **2022**, *10*, 4725–4737. [CrossRef]

64. Xu, X.; Su, M.; Sun, Y.; Guo, B.; Wang, H.; Xu, G. Four-Switch Single-Phase Common-Ground PV Inverter with Active Power Decoupling. *IEEE Trans. Ind. Electron.* **2022**, *69*, 3223–3228. [CrossRef]
65. Peng, F.; Member, S.; Zhou, G.; Member, S.; Xu, N.; Gao, S. Zero Leakage Current Single-Phase Quasi-Single-Stage Transformerless PV Inverter with Unipolar SPWM. *IEEE Trans. Power Electron.* **2022**, *37*, 13755–13766. [CrossRef]
66. Bahrami-Fard, M.; Moeini, N.; Shahabadini, M.; Iman-Eini, H.; Liserre, M. A New Topology and Modulation Strategy to Suppress the Leakage Current in Transformerless Cascaded H-Bridge Inverters in PV Application. *IEEE J. Emerg. Sel. Top. Power Electron.* **2022**. [CrossRef]
67. Patrao, I.; Figueres, E.; González-Espín, F.; Garcerá, G. Transformerless Topologies for Grid-Connected Single-Phase Photovoltaic Inverters. *Renew. Sustain. Energy Rev.* **2011**, *15*, 3423–3431. [CrossRef]
68. Jana, J.; Saha, H.; Das Bhattacharya, K. A Review of Inverter Topologies for Single-Phase Grid-Connected Photovoltaic Systems. *Renew. Sustain. Energy Rev.* **2017**, *72*, 1256–1270. [CrossRef]
69. Li, W.; Gu, Y.; Luo, H.; Cui, W.; He, X.; Xia, C. Topology Review and Derivation Methodology of Single-Phase Transformerless Photovoltaic Inverters for Leakage Current Suppression. *IEEE Trans. Ind. Electron.* **2015**, *62*, 4537–4551. [CrossRef]
70. Khan, M.N.H.; Forouzesh, M.; Siwakoti, Y.P.; Li, L.; Kerekes, T.; Blaabjerg, F. Transformerless Inverter Topologies for Single-Phase Photovoltaic Systems: A Comparative Review. *IEEE J. Emerg. Sel. Top. Power Electron.* **2020**, *8*, 805–835. [CrossRef]
71. Islam, M.; Mekhilef, S.; Hasan, M. Single Phase Transformerless Inverter Topologies for Grid-Tied Photovoltaic System: A Review. *Renew. Sustain. Energy Rev.* **2015**, *45*, 69–86. [CrossRef]
72. Gubía, E.; Sanchis, P.; Ursu'a, A.; Lo'pez, J.; Marroyo, L. Ground Currents in Single-phase Transformerless Photovoltaic Systems. *Prog. Photovolt Res. Appl.* **2007**, *15*, 629–650. [CrossRef]
73. Chen, W.; Yang, X.; Zhang, W.; Song, X. Leakage Current Calculation for PV Inverter System Based on a Parasitic Capacitor Model. *IEEE Trans. Power Electron.* **2016**, *31*, 8205–8217. [CrossRef]
74. Kerekes, T.; Teodorescu, R.; Liserre, M.; Klumpner, C.; Sumner, M. Evaluation of Three-Phase Transformerless Photovoltaic Inverter Topologies. *IEEE Trans. Power Electron.* **2009**, *24*, 2202–2211. [CrossRef]
75. González, R.; Gubía, E.; López, J.; Marroyo, L. Transformerless Single-Phase Multilevel-Based Photovoltaic Inverter. *IEEE Trans. Ind. Electron.* **2008**, *55*, 2694–2702. [CrossRef]
76. Ji, B.; Wang, J.; Zhao, J. High-Efficiency Single-Phase Transformerless PV H6 Inverter with Hybrid Modulation Method. *IEEE Trans. Ind. Electron.* **2013**, *60*, 2104–2115. [CrossRef]
77. Xiao, H.; Xie, S. Leakage Current Analytical Model and Application in Single-Phase Transformerless Photovoltaic Grid-Connected Inverter. *IEEE Trans. Electromagn. Compat.* **2010**, *52*, 902–913. [CrossRef]
78. Bradaschia, F.; Cavalcanti, M.C.; Ferraz, P.E.P.; Neves, F.A.S.; Dos Santos, E.C.; Da Silva, J.H.G.M. Modulation for Three-Phase Transformerless z-Source Inverter to Reduce Leakage Currents in Photovoltaic Systems. *IEEE Trans. Ind. Electron.* **2011**, *58*, 5385–5395. [CrossRef]
79. Yu, W.; Lai, J.S.; Qian, H.; Hutchens, C. High-Efficiency MOSFET Inverter with H6-Type Configuration for Photovoltaic Nonisolated AC-Module Applications. *IEEE Trans. Power Electron.* **2011**, *26*, 1253–1260. [CrossRef]
80. Vazquez, G.; Kerekes, T.; Rolan, A.; Aguilar, D.; Luna, Á.; Azevedo, G. Losses and CMV Evaluation in Transformerless Grid-Connected PV Topologies. In Proceedings of the 2009 IEEE International Symposium on Industrial Electronics, Seoul, Republic of Korea, 5–8 July2009; pp. 544–548. [CrossRef]
81. Gu, B.; Dominic, J.; Lai, J.S.; Chen, C.L.; Labella, T.; Chen, B. High Reliability and Efficiency Single-Phase Transformerless Inverter for Grid-Connected Photovoltaic Systems. *IEEE Trans. Power Electron.* **2013**, *28*, 2235–2245. [CrossRef]
82. *IEC 61727 CDV*; Characteristics of the Utility Interface for Photovoltaic (PV) Systems. International Electrotechnical Commission: Geneva, Switzerland, 2002.
83. *AS 4777.3-2005*; Grid Connection of Energy Systems via Inverters Part 3: Grid Protection Requirements. Council of Standards Australia: Sydney, Australia, 2005.
84. *AS 4777.1-2005*; Grid Connection of Energy Systems via Inverters Part 1: Installation Requirements. Council of Standards Australia: Sydney, Australia, 2005.
85. *AS 4777.2-2005*; Grid Connection of Energy Systems via Inverters Part 2: Inverter Requirements. Council of Standards Australia: Sydney, Australia, 2005.
86. PSIM User's Guide. 2007. Available online: http://www.Psimeurope.Com (accessed on 27 November 2022).
87. Freddy, T.K.S.; Lee, J.H.; Moon, H.C.; Lee, K.B.; Rahim, N.A. Modulation Technique for Single-Phase Transformerless Photovoltaic Inverters with Reactive Power Capability. *IEEE Trans. Ind. Electron.* **2017**, *64*, 6989–6999. [CrossRef]
88. Kumar, K.S.; Kirubakaran, A.; Subrahmanyam, N. Bidirectional Clamping-Based H5, HERIC, and H6 Transformerless Inverter Topologies with Reactive Power Capability. *IEEE Trans. Ind. Appl.* **2020**, *56*, 5119–5128. [CrossRef]
89. Fang, J.; Shi, M.; Xiao, H.; Wang, R. A Zero-Voltage-Transition H5-Type Transformerless Photovoltaic Grid-Connected Inverter. *IEEE Access* **2019**. [CrossRef]
90. Mahfuz-Ur-Rahman, A.M.; Islam, M.R.; Muttaqi, K.M.; Rahman, M.A.; Sutanto, D. An Advanced Modulation Technique for Transformer-Less Grid-Connected Inverter Circuits Used in Solar Photovoltaic Systems. *IEEE Trans. Ind. Electron.* **2022**, *70*, 3878–3887. [CrossRef]
91. Saridakis, S.; Koutroulis, E.; Blaabjerg, F. Optimization of SiC-Based H5 and Conergy-NPC Transformerless PV Inverters. *IEEE J. Emerg. Sel. Top. Power Electron.* **2015**, *3*, 555–567. [CrossRef]

92. Xiao, H.; Zhang, L.; Wang, Z.; Cheng, M. A New Soft-Switching Configuration and Its Application in Transformerless Photovoltaic Grid-Connected Inverters. *IEEE Trans. Ind. Electron.* **2018**, *65*, 9518–9527. [CrossRef]
93. Xiao, H.F.; Zhang, L.; Li, Y. A Zero-Voltage-Transition HERIC-Type Transformerless Photovoltaic Grid-Connected Inverter. *IEEE Trans. Ind. Electron.* **2017**, *64*, 1222–1232. [CrossRef]
94. Tang, Z.; Su, M.; Sun, Y.; Cheng, B.; Yang, Y.; Blaabjerg, F.; Wang, L. Hybrid UP-PWM Scheme for HERIC Inverter to Improve Power Quality and Efficiency. *IEEE Trans. Power Electron.* **2019**, *34*, 4292–4303. [CrossRef]
95. Wang, J.; Luo, F.; Ji, Z.; Sun, Y.; Ji, B.; Gu, W.; Zhao, J. An Improved Hybrid Modulation Method for the Single-Phase H6 Inverter with Reactive Power Compensation. *IEEE Trans. Power Electron.* **2018**, *33*, 7674–7683. [CrossRef]
96. Wang, J.; Gao, S.; Sun, Y.; Ji, Z.; Cheng, L.; Li, L.; Gu, W.; Zhao, J. Single Phase Bidirectional H6 Rectifier/Inverter. *IEEE Trans. Power Electron.* **2019**, *34*, 10710–10719. [CrossRef]
97. Yang, Y.; Yang, Y.; He, L.; Fan, M.; Xiao, Y.; Chen, R.; Xie, M.; Zhang, X.; Zhang, L.; Rodriguez, J. A Novel Cascaded Repetitive Controller of an *LC*-Filtered H6 Voltage-Source Inverter. *IEEE J. Emerg. Sel. Top. Power Electron.* **2022**. [CrossRef]
98. Liu, B.; Su, M.; Yang, J.; Song, D.; He, D.; Song, S. Combined Reactive Power Injection Modulation and Grid Current Distortion Improvement Approach for H6 Transformer-Less Photovoltaic Inverter. *IEEE Trans. Energy Convers.* **2017**, *32*, 1456–1467. [CrossRef]
99. Begh, M.A.W.; Liegmann, E.; Mahajan, A.; Palanisamy, A.; Siwakoti, Y.P.; Karamanakos, P.; Abdelrahem, M.; Kennel, R. Design of State-Feedback Controller for a Single-Phase Grid-Connected Siwakoti-h Inverter with LCL Filter. In Proceedings of the PCIM Europe Conference 2019, Nuremberg, Germany, 7–9 May 2019; pp. 1587–1594.
100. Begh, M.A.W.; Liegmann, E.; Karamanakos, P.; Kennel, R. Direct Model Predictive Control of a Single-Phase Grid-Connected Siwakoti-H Inverter. In Proceedings of the IECON (The 46th Annual Conference of the Industrial Electronics Conference), Singapore, 18–21 October 2020; Volume 2020, pp. 3045–3050.

Disclaimer/Publisher's Note: The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.