

Review

Foundry Service of CMOS MEMS Processes and the Case Study of the Flow Sensor

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Abstract: The complementary metal-oxide-semiconductor (CMOS) process is the main stream to fabricate integrated circuits (ICs) in the semiconductor industry. Microelectromechanical systems (MEMS), when combined with CMOS electronics to form the CMOS MEMS process, have the merits of small features, low power consumption, on-chip circuitry, and high sensitivity to develop micro-sensors and micro actuators. Firstly, the authors review the educational CMOS MEMS foundry service provided by the Taiwan Semiconductor Research Institute (TSRI) allied with the United Microelectronics Corporation (UMC) and the Taiwan Semiconductor Manufacturing Company (TSMC). Taiwan's foundry service of ICs is leading in the world. Secondly, the authors show the new flow sensor integrated with an instrumentation amplifier (IA) fabricated by the latest UMC 0.18 μm CMOS MEMS process as the case study. The new flow sensor adopted the self-heating resistive-thermal-detector (RTD) to sense the flow speed. This self-heating RTD half-bridge alone gives a normalized output sensitivity of $138 \mu\text{V}/\text{V}/(\text{m}/\text{s})/\text{mW}$ only. After being integrated with an on-chip amplifier gain of 20 dB, the overall sensitivity of the flow sensor was measured and substantially improved to $1388 \mu\text{V}/\text{V}/(\text{m}/\text{s})/\text{mW}$ for the flow speed range of 0–5 m/s. Finally, the advantages of the CMOS MEMS flow sensors are justified and discussed by the testing results.

Keywords: CMOS; MEMS; UMC 0.18 μm ; flow sensor



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1. Introduction

When humans entered the 21st century from the 20th century, the cross-sector integration of science and technology was constantly emerging, in conjunction with the trend of miniaturization, multi-functionality, and precision. It is the development of various cutting-edge technologies and industries (including nanotechnology, materials, chemicals, electronics, computers, information, photovoltaics, machinery, medicine, biotechnology, health care, environmental protection, and energy, etc.), and will have a huge impact on human life, even economic and wealth distribution. The first to propose the concept of microelectromechanical systems (MEMS) or micro system technology (MST) was the physicist, R. Feynman [1]. In 1959, at the annual meeting of the American Physical Society, he delivered a speech entitled “There is plenty of room at the bottom” to attract people’s attention to small-scale science and technology. Shortly after Feynman’s second speech “Infinitesimal machinery”, this emerging technology measured in units of the “micrometer” (μm). The invention of the transistor at Bell Telephone Laboratories in 1947 sparked a fast-growing microelectronic technology [2,3]. Piezoresistive silicon strain gauges were introduced in the late 1950s by Kulite Semiconductor, with Bell Lab’s first licensee of patents on semiconductor piezoresistance reported in 1954 [4,5]. It was discovered that the piezoresistive effect in Ge and Si had the potential to produce Ge and Si strain gauges with

a gauge factor (i.e., instrument sensitivity) 10 to 20 times greater than those based on metal films [4]. As a result, Si strain gauges began to be developed commercially in 1958. The first high-volume pressure sensor was marketed by National Semiconductor in 1974. This sensor included a temperature controller for constant-temperature operation. In 1982, silicon was called a mechanical material in K. Petersen's famous review article [6]. During 1987–1988, a turning point was reached in micromachining when, for the first time, techniques for the integrated fabrication of mechanisms (i.e., rigid bodies connected by joints for transmitting, controlling, or constraining relative movement) on Si were demonstrated. The resonant gate transistor (RGT) [7] was dissimilar with conventional transistors in that it was not fixed to the gate oxide. As an alternative, it was movable and cantilevered with respect to the substrate used. In 1967, the RGT was the earliest demonstration of micro electrostatic actuators. It was also the first demonstration of surface micromachining techniques. In 1971, Intel publicly introduced the world's first single chip microprocessor, the Intel 4004. The 4004 powered the Busicom calculator and was Intel's first microprocessor [8]. Muller, Fan, and Tai invented the world's first micrometer-sized electrostatic motor (micromotor) in 1989 at the University of California, Berkeley, using the IC process technology before the official terminology of MEMS [9,10]. R. S. Muller of UC Berkeley started the IEEE Electron Devices Society of IEEE/ASME Journal of Microelectromechanical Systems in 1990. The story of the invention of the charge-coupled device (CCD) is easier to unravel: L.F.J. Sangster [11] of Philips Research Laboratory and W.S. Boyle and G.E. Smith [12] of Bell Laboratories at Murray Hill independently came up with the CCD structure. In the United States, J.B. Angell, Stanford University [13–15], and K. D. Wise from University of Michigan also made astonishing steps with their work [13,15–19]. Though there were many initiatives in the 1960s, it is almost certain that Stanford University's Integrated Circuits Laboratory, under the guidance of Prof. J. Angell, can be credited with being the renowned research group to be active in the field of silicon sensors and micromachining. Another enthusiastic group had also been working on silicon sensors for biomedical applications under the guidance of sensor pioneer Prof. W. H Ko, Case Western Reserve University [20,21]. The first of the gate-controlled diode designed by Zemel et al. [22] at the University of Pennsylvania can also be noted. In Sweden, I. Lundstrom et al. invented Pd-gate, which led many to interesting gas-sensitive devices at the University of Linköping in 1975 [23], and G. Stemme, who worked at Royal Institute of Technology, Sweden, also made contributions in this field [24]. The first to point out the necessity of applying CAD to sensors was S. D Senturia from MIT, UK, in 1976 [25]. The first silicon flow sensor based on the temperature sensitivity of a diffused Wheatstone bridge in silicon was designed by van Putten and Middelhoek Delf University of Technology in 1974 [26]. P. Bergveld of the University of Twente [27] and R Puers of K. U Leuven are also remarkable mentions from the Netherlands [28]. The Institute of Integrated Micro and Nano Systems, School of Engineering and Electronics, Scottish Microelectronics Centre, University of Edinburgh, Scotland; T. Matsuo of Tokohu University, Japan [17]; M. Bao of Fudan University, China [20]; W. Gopel from the University of Tübingen, 1983 [29–31]; and E. Obermeier T.U Berlin, Germany 1987 [32,33] are some of the renowned institutions and professors from distinguished universities from several countries whose era should be remembered.

In 1994, Cornell University introduced a bulk micromachining process called single crystal reactive etching and metallization (SCREAM) [34]. Special mention is also made of Petersen's review paper [6], a truly seminal work that gave the field a much-needed impetus. From 2005 to 2021 with the advancement in MEMS fabrication, manufacturing technologies and processes, the various applications of MEMS structures were explored and developed, some of which are airbag accelerometers, intelligent tires, vehicle security systems, inertial brake lights, headlight leveling, rollover detection; inkjet printer heads, projection screen and televisions, mass data storage systems, sports training devices, earthquake detection and gas shutoff, projection displays in portable communications devices and instrumentation, voltage controlled oscillators (VCOs); surveillance, arming systems, embedded sensors, data storage, aircraft control, tanks control; and blood pressure sensors,

muscle stimulators and drug delivery systems, implanted pressure sensors, prosthetics body parts, polymerase chain reaction (PCR) microsystems, micromachined scanning tunneling microscopes (STMs), biochips for detection of hazardous chemical and biological agents, high-throughput drug screening, and so on.

Thus, we can observe, from the last several decades, that there has been rapid growth of complementary metal-oxide-semiconductor (CMOS) MEMS fabrication technology, which enables the manufacturing of micro devices of various sensors and actuators. The term MEMS originally meant miniaturized electromechanical actuators but now applies to a broad family of micromachined sensors, actuators, and systems with coupled electrical, mechanical, radiant, thermal, magnetic, and chemical effects. The technologies are based on the sequence of the fabrication of CMOS circuitry and MEMS elements, while silicon-on-insulator (SOI) and CMOS MEMS are discussed separately [4,35–37]. There are different CMOS MEMS fabrication approaches, namely pre-CMOS, intermediate-CMOS, and post-CMOS. Starting from 0.8 μm double-polysilicon–double-metal (DPDM) CMOS process, tremendous efforts have been made to continuously improve process yield and reliability, while minimal feature sizes and fabrication cost continue to decrease [35,38–40]. The concept of producing MEMS devices in a standard CMOS process was first described by H. Baltes [29,39,41–48]; other researchers from Switzerland, namely N. F. de Rooij, University of Neuchatel [49] and R. Popovic, EPFL [50], are famous contributors to this field. Baltes conducted the feasibility study followed by the launch of several national agencies that had the ability to provide the CMOS foundry service. The motivation for its research and development (R&D) was to directly use off-the-shelf IC foundry equipment and integrate the MEMS sensors and actuators with sensing signal processing on the same silicon chip (on-chip circuitry). Designers of MEMS devices only need to design the layout and, after the completion of the foundry service, to perform post-processing to obtain the desired MEMS devices. The benefits of the MEMS sensors, actuators, and the signal processing circuits can be linked on-chip together to reduce the influence of external noise to a minimum and improve component performance. After verifying the stability and reliability of the CMOS MEMS devices by using CMOS foundry, it may be quick to enter the production market and create business opportunities. Semiconductor roadmaps show the current state and, more important, outline the future performance of CMOS technology with ever-increasing integration density and decreasing feature size [37,51–55]. With the breakthrough of technologies, it has enabled integrating MEMS structures with ICs on a single CMOS substrate, so-called monolithic CMOS MEMS integration.

CMOS-compatible MEMS technologies includes bulk micromachining (wet or dry, isotropic or anisotropic, from wafer front or back), surface micromachining (sacrificial dielectric and/or metal or polysilicon), micromachining before/after completion of the IC process (pre-CMOS/post-CMOS), use of IC materials for microstructures with electro-thermo or opto-mechanical functions, thin film deposition, chemical-mechanical polishing (CMP), and wafer bonding. However, if the above cannot be exactly fabricated in the simple clean room of researchers' laboratory, commercial CMOS foundry service could be found as help.

Caltech released the first IC-integrated flexible shear stress sensor skin in 2003, which can instantly respond to aerodynamics drag. The measurement signals are mixed for adaptive flow control and the flight control of fixed-wing micro-aircraft [56,57]. MEMS multi-sensor chip for gas flow sensing was also developed by Xu et al. [58]. The above-mentioned sensor-actuated array chips were applied to a 2 μm CMOS MEMS foundry service. Recently, the Hong Kong University of Science and Technology (HKUST) and National Chao-Tong University (NCTU) have co-developed a calorimetric flow sensor using a CMOS 0.18 μm double-poly-four-metal (2P4M) MEMS foundry service provided by the Chip Implementation Center (CIC) of Taiwan to completely manufacture the overall chip [59,60].

The authors have chosen flow sensor to be a design example later in Section 4. Some reasons why the flow sensor was selected as the case study herein are as follows:

- Flow sensors have many emerging applications such as in oxygen respirators [61], leak detection [62], flow rate detection [59,60], gas supply control [58,63], air speed detection of wind tunnel [64], wind turbine [65–68], biomimetic flapping wing studies [69–75], etc. A robust and miniaturized instrument and measurement system is required to obtain accurate and reliable flow speed recordings of the above applications.
- Compared to other mechanical sensors, fewer flow sensors were developed by the CMOS MEMS foundry service and deserve to be discussed more [76,77].
- The design configurations of flow sensors are quite different from other mechanical sensors such as pressure sensors and inertial sensors [78]. Their requirement about the post-process was different from other MEMS sensors as well. By including this case study, one can complete the addressing of CMOS MEMS foundry technology.

It is indeed important to mention future trends, where a number of researchers have started exploring more about Silicon carbide materials and nanostructures. The study of these materials requires a good understanding of physical, biological and chemical properties, fundamental studies, as well as applied, theoretical and/or computational studies related to several new applications. Bulk silicon carbide is a wide-bandgap semiconductor with different crystalline forms owing to excellent electronic characteristics; it has mainly been used for high-temperature, high-frequency, and high-power electronic devices. It is also recognized as one of the best biocompatible materials, especially in cardiovascular and blood-contacting implants and other biomedical devices [79–86].

2. CMOS MEMS Foundry Service

United Microelectronics Corporation (UMC) was founded as Taiwan's first IC fabrication company in 1980 as a spin-off from the government-sponsored Industrial Technology Research Institute (ITRI) in Hsinchu, Taiwan. Being a significant supplier to the automotive industry, UMC has four 300 mm fabs: one in Tainan, Taiwan; one in Singapore; one in Xiamen, China; and one in Japan. UMC also has several 200 mm fabs in Hsinchu and Suzhou, China. In 1995, the foundry service just started. In 1996, the UMC 0.35 μm CMOS process was released successfully. In 1997 and 1999, the minimum line width or the critical dimension (CD) was upgraded to 0.35 μm and 0.18 μm , respectively. At that time, UMC focused on improving their CMOS IC process capability only. The CMOS MEMS researchers need to carry out their die-level post-process of CMOS MEMS personally, e.g., by performing their own plasma-enhanced chemical vapor deposition (PECVD) process in which the deposition of thin films of various materials takes place at a low temperature (<350 °C) that the standard CMOS chips can endure. The various post-processes after the CMOS standard process may be also followed by die-level photolithography, wet etching (backside), wet etching (front side), wet etching followed by electroplating nickel, or wet etching (fronts side) followed by gelatin coating [87,88] or parylene coating [89], etc. The details will be mentioned in Section 3.

Taiwan Semiconductor Manufacturing Company, Ltd. (TSMC) is another Taiwanese multinational semiconductor contract manufacturing and design company with its headquarters and main operations located in Hsinchu Scientific Park in Taiwan. On 300 mm wafers, currently, TSMC has silicon lithography on node sizes ranging from 0.13 μm to 5 nm and is ranked the number one of the IC foundry providers in the world. The capability of the IC foundry service in Taiwan proves its top leading place in the globe. The reasons are not only due to the strong IC design houses and the reliable equipment supply of the semiconductor process but also due to the high utility rate of the process equipment and high product yield rate. For TSMC especially, they additionally created the advantage of flexibility in process sequence and process conditions and set up a very high entry barrier, which other IC fab companies may not easily surpass.

Regarding the IC designer training for students in Taiwan, the Ministry of Science and Technology (MOST; or National Science Council) founded the CIC in Hsinchu Scientific Park. CIC provided low-price or free access of Cadence software to the academics and called for IC designs from all universities in Taiwan regularly. After review and defense,

CIC granted the real chip implementation for the selected IC designs and merged the selected IC layouts into a multi-project-wafer (MPW). Finally, CIC sent the photomasks to TSMC or UMC for fabricating a batch of wafers with these selected IC designs. After the IC foundry service, the IC designers could receive 20–40 pieces of CMOS IC chips for testing and verifying the functionality. The student designers had obligations to submit the test reports to CIC within months after they received the IC chips. Through this kind of education training, using real IC foundry services with several times of call-for-designs every year, CIC trained many IC student designers for IC design houses as well as developing or exploring some advanced IC circuit designs at the same time. It is important to note that, many universities do not have proper clean rooms except for a few of them. Maintaining a high-class clean room needs millions in investment. Like our research team, many other researchers are able to use this foundry service to fabricate the novel design using the CMOS MEMS process without any huge investment. The Sensor and IC designer could fabricate their design model smoothly without much hindrance, and the foundry companies also kept updated about the new design invention and innovation. Both the teams mutually benefitted from the faster development process.

The commercial IC design framework has been standardized by Cadence with Tenor (layout design), H-SPICE (circuit simulation), Verilog (IC verification), and so on. Therefore, CIC provided a huge education discount for all universities in Taiwan to buy the user license of Cadence. All student users needed to use this IC design software as the compatible design platform for doing their IC design via the CIC foundry service or even in IC technology transfer to industries. In addition, the well-trained students by CIC could easily find jobs in IC design houses after their graduation from campus. Most important of all, because CIC always asked help from TSMC and UMC about their latest version of the CMOS IC foundry service, the design rule of the minimum line width was accordingly improved from the earlier 0.35 μm CMOS process down to the 0.18 μm CMOS process.

Therefore, the IC designers in universities could access the state-of-art of IC foundry service in Taiwan and have much less time lag in developing the tiny IC chips in their current stages. CIC is not the first research center to use the MPW concept to provide the IC foundry service. The most famous prior example is the Metal Oxide Semiconductor Implementation Service (MOSIS) in the USA, with the provider MCNC (Microelectronics Center of North Carolina). As the CIC's single-poly-three-metal (1P3M) CMOS structures show in Figure 1, the corresponding sequence of material layers with their specific thickness and doping concentration cannot be changed. The only thing the IC/MEMS designers can change is their layouts of IC/MEMS devices. Compared to MOSIS in the USA, the IC foundry service in CIC does not charge the student designers in Taiwan. However, CIC has the authority to turn down any IC design proposals.

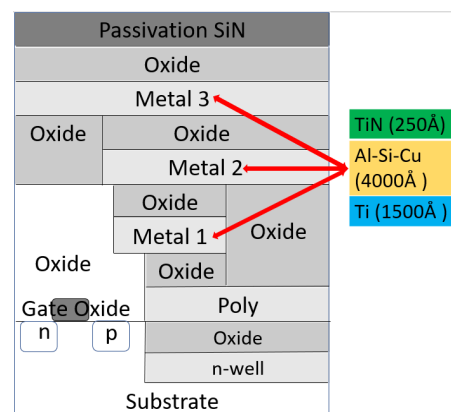


Figure 1. The structure layers of the 1P3M CMOS process provided by CIC and TSMC. Each metal structure is composed of TiN (barrier), Al-Si-Cu (conductor), and Ti (adhesion) [90].

2.1. Early Development of CMOS MEMS

The research on CMOS MEMS devices in Taiwan was started in National Taiwan University (NTU). It began with Chang, Lu, and Liu asking for help with CIC's CMOS foundry to guide students to attend the IC design courses held in CIC in the summer of 1994 and to start the layout design of capacitive micro accelerometers, piezoresistive micro pressure sensors, and sensing signal reading circuits [37,91]. The layout designers must design IC on one side and use the software to repeatedly check, simulate, and verify to minimize the possible bugs in the other side. For this reason, the IC design software focuses on the integration of transistor components and processes with known characteristics and completes the huge IC system. The designers did not receive much stress that the micro-structured layers of the wafer were subjected to, and they were not told how to perform the conversion of physical signals into electrical signals for sensing/actuating, either [92]. In other words, if they would have liked to use commercial IC design software to design or even manufacture CMOS MEMS devices, they must have first clarified the fundamental differences between transistor IC and CMOS MEMS devices. In addition, they needed to communicate this CMOS MEMS concept to CIC leaders who originally worked on the standardization and protocol of IC foundry. Otherwise, the IC designer would be amazed about the "strange" layout design methodology of CMOS MEMS devices. For example, the CMOS MEMS designers still used the Cadence software to draw layouts, but they needed not go through the complete verification procedure of the standard IC because MEMS structures are not ICs. The exact verification of the complete ICs should include the followings: (1) design rule check (DRC): checks whether the layout patterns are too dense, and ensure the foundry's production correctness, and there will be no short circuit problem; (2) electrical rule check (ERC): checks electrical characteristics; (3) layout versus schematic (LVS): compares and map the layout with the logic circuit of the schematic; and (4) layout parameter extraction (LPE): captures the electrical parameters of the layout.

For the MEMS device of the non-signal processing circuit, DRC verification is necessary to ensure that the microstructure can be successfully made, but the other three verifications (2–4) to MEMS sensor are not required (for example, a variable capacitor membrane subject to a pressure loading cannot be given or simulated for its capacitance change). Furthermore, for an IC designer, it seems a waste of a chip area of $400 \times 400 \mu\text{m}^2$ to make a single sensor capacitor because making an 8086 microprocessor may use the similar chip area. Even though the dimensions of the MEMS device are well simulated and determined in advance by finite element analysis (FEA), which has not yet been integrated into the circuit design software so far. The MEMS engineers also need to conduct cross-domain communication because CMOS MEMS are different from the traditional circuit design training. At the end of 1995, with the help of CIC and TSMC, the NTU group successfully developed the first CMOS MEMS mechanical sensors, including a piezoresistive pressure sensor and a capacitive accelerometer with a switched capacitor circuit for capacitance measurement. The first two mechanical sensors had chip areas of $2 \text{ mm} \times 3 \text{ mm}$ and $3 \text{ mm} \times 3 \text{ mm}$, respectively; the tiny switched capacitor circuit was directly placed among the mechanical sensors [35,91].

2.2. Educational CMOS Foundry Service Provided by TSRI

The Taiwan Semiconductor Research Institute (TSRI) under the National Applied Research Laboratories (NARLabs) has now been a consolidation of the CIC and Nano Device Laboratories (NDL) since 2019, with the hope of creating an integrated semiconductor research environment in which world-class academic research and innovative technological development can be conducted to sustain the competitiveness of the semiconductor industry in Taiwan. It is also to keep pace with international technology trends as well as the 3-nm node and the rapid development of new applications in, e.g., artificial intelligence, quantum computers, next-gen magnetic random-access memory, high-speed computers, and 5G network.

At the heart of sensor products is the CMOS technology using the latest TSRI/UMC 0.18 μm single-poly-six-metal (1P6M) process, which enables us to combine the sensor component with amplifier circuitry on a tiny CMOS silicon chip. The CMOS MEMS technology provides error-free gas flow metering that remains stable over a long period and generates a fast and high-precision sensor signal, recently [93–97]. Figure 2a shows the UMC 0.18 μm CMOS process proceeded with isotropic XeF_2 undercut etching for the MEMS open area; Figure 2b shows the use of shallow-trench-isolation (STI) to protect polysilicon during the etching process. It is because the gate oxide thickness is only 4 nm, and it is hard to protect the polysilicon sensor from the XeF_2 attack. Therefore, the authors proposed the using of STI oxide to protect polysilicon from the XeF_2 attack, shown in Figure 2b. The authors received permission from TSRI even though placing the polysilicon patterns above STI in MEMS region was originally a violation to the design rule.

Figure 3 shows the scanning electron microscope (SEM) photo of the so-called MEMS open area or the cavity after the isotropic XeF_2 undercut etching provided by TSRI/UMC. (All over the MEMS open area, thousands of $8\ \mu\text{m} \times 8\ \mu\text{m}$ square etch-holes were designed for XeF_2 to go through and etch the cavity underneath this MEMS open area). The etched depth by XeF_2 is measured as $44.94\ \mu\text{m}$, almost four times of the CMOS thickness of $11\ \mu\text{m}$, and is large enough to ensure the fully freestanding of the MEMS structures without any spikes or pillars underneath. This etched depth also allows the lateral separation distance between two square etch-holes to be as far as $20\ \mu\text{m}$ so that the sensor connection lines can zigzag among the etch-holes on the levitated MEMS open area. Figure 3a shows the $8\ \mu\text{m} \times 8\ \mu\text{m}$ etch-holes, of which the measured spacing is averaged as $9.09 \pm 0.28\ \mu\text{m}$ on the CMOS layer. Figure 3b also shows how smooth the sidewall or the trench wall of $8\ \mu\text{m} \times 8\ \mu\text{m}$ etch-holes are. The etch-hole is the shape of a nozzle and has some grass residue accordingly. The whole MEMS open area is actually a freestanding plate membrane mesh. The step-by-step 1P6M CMOS MEMS process is shown in Figure 4. Figure 4a shows the deposition of the polysilicon above the substrate; Figure 4b represents the CMOS layer with an additional pattern of contact layer; Figure 4c depicts the standard CMOS layer with amorphous SiO_2 , metal M1–M6, metal 7 hard mask, and a passivation layer; Figure 4d developed the thick photoresist layer to perform the patterning; lastly, Figure 4e,f shows anisotropic silicon oxide etching and XeF_2 isotropic silicon etching, respectively.

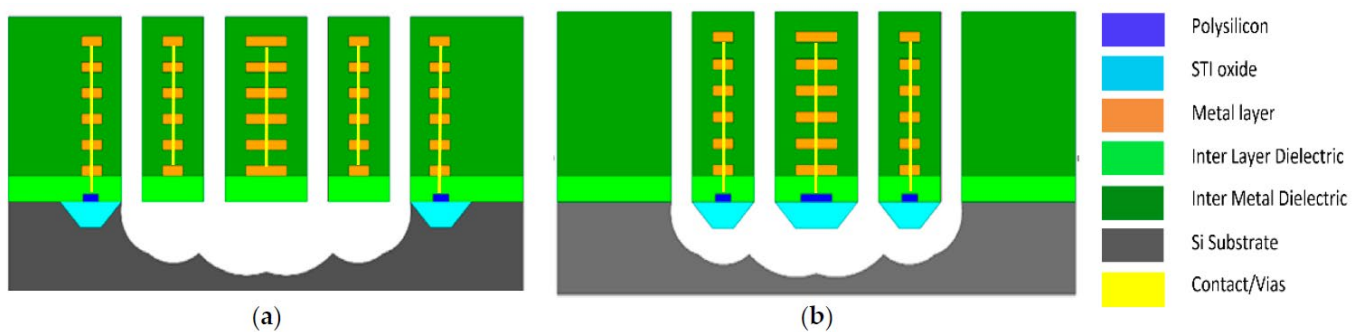
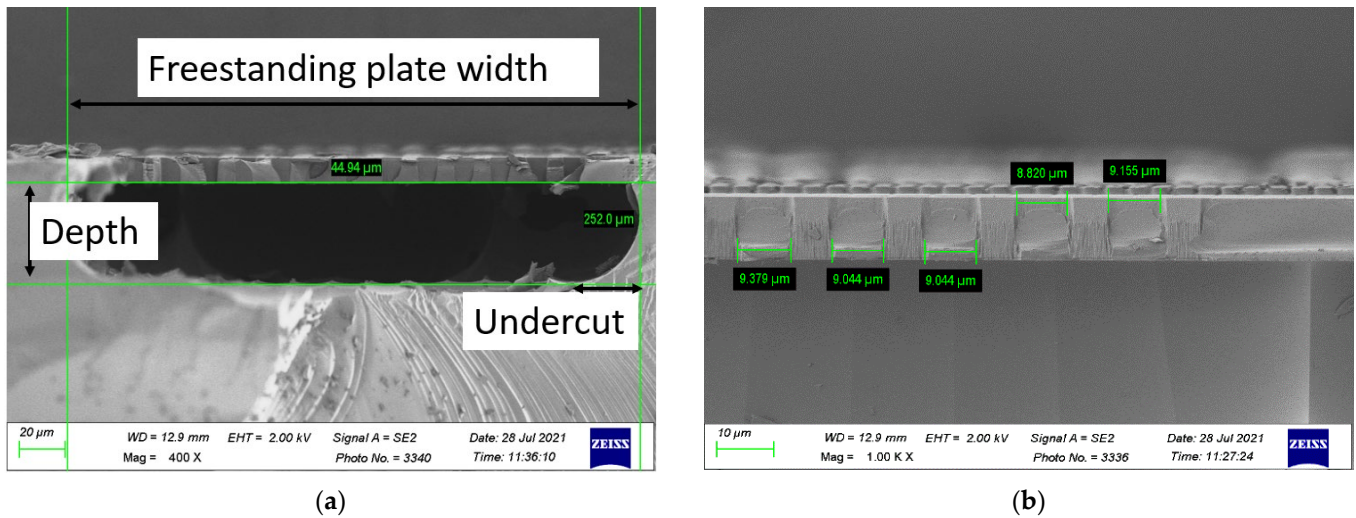


Figure 2. Chip cross sections after the current CMOS process provided by TSRI and UMC: (a) typical UMC 0.18 μm CMOS MEMS process with isotropic XeF_2 undercut etching for the MEMS open area; (b) alternative way in MEMS region using shallow-trench-isolation (STI; light blue) to protect polysilicon (dark blue) during XeF_2 etching.



(a)

(b)

Figure 3. (a) SEM of the MEMS area or the cavity after the undercut etching; (b) SEM of $8\ \mu\text{m} \times 8\ \mu\text{m}$ etch-holes (with measured $9.09 \pm 0.28\ \mu\text{m}$ in average) on CMOS layer. The MEMS area is freestanding plate with a membrane mesh.

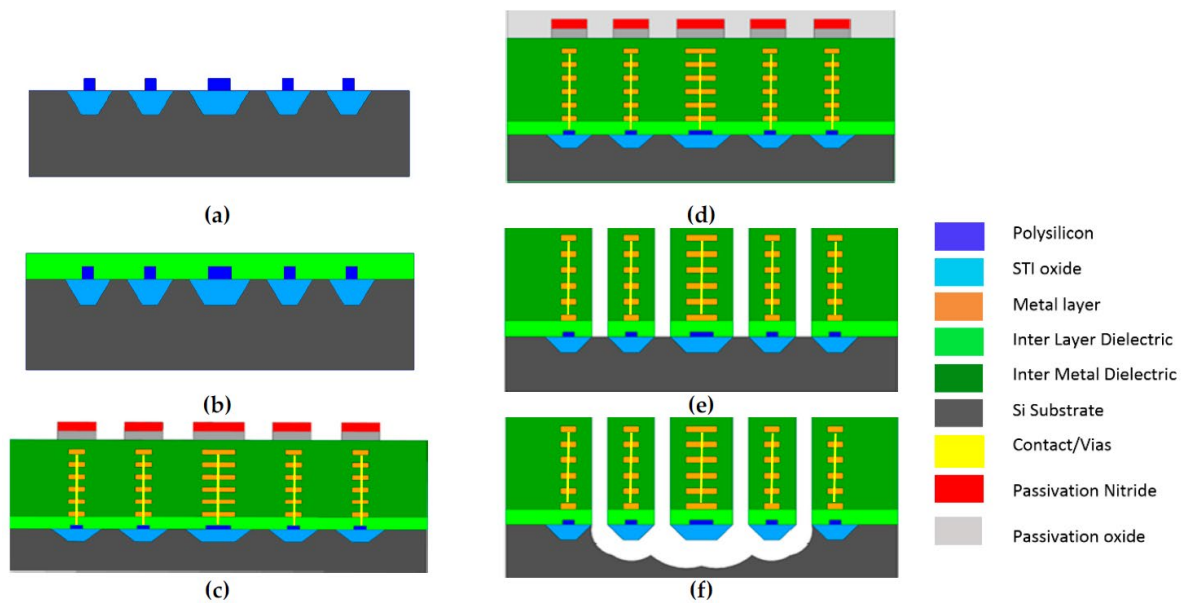


Figure 4. Step-by-step fabrication process of the CMOS MEMS foundry process: (a) depositing the polysilicon above the substrate; (b) the CMOS layer with additional pattern of contact layer; (c) the standard CMOS layer with amorphous SiO₂, metal M1–M6, metal 7 hard mask and passivation layer; (d) depositing the thick photoresist layer to perform the patterning; (e) anisotropic silicon oxide etching; (f) XeF₂ isotropic silicon etching.

The powerful CMOS MEMS foundry service in Taiwan has contributed to a variety of MEMS microsensors such as magnetic sensors [90,98–102], humidity sensors [103–108], gas sensor [54,63,109–112], pressure sensors [16,78,113–117], thermoelectric energy harvesters [118–122], strain sensors [37,40,53], thermal sensors [123–129], etc. Advantages such as calibration by digital programming, self-testing, and digital interfaces have been demonstrated. The CMOS MEMS processes technologies of the past several decades, not only limited to those from Taiwan, are summarized in Table 1. In the earlier stage, the CMOS MEMS process had a larger CD or minimum line width in the academic labs of Europe and USA [73–80]. As the CD kept on decreasing to $0.8\ \mu\text{m}$ [35] or even smaller than $0.6\ \mu\text{m}$ [90,113], $0.35\ \mu\text{m}$ [94,122,130–132], $0.18\ \mu\text{m}$ [96,100,102,109,112,128,133], and so on, the CMOS MEMS foundry service has still been running smoothly.

Table 1. CMOS MEMS processes technology followed in the past several decades.

Structure	Sacrificial	Interconnect	Process Technology	Applications	Year (Country)	References
SiO ₂	nitride	Si	Bipolar, triple diffused	pressure sensors	1979 (U.S.A)	[16]
polysilicon	oxide	silicon nitride	4 mask single sided process	neuron probe	1985 (U.S.A)	[18]
Al	oxide/nitride	Au, Cr	3 μm double poly single metal (2P1M)	mass flow sensor	1990 (U.S.A)	[19]
Al	photoresist	Al	1 μm	spatial light modulators (SLMs)	1990 (U.S.A)	[134]
polysilicon	oxide	W/TiN/TiSi ₂	3 μm	accelerometer	1992 (U.S.A)	[135]
polysilicon	oxide/metal	metal	Bulk/surface micromachining	thermal capacitor	1996/1997 (Switzerland)	[43,47]
poly-SiGe	Ge or SiO ₂	Al	3 μm	CMOS gate	1999 (U.S.A)	[136]
polysilicon	nitride	metal (Al)	0.8 μm double poly double metal (2P2M)	accelerometer	1997 (Taiwan)	[35]
poly, Al, Si, Cu	nitride	via	0.6 μm single poly triple metal (1P3M)	3D micro coil	1999 (Taiwan)	[90]
polysilicon	oxide	Al	0.8 μm	pressure sensor	1999 (Taiwan)	[113]
polysilicon	oxide	Al	0.35 μm single poly quadruple metal (1P4M)	bandpass filter	2001 (Taiwan)	[130]
nickel	oxide	TiN	0.35 μm/65 nm	micromechanical resonator	2008 (U.S.A)	[137]
AlN	Si	W/Ti/TiN	0.35 μm	precision oscillators	2009 (U.S.A)	[138]
Al	oxide	via	TSMC 0.35 μm	integrated resonator	2011 (Taiwan)	[131]
Al	oxide	via	0.35 μm	integrated resonator	2014 (Taiwan)	[132]
polysilicon	oxide	via	0.35 μm	flow sensor	2020 (Hong Kong)	[94]
n-type and n-type polysilicon	oxide	via	TSMC 0.35 μm	micro generator	2013 (Taiwan)	[122]
polysilicon	photoresist	Al	0.18 μm	capacitive accelerometer	2012 (Taiwan)	[133]
Al	oxide	via	0.18 μm	absolute pressure sensor	2013 (Taiwan, Singapore)	[139]
bimetallic nitride	polymer	W	0.18 μm	CMOS resonator	2015 (Malaysia)	[140]
AlCu	oxide	Ti/TiN	0.25 μm back end of line (BEOL)	accelerometer	2018 (Spain)	[141]
n-type silicon and p-type silicon	oxide	via	0.18 μm	magnetic sensors	2021 (Taiwan)	[102]
polysilicon, Al	oxide	via	0.18 μm	flow sensor	2021 (Taiwan)	[96]

Fabrication technologies during CMOS and CMOS MEMS processes include thermal conversion [94,141–145], chemical vapor deposition (CVD) [4,80,134], epitaxy [32,146–150], physical vapor deposition (PVD) [151–155], atomic layer deposition (ALD) [156,157], spin-on films/dielectrics [158–160], bulk micromachining [161], surface micromachining [51,113,135,162], photolithography module [163], dry etching, and wet etching. Most of the materials used for structural, sacrificial and passivation layers include silicon and its oxide, nitride, silicon-germanium, carbide derivatives, and other notable semiconductor and dielectric materials [133,136,164].

3. Post-Processes of CMOS MEMS Devices

The structures on general ICs are stacked densely and seamlessly. However, for most microsensors, freestanding membranes or suspension bridges are often required. MEMS post-processes help to release these freestanding microstructures after CMOS foundry service. Figure 5 shows all the different post-processes ever developed.

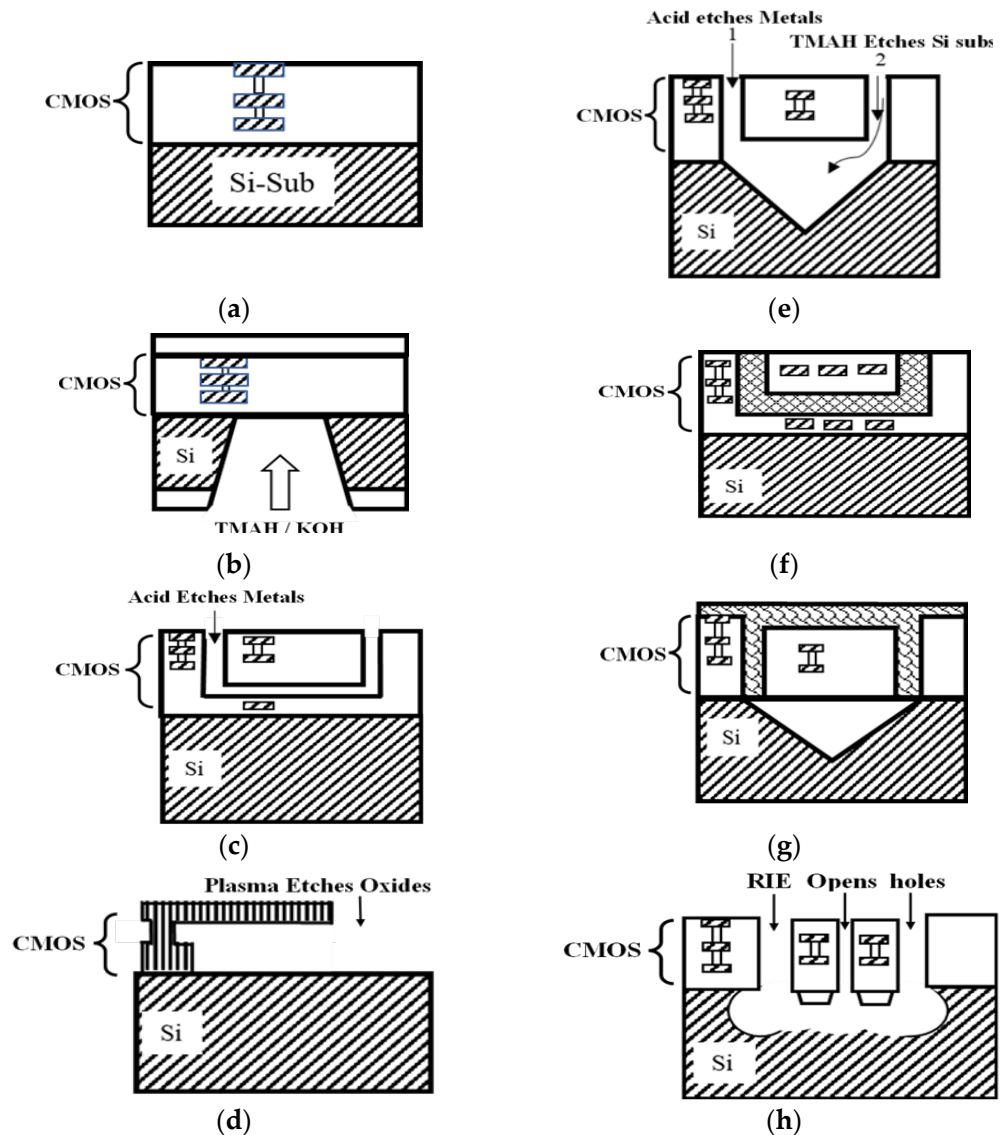


Figure 5. Post-processes ever used for CMOS MEMS in Taiwan: (a) CMOS silicon wafer; (b) backside wet etching using tetramethylammonium hydroxide (TMAH)/potassium hydroxide (KOH) for bulk micromachining [91,165]; (c) acid etch metals (surface micromachining) [35,37]; (d) deep trench plasma etching to release the cantilever [130]; (e) acid is used to etch metals and TMAH used to etch the Si substrate [57]; (f) electroplating Ni in the process (c) [90,137]; (g) parylene or gelatin is coated on process (e) [87,88]; (h) anisotropic and isotropic etching with STI protection [96,97,102,166].

Figure 5a shows the CMOS standard process, which is composed of four kinds of different thin films including silicon nitride (Si_3N_4), silicon dioxide (SiO_2), aluminum, and polysilicon on the silicon substrate. The arrangements of thin films in the order from bottom to top are silicon substrate, silicon dioxide, multiple metal layers with their inter-layer dielectrics (ILD), and the final passivation nitride layer on the top. When the semiconductor chip is stacked on the redistribution layer (RDL: metal interconnect that electrically connect one part of the package to another) and may have through holes for partially exposing the RDL, through the holes corresponding to the substrate pads and having conductive material filling through the holes, the uppermost semiconductor chip may have the same elements as the lower semiconductor chip and may be flip-chip bonded through the holes.

During the post-process of Figure 5b for fabricating a membrane, the backside of the silicon substrate was lapped and polished to reduce its thickness from $680\ \mu\text{m}$ to $200\ \mu\text{m}$.

This procedure decreases much time for backside V-groove etching and preserves the aluminum pads from being attacked by the exposed anisotropic etching solution. Then, it adopts low-temperature technology to deposit the masking films on the backside of the substrate. These masking films were 250 °C PECVD silicon nitride and sputtered silicon oxide at near room temperature. The thickness of PECVD silicon nitride is 0.4 µm and the sputtered silicon oxide is 1.2 µm, for example. After the infrared double-sided lithography, the masking film was patterned by reactive ion etching (RIE) with CF₄ plasma. The reason for the requirement of low temperature in MEMS post-process is that the CMOS aluminum layers may have problems of spiking or short circuits in an environment with a temperature higher than 350 °C. In the final step, ethylene-diamine pyrocatechol (EDP) or tetra-methyl-ammonium-hydroxide (TMAH) was used as the silicon anisotropic etching solution [117]. Such anisotropic solutions are good in etching the [1] silicon wafers, but etch-stop on the CMOS oxide layer. It also has good selectivity in metal preservation. The disadvantages are that it wastes the wafer area at the slope on the {111} [87,167] plane [161,165]; the backside photolithography needs to use a double-sided mask aligner; the wafer needs to be thinned and have an additional protective layer (PECVD nitride or sputtered oxide) [165].

The above drawbacks of the post-process Figure 5b are due to the backside V-groove etching [161,165]. When a metal layer is well-designed in advance and assigned to be the sacrificial layer in the post-process (Figure 5c), the sacrificial layer will be etched completely from the front side, and the silicon nitride layer will be released as a suspended structure in the micrometer scale. After all, this is a maskless post-process and needs a wet etching only. The sacrificial material is aluminum. Therefore, it is necessary to select an etchant which can remove aluminum selectively. One etchant recipe consisting of phosphoric acid (75%), nitric acid (5%), acetic acid (5%), and deionized (DI) water (15%) is adopted to etch a sacrificial layer at the temperature of 60 °C. Of course, this post-process needs etching holes from the front side to fabricate suspended open structures without difficulties, but it requires a hole-filling process subject to a membrane fabrication.

With the post-process shown in Figure 5d, the metallic suspension bridges can be created from the front side, and the sacrificial material is changed to oxide accordingly. Herein, the plasma etching is performed after the passivation nitride is removed and the top metal layer is exposed. Therefore, the top metal layer is used as the etch-resistant material during the subsequent dry etching that creates the laminated microstructure. Without wet etching, surface tension sticking does not occur, and the laminated-suspension microstructures are achieved. The anisotropic oxide plasma etches through to the silicon substrate by CF₄/O₂ RIE. By employing the large undercut of SF₆ RIE, 2.5 µm width of the beam could be released within 15 min [130].

Figure 5e is for releasing the suspension bridge structure of accelerometers, flowmeters, or infrared thermometers; the layers of the CMOS are opened with patterns and then also soaked in the anisotropic etching solution to attack the silicon substrate frontside.

Choices of highly selective etchants are listed in Table 2 and remove different sacrificial layers including “contact”, “metal”, and “via”. The etchant-(1) is used to etch the Ti-W alloy (the “contact” and “via” layers). Etchant-(2) is used to remove the aluminum (the “metal” layer.) The sacrificial layers etching process involves: first, clean the CMOS sensor die with the acetone, isopropyl alcohol (IPA), and DI water. Second, the die is immersed in etchant-(2) maintained at 70 °C for 50 min. Third, immerse the die in etchant-(1), maintaining the temperature at 70 °C for 30 min. Repeat the etching-(1) and etching-(2) for five times to remove the sacrificial metal layers clearly. The silicon anisotropic etching may use the etchant-(3) finally to release the diaphragm.

An inverted pyramid or V-groove is formed under the suspension bridge floating structure by this post-process of front-side etching herein. The good point is that there is no hole-enlarging problem for the {111} slope, and the depth of the V-groove does not have to be etched through the silicon substrate as in the second type post-process. The disadvantage is that the cross-section of the multi-layer suspension bridge structure is easily invaded into the gaps between the layers by the etching solution of the silicon crystal, destroying the

deposited embedded metal and polysilicon layers. In addition, when the CMOS foundry is completed, the silicon nitride protective layer is patterned at the metal contacts (I/O pads) on the front side of the wafer [168]. Therefore, when the silicon crystal is anisotropically etched, care should be taken to ensure the selectivity of the etchant to silicon and metals. In the formation of the bridge floating plate or even the first post-process on membrane, the metal contacts cannot also be sacrificed. Usually, the first two post-processes use EDP or TMAH [88].

Table 2. Post etching recipe of CMOS sensor.

Metal	Etchant	Formula
Ti-W alloy	(1) H ₂ SO ₄ : H ₂ O ₂	3:1
TiN-Al/Si/Cu-Ti	(2) H ₃ PO ₄ :HNO ₃ :CH ₃ COOH:H ₂ O	14:1:2:3
silicon	(3) TMAH	25%

An example of the CMOS post-process of Figure 5f is, for fabricating the magnetic coil [90], in view of the production of magnetic coils and based on the consideration of reducing the magnetic loss of general semiconductor materials, a micro-electroforming process must be added after the post-process Figure 5c. The coil structure is basically divided into a ferro-core and a conductive winding around it. The metal layers (M1 and M3 in Figure 1) and the via of the CMOS process can be re-wrapped to form a 3D coil, and the center core needs to be ferromagnetic. The main spirit of electroforming is that the metal layer M2 in Figure 1 is designed as a core shape, but the two ends are exposed. After all the CMOS structures are grown and stacked, the M2 aluminum core of the central core portion is etched by an acid solution firstly, and a microchannel is formed. The polysilicon or titanium is used as a seeding layer to infiltrate the iron–nickel electroforming liquid, and the electroformed iron-nickel alloy is grown and filled into micro-channels. In the channel, it acts as a high permeability iron core microstructure.

Figure 5g is after the post-process of Figure 5e and works for fabricating membranes for pressure sensors. Then, the CMOS sensor die is packaged by the wire-bonding and cavity sealing before testing. For ensuring the well function of the CMOS pressure sensor, one must seal etching holes on the diaphragm after the post etching to isolate the cavity from the ambient environment. The authors used a reversible thermoplastic gelatin to seal the etching holes [87,88]. A room-temperature growth parylene is also suitable for sealing the etching holes in a dry manner [89].

The post-process Figure 5h is the UMC-0.18 μm CMOS MEMS process of Figure 4, which includes the anisotropic silicon oxide etching process and isotropic silicon etching process. The post-process included an anisotropic dry etching with CHF₃/O₂ RIE to remove the sacrificial oxide layer and an isotropic dry etching with gas-phase XeF₂ to etch the silicon substrate. The isotropic XeF₂ undercut etching is for the MEMS open area. The detailed explanation has been given in Figures 2–4. STI oxide is used to protect polysilicon during XeF₂ etching [96,97,102,122].

4. Case Study of Flow Sensor Using UMC 0.18 μm CMOS MEMS Process

CMOS MEMS technology has been utilized in recent times for the fabrication of low-cost micromachined flow sensors [4,62,161,168–170]. Flow sensors are the key elements in most systems for monitoring and controlling fluid flows. With the design of MEMS thermal flow sensors, unprecedented performances, such as ultra-wide measurement ranges, low power consumptions, and extreme size miniaturization were targeted, although several critical issues remain still to be solved.

After obtaining the consent of CIC, the authors developed the manufacturing flow of CMOS MEMS sensors, as shown in Figure 6. In the design system, after creating a library, one can choose schematic or Virtuoso according to our need. The schematic editor used in this case is called Composer, ADS. The model simulator used is H-spice, Spectre. The

simulator can run the Netlist pre- and post-simulation after verification being performed in Calibre.

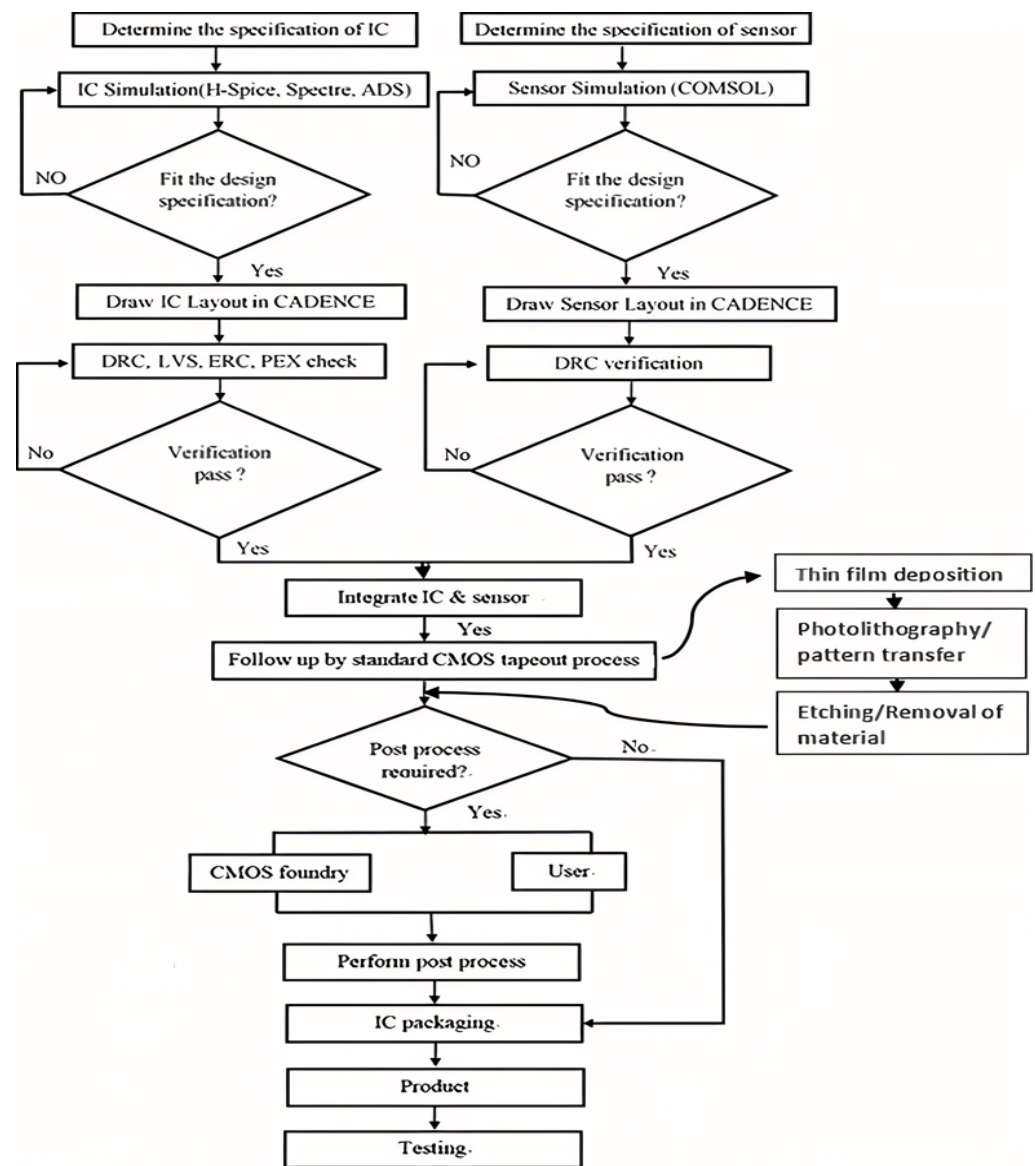


Figure 6. CMOS microsensor fabrication process. Analysis of analog circuit behavior is performed by H-Spice, Spectre, and ADS software; analysis of simulated sensor behavior is performed by COMSOL or ANSYS, which is combined with related sensing principles. Both the circuit layout and sensor layout use the same CMOS material layers. However, in the layout verification part, the sensor must pass DRC at most (under some special conditions can even relax certain DRC rules).

4.1. CMOS MEMS Sensor Design Flow

In the following, the authors took the flow sensor design as an example to verify the CMOS MEMS process of Figure 6. The work builds on a fabrication process reported at Transducers-2021 [96], revealing that CMOS MEMS technology can generate minimal space utilization micromachined flow sensors. The flow sensor was designed with a self-heating half-bridge RTD or a hot wire that did not use any heater during the operation. This concise device size can be in the range of 100 μm and ideally fabricated by the CMOS MEMS process. The amplifier was also added later to the sensor design. Numerous micromachined thermal flow sensors have been surveyed for different materials and applications including

battery-free, wireless devices, nano mechanical sensor [171], infrared sensors [172–176], and calorimetric sensors [144,177–180]. The high-quality CMOS foundry services provided by TSMC and UMC foundry were highly welcome over the past two decades. The CMOS MEMS foundry is therefore one of the best candidates so far to implement the new MEMS sensor design and fabrication. Another major advantage for this kind of flow sensor is its low power consumption.

4.2. Flow Sensor Design

Initially, the design of the flow sensor was conducted with a self-heating or hot-wire type where it did not use any additional heater during the operation. The self-heating of the RTD bridge circuit was originally a noise problem and a shortcoming to the thermal flow sensors. We conventionally needed to eliminate this noise by ways of reducing excitation (sensing) current or using pulse measurements. We only adopted a bridge circuit composing of 2 RTDs, R_1 and R_2 , in series, as shown in Figure 7a. The self-heating voltage V_0 is no more a noise, but the bias to the RTD half bridge is necessary for the device operation. Resistor R_1 is on the substrate, and R_2 is on the MEMS cavity or the free standing plate region, which provides good thermal isolation [96]. T_1 is the local temperature on the substrate, and T_2 is on the MEMS cavity with air gap underneath, accordingly. Figure 7b shows the layout diagram of the flow sensor with an amplifier circuit drawn in Cadence software. The amplifier circuit will be mentioned in Section 4.3 [180].

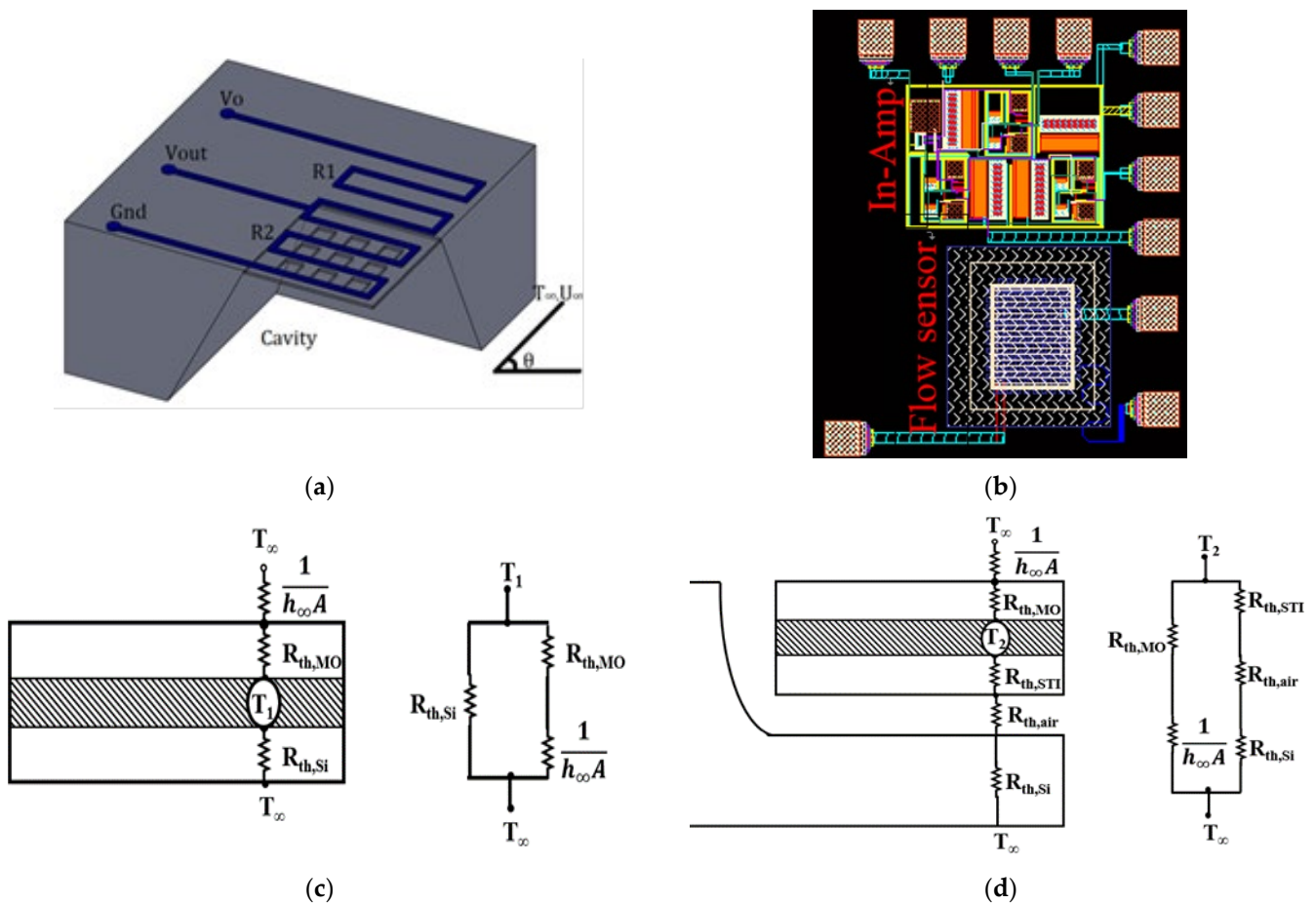


Figure 7. Flow sensor design: (a) the self-heating half-bridge RTDs R_1 and R_2 ; (b) layout diagram of flow sensor and amplifier; (c) 1D thermal resistance (R_{th}) model of the RTD R_1 with T_1 on Si substrate; and (d) 1D thermal resistance model of the RTD R_2 with T_2 on the floating MEMS area with air gap.

By the one-dimensional (1D), steady state thermal resistance analysis of heat conduction about the silicon substrate and the MEMS cavity area, the simplified models are

assumed in Figure 7c,d, respectively. The heating or bias power q from the RTDs diffuses to ambient by ways of the convective cooling on the top and the conduction on the bottom (“//” means two thermal resistances in parallel). Using the Fourier law of heat conduction [181], the temperature differences $\Delta T_{1,2} = (T_{1,2} - T_{\infty})$ related to the heat transfer rate q are shown in Equations (1) and (2).

$$\frac{T_1 - T_{\infty}}{\left(\frac{L_{Si}}{k_{Si}A}\right) // \left(\frac{1}{h_{\infty}A} + \frac{L_{MO}}{k_{MO}A}\right)} = q = \frac{V_0^2}{4R_0} \quad (1)$$

$$\frac{T_2 - T_{\infty}}{\left(\frac{L_{Si}}{k_{Si}A} + \frac{L_{STI}}{k_{SiO_2}A} + \frac{L_{ca}}{k_fA}\right) // \left(\frac{1}{h_{\infty}A} + \frac{L_{MO}}{k_{MO}A}\right)} = q = \frac{V_0^2}{4R_0} \quad (2)$$

In addition, the heat transfer coefficient h_{∞} relates to the flow speed U_{∞} by the laminar boundary layer theory, as in Equation (3) or Equation (4), subject to a flat plate under the medium value of the Reynolds number flow [182]. Substituting Equation (4) into Equations (1) and (2) can correlate the temperature difference and the flow speed.

$$Nu = \frac{h_{\infty}x}{k_f} = 0.664(Re^{1/2})(Pr^{1/3}) = 0.664Pr^{1/3}\sqrt{\frac{U_{\infty}x}{\nu}} \quad (3)$$

$$h_{\infty} = 0.664k_fPr^{1/3}\sqrt{\frac{U_{\infty}}{\nu x}} \quad (4)$$

where

A : Area of chip ($300 \mu\text{m} \times 250 \mu\text{m}$)

ΔT : Temperature difference

h : Convective heat transfer coefficient.

L_{Si} : Thickness of silicon ($400 \mu\text{m}$)

L_{MO} : Thickness of metal ($9.76 \mu\text{m}$)

L_{STI} : Thickness of STI ($0.4 \mu\text{m}$)

L_{ca} : Thickness of air cavity ($45 \mu\text{m}$)

K_f : Thermal conductivity of air (0.025 W/m K)

K_{Si} : Thermal conductivity of silicon (148 W/m K)

K_{MO} : Thermal conductivity of metal (237 W/m K)

K_{SiO_2} : Thermal conductivity of silicon dioxide (1.3 W/m K)

Nu : Nusselt number

Pr : Prandtl number (0.73 for air)

q : Heat transfer rate

Re : Reynolds number

R_0 : Heater resistance in ohm

$T_{1,2}$: Surface temperature of positions 1 and 2

T_{∞} : Ambient temperature ($25 \text{ }^{\circ}\text{C}$)

U_{∞} : Freestream flow speed ($1\text{--}10 \text{ m/s}$)

V_0 : Power supply (1.8 V)

ν : Kinematic viscosity (viscosity/density) of the air at $25 \text{ }^{\circ}\text{C}$ ($15.52 \times 10^{-6} \text{ m}^2/\text{s}$)

x : Sensor bridge length occupied by the sensor on the chip. ($167.5 \mu\text{m}$)

We have taken R_0 as the design resistance value ($1 \text{ k}\Omega$) of one RTD with the temperature coefficient of resistance ($\text{TCR} = 2.97^{-3}/^{\circ}\text{C}$). As the flow speed increases across the biased RTDs, both RTDs have a temperature drop, but the cooling effect of R_1 on the silicon substrate is better than R_2 on the MEMS cavity with air gap thermal isolation. So, the temperature difference $\Delta T_2 = T_2 - T_{\infty}$ of R_2 is greater than $\Delta T_1 = T_1 - T_{\infty}$ of R_1 . The values of R_1 and R_2 after application of flow speed can be shown below.

$$R_2 = R_0[1 + (\text{TCR})(T_2)] \quad (5)$$

$$R_1 = R_0[1 + (TCR)(T_1)] \quad (6)$$

The output voltage of the half-bridge is therefore approximated as Equation (5) following the temperature difference between two RTDs by the voltage divider formula and the binominal theorem, as below.

$$V_{out}/V_0 \approx (0.5)[1 + (TCR)(0.5)(T_2 - T_1)] \quad (7)$$

Combining Equations (1), (2), (4), and (7), we can correlate the output voltage V_{out} and flow speed U_∞ . By this theoretical formulation, the output voltage change is first estimated as 0.125–0.5 mV by 1 V DC bias per 1 m/s flow speed change if the TCR values are 500–2000 ppm/K. The authors moreover predict the theoretical output voltage in Figure 8a.

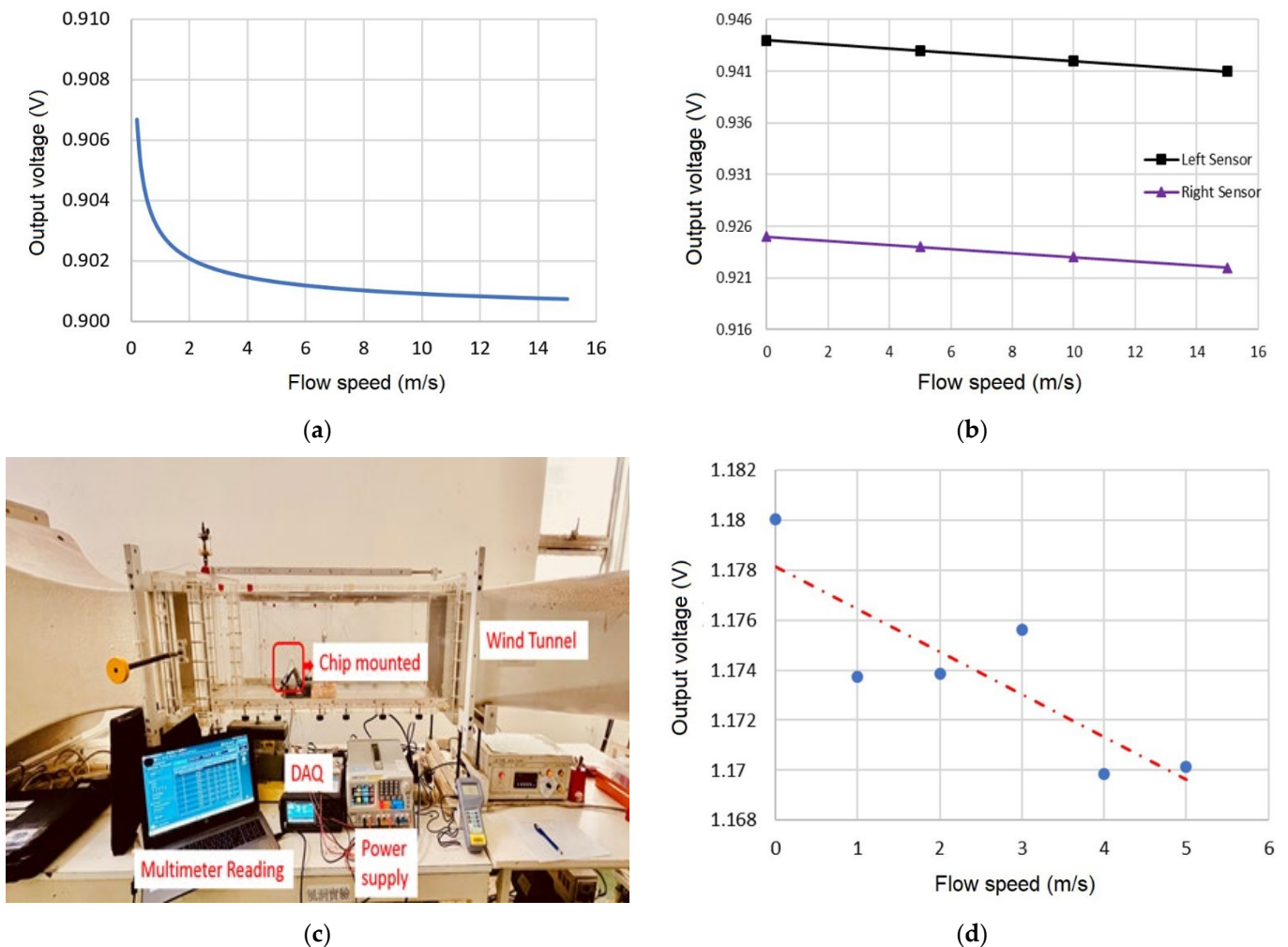


Figure 8. Flow sensor output voltage vs. flow speed: (a) theoretical prediction by Equations (1), (2), (4), and (5); (b) testing result of the fabricated CMOS MEMS self-heating flow sensor; (c) wind tunnel facility for flow sensor testing; and (d) testing result of the fabricated CMOS MEMS self-heating sensor with integrated amplifier circuit in Section 4.3.

Based on the UMC 0.18 μm standard 1P6M CMOS foundry with the MEMS post-process shown in Figure 4, the flow sensor was implemented with cavities underneath the freestanding plates of multiple metals M1–M6 and ILD.

According to the theoretical values of Figure 8a, the output voltage Figure 8b of the fabricated flow sensor by UMC 0.18 μm MEMS process was verified by a wind tunnel facility in Figure 8c. Preliminarily, the theoretical sensitivity of 113 $\mu\text{V}/\text{V}/(\text{m/s})/\text{mW}$ is

near to the measured sensitivity $138 \mu\text{V}/\text{V}/(\text{m/s})/\text{mW}$ under the flow speed of 15 m/s ; the linearity of the measured output voltage is obviously better than the theoretical one. The reason why the sensitivity of the theoretical output voltage was underestimated is that the actual flow speed was lower than the freestream speed, U_∞ . The amount of flow speed retarding from the freestream inside the boundary layer of the flow sensor surface could be furthermore investigated by FEAs such as ANSYS or COMSOL. The 18% sensitivity difference between the theoretical and experimental data corresponds to factors such as packaging design and resistance variation during the semiconductor fabrication.

4.3. Instrumentation Amplifier Design

The instrumentation amplifier (In-Amp or IA) shown in Figure 9a can amplify the output signal of the above CMOS MEMS flow sensors. MEMS flow sensors are often based on temperature detection. For most materials, the electrical resistivity changes with temperature. IA is a type of differential amplifier that has been outfitted with input buffer amplifiers, which eliminate the need for input impedance matching and thus make the amplifier particularly suitable for use in measurement and test equipment. Additional characteristics include a very low DC offset, low drift, low noise, very high open-loop gain, very high common-mode rejection ratio (CMRR), and very high input impedances. IAs are used where great accuracy and stability of the circuit for short-term and long-term are required [183]. Using materials with the appropriate TCR permits us to achieve a high sensitivity to temperature changes and thus to flow speed. Integration on the same chip will contribute to a more precise output, sources of error will be minimized, and fault-prone solder points will be eliminated [184].

The IA layout consists of three operational amplifiers circuits in Figure 9b, which always has difficulty in equalizing two $R_1 \sim R_3$ values in the layout of Figure 9a for real CMOS fabrication. It therefore gives a testing result of 30 dB gain only under the bandwidth of 10 kHz. The DC level also deviates from the design value of $V_0/2$. With the supply voltage as $V_0 = 1.8 \text{ V}$ and reference voltage as 1 V , the total current consumption is 1.335 mA .

The half-bridge output voltage of Equation (5) has a DC level of $0.5 V_0$. Although it does not affect the sensitivity, the DC level should be reset to zero. Using the IA of Figure 9, the DC level is easy to eliminate by assigning the $V_1 =$ sensor output voltage and $V_2 = 0.5 V_0$. Again, due to the difficulty in equalizing two $R_1 \sim R_3$ values in the layout of Figure 9a for real CMOS fabrication, the DC level cannot be exactly eliminated. This deficiency can be observed from the output voltage of the amplified output voltage of the flow sensor in Figure 8d.

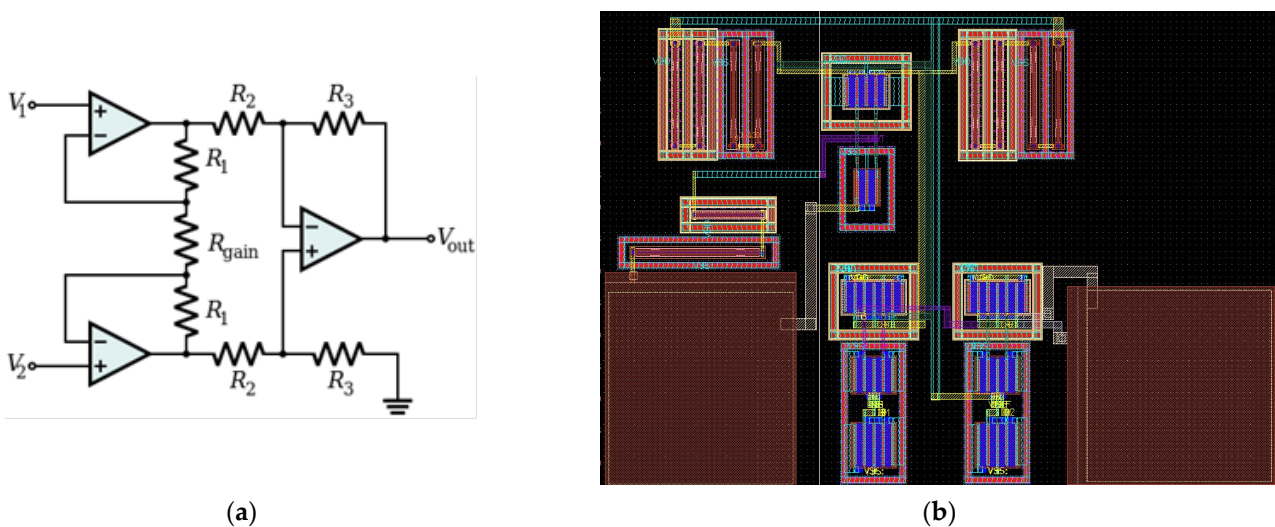


Figure 9. Instrumentation amplifier (IA): (a) circuit diagram of the IA; (b) layout diagram of single stage op-amp of the IA drawn in Cadence software.

With the on-chip integration IA of Figure 9, the authors redid the wind tunnel testing on the CMOS MEMS flow sensor. The overall sensitivity of the integrated flow sensor was improved to $1388 \mu\text{V}/\text{V}/(\text{m}/\text{s})/\text{mW}$ for a flow speed ranging within 0–5 m/s, as plotted in Figure 8d. The voltage gain discussion will be addressed in the next section.

5. Results and Discussions

The following advantages and technical issues of CMOS MEMS technology are discussed by the case study of flow sensors:

5.1. Smaller Device Size

Technology has been pushed to the point that we can build a device so small that it can hardly be seen with our human eye. The typical size of MEMS devices is usually measured in micrometers. Using similar fabrication techniques as in building ICs, people are now able to build sensors and actuators on the same microscopic level with the processor chip. Measured in micrometers, almost all MEMS sensors and actuators can be batch-produced together on the same chip with circuitry. They indeed compose a system on a chip as small as possible according to the CMOS technology now [153].

The flow sensor is made with the latest U18MEMS CMOS MEMS process, which was discussed in Section 4.2. The dimensions of the flow sensor were miniaturized to save the chip area and achieve an acceptable sensitivity and linearity. The sensor size herein was $300 \mu\text{m} \times 250 \mu\text{m}$ in Figure 7a,b, which is smaller than many prior arts'. Within the flow speed range of 0–15 m/s in a wind tunnel, a normalized sensitivity of this small CMOS MEMS sensor was obtained as $138 \mu\text{V}/\text{V}/(\text{m}/\text{s})/\text{mW}$, which is with the same order of magnitude to the best value of $160 \mu\text{V}/\text{V}/(\text{m}/\text{s})/\text{mW}$ of the prior arts [59,60,62,76,93,94,97,185].

5.2. Less Power Consumption

With enhanced sensitivity and less power consumption with only one RTD self-dissipating power of 0.81 mW, we can say that signal-to-noise ratio (SNR) is better as the sensitivity was able to measure without any readout circuit [96,186]. In a digital viewpoint, the small voltage swing results in a small noise margin. In the analog domain, the strength of signal level is weakened due to the low supply voltage. The total power consumed by the flow sensor with IA is 3.24 mW. Other designs such as calorimetric-type flow sensors consume more power due to the additional center heater for adjusting the output performance [59,93,94,181].

5.3. Enhancing the Sensing Sensitivity by On-Chip Amplifiers

Adding on-chip amplification circuits to the RTD flow sensors may result in a different behavior of the sensor output sensitivity compared to the one without amplifier circuitry. Addressing the above challenge requires the collaboration of MEMS and analog circuit design engineers. The case study of the self-heating RTD flow sensor alone gives a normalized output sensitivity of $138 \mu\text{V}/\text{V}/(\text{m}/\text{s})/\text{mW}$ under the flow speed of 15 m/s. With the measured gain of IA as 30 dB calibrated at 10 kHz, and by integrating it into the self-heating RTD sensor, the overall sensitivity is improved to $1388 \mu\text{V}/\text{V}/(\text{m}/\text{s})/\text{mW}$ for flow speeds ranging within 0–5 m/s in Figure 8d. The overall voltage gain is 20 dB smaller than the calibrated value of 30 dB. In other words, the CMOS flow sensor with on-chip IA was observed to have 10x better sensitivity.

5.4. Other Technical Issues of CMOS MEMS Process

5.4.1. Residual Stress and Resistivity of the CMOS Layers

In the surface micromachining, reducing the residual stress of the microstructure is an issue involving the warping of the microstructure after its release and suspension by removing the sacrificial layer, or even causing the adhesion or stiction to the silicon substrate. The phenomenon of the device failure is that the suspended micro structures, after CMOS fabrication and post-processing, have some unavoidable residual stress where

the CMOS process is not able to adjust the process parameters as the polysilicon structure layer is grown in the LPCVD of surface micromachining. The residual stress problem can be minimized by avoiding the cantilever structure (because the free end will arbitrarily turn up or bend down) or I-beam configuration [130]. Instead, one can use a thin bridge or membrane design (e.g., Figures 2–4) to resist the residual stress by the rigidity of the structure. The residual stress state of each structural layer of CMOS materials, including information such as tensile stress or compressive stress, magnitude, etc. cannot be obtained from the technology file of the foundry service. Therefore, a concept of “test key” may be necessary to develop the mechanical parameter monitoring technology of the semiconductor process by an onsite sensing way [37,92,165]. The microstructure of the in-situ gauge or test key showing mechanical behavior such as residual stress/strain and mechanical properties such as Young’s modulus and Poisson’s ratio.

Similarly, the resistivity or TCR values of polysilicon and metal layers in CMOS layers cannot be identified very accurately from the technology file of the foundry service, either. This is the reason why the theoretical prediction of 1D thermal resistance model in Figure 8a deviates away from the measured data Figure 8b so obviously. For perfecting the CMOS MEMS sensor design in the future, allocating some small area with test keys for in situ measuring the resistivity and TCR values is mandatory.

5.4.2. Monolithic Integration of MEMS and CMOS Circuits

Finally, the ideal monolithic MEMS device, although it can be directly implemented in a CMOS foundry service, has some problems that need to be solved. The biggest difficulty lies in the integration of the circuit functions because the IC design software cannot directly simulate the output signal changes caused by the MEMS sensor. For example, the sensing capacitor or RTD is only a value-fixed capacitance or resistance in Cadence. H-Spice may predict the relationship between the pre-drive bias voltage and the output voltage but cannot capture the model in which the sensing capacitance or resistance changes.

The so-called “on chip” in the circuit function still lacks real integration with MEMS sensors. It means that only the MEMS sensing element and the signal processing circuit are fabricated on the same silicon chip physically (for the CMOS MEMS chip, the process and the material are already compatible). However, there is no circuit model available for the MEMS devices. Therefore, the overall system optimization of MEMS and IC devices cannot be performed yet in the Cadence software so far. In the existing operation of the Cadence software, the signal processing circuit first completes all the verification procedures, and then it is put together with the layout of the MEMS sensor that is verified by the DRC only. Finally, it is sent directly to the foundry production. After the foundry service, the basic functions of ICs are firstly tested, and then the “hybrid” connection is performed nearest to the wire bonding pads to realize the physical sensor test totally. (This is what the authors actually have completed about the integration testing of the amplified flow sensor output in Figure 8d). For the successful integration of MEMS and circuitry function by CMOS MEMS in the future, there are several difficulties needed to be overcome.

6. Conclusions

The authors have summarized the CMOS MEMS techniques and processes used during the design of various kinds of sensors. Design applications mentioned in this paper such as flow sensor and instrumentation amplifier (IA) were made using the latest U18MEMS process, which is a combination of the UMC 0.18 μm 1P6M process along with the MEMS post-process of XeF_2 etching by TSRI. Moreover, a potential sensors system-on-chip (SOC) through CMOS–MEMS technology becomes feasible to be widely implemented in smart living communities. The latest process shows that by employing CMOS-based fabrication technologies, we can monolithically integrate MEMS devices and their associated application-specific ICs, thereby enhancing their overall performance as compared with their stand-alone counterparts. As a case study herein, the CMOS MEMS flow sensor with on-chip IA was observed to have 10x better sensitivity than a flow

sensor alone. This self-heating RTD bridge alone gives a normalized output sensitivity of $138 \mu\text{V}/\text{V}/(\text{m}/\text{s})/\text{mW}$ for a flow speed under 15 m/s. With the measured gain of IA as 30 dB, and by integrating it with the afore-mentioned flow sensor, the overall sensitivity is improved to $1388 \mu\text{V}/\text{V}/(\text{m}/\text{s})/\text{mW}$ for a flow speed within 0–5 m/s. The integrated voltage gain is observed as 20 dB subject to DC air-flow impinging. This foundry service of CMOS–MEMS processes will be useful as it leads to a smaller size and less power consumption with enhanced sensitivity response and could be widely applied to more smart or intelligent fields, e.g., the operation monitoring of wind turbines and biomimetic flights, etc. Although this study aimed to report the development processes of past and present CMOS MEMS processes, the author additionally validates the current processes and techniques with a design of flow sensor while using polysilicon as the design material so that it can then be implemented in any flow-sensing applications. It is important to note that this may be an appropriate moment to list a few more semiconductor materials for their high voltage, high frequency applications. In the upcoming years, many small companies, serving niche markets with special processes using different material such as SiC, GaN, etc., may make medium-cost IC's and sensors and will coexist alongside a few large IC industries, producing inexpensive smart sensor systems for mass markets, which may indeed fulfill the current high demand, leading to chip shortage. CMOS MEMS processes have already become an integral part of all the electronic devices, vehicles, biomedical devices, etc., and looks to be a promising and fruitful field of scientific research for the years to come.

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