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Design Methodology Based on Prebuilt Components for Modular Multilevel Converters with Partial Integration of Energy Storage Systems

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Abstract: To provide ancillary services in HVDC applications, modular multilevel converters (MMCs) with integration of energy storage systems are a promising solution as they take advantage of the modularity and the controllability of the stored energy. In these solutions, an energy storage system is connected to the DC capacitor of a submodule (SM) to make an energy storage submodule (ES-SM). An MMC with partial integration (MMC-PIES) is an MMC with each arm made of a mix of SMs and ES-SMs. In this paper, we propose a novel design methodology for these converters considering they are built based on existing prebuilt submodules, while design methodologies in the literature consider the SM and ES-SM characteristics to be degrees of freedom. Therefore, the proposed approach is closer to an industrial standpoint and computes the minimum number of ES-SMs to comply with requirements. We also include a new optimization method for the circulating currents needed to balance the energy in the SM and ES-SM capacitors. Design scenarios are presented. The results show that the value of the DC capacitance and the current limitation of the switches highly influence the design, restricting the possible operating points. In addition, half-bridge ES-SMs seem to be a more promising solution than full-bridge ES-SMs, reducing the number of ES-SMs.

Keywords: high-voltage direct current (HVDC); power converter; modular multilevel converter (MMC); ancillary services; energy storage system; design methodology

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1. Introduction

The growth of renewable energy sources and the liberalization of the electricity market have made it more difficult to ensure an affordable and secure supply of electrical energy. The introduction of numerous intermittent sources of energy that are geographically spread and the increasing power that must be transmitted through transmission lines have imposed new constraints on existing AC power transmission systems. High-voltage direct current (HVDC) appears to be an attractive solution to transmit more power across long distances, and therefore, to connect large offshore windfarms in a more economical and environmentally friendly way or to interconnect asynchronous areas [1]. Thus, numerous HVDC point-to-point, multi-terminal or even grid projects have emerged during recent years [2].

Due to remarkable advances in power electronics, voltage source converters (VSC) are now the reference conversion structure. Regarding former line commutated converters (LCCs), they allow greater controllability and lower harmonic content. Among all the various topologies, the modular multilevel converter (MMC), patented by R. Marquardt in 2001 [3], has become the most attractive converter technology in high voltage applications, due to its low switching losses, voltage scalability, reliability, and to the control of its internally stored energy [4].

The decommissioning of conventional power plants, at the same time as the increased penetration of power electronic devices in the grid, have led to a stronger need for flex-

ibility from transmission system operators (TSOs) [5]. In particular, as fewer and fewer traditional synchronous generators are coupled to the grid, and as power converters do not provide inertia [6], the kinetic energy needed to maintain system stability is decreasing. Consequently, the existing dynamics of system frequency is inevitably altered.

On the one hand, multi-megawatt standalone energy storage systems have been implemented during recent years to enhance system stability [7,8]. On the other hand, MMCs have energy stored within their submodules (SMs). This complex topology offers a degree of freedom to control this internal energy as compared with conventional VSCs. Unfortunately, MMCs are not usually sized to store enough energy to provide ancillary services as grid scale energy storage systems [9]. From that perspective, studies in the literature have considered adding an energy storage system to draw the utmost of this degree of freedom, and then the provision of ancillary services would be feasible. Therefore, the integration of energy storage systems within MMCs have received significant interest in recent years [10–17]. Notably, a CIGRE working group (WG B4-84) was recently created in 2021 to deal with the feasibility and application of electric energy storage systems embedded in HVDC systems. Although, the classification of ancillary services is large, and varies between system operators, due to space limitations, MMCs with integrated energy storage systems are well suited for services that require low energy capabilities. Similarly, it is reasonable to not significantly affect the design of the converter station if it represents only a fraction of the power rating of the MMC. In that way, short-term ancillary services have been targeted, and particularly, the new fast frequency response services [18,19] or the power oscillation damping [19].

MMCs are well suited for this purpose since they rely on several stacks, or arms, of low-voltage cascaded SMs. Several approaches have been explored in recent years. In [14], a cascaded H-bridge branch that was parallel with a portion of an arm is used to provide an integrated energy storage system; [15] proposed a storage that was parallel with the arm inductors. However, the modularity of an MMC allows the energy storage elements (ESEs) to be implemented locally within each SM to make energy storage submodules (ES-SMs). The energy storage elements can be controlled independently, decoupled from the DC bus voltage of the converter, and its design eased by taking advantage of its high scalability. However, each of the ESEs must withstand the submodule capacitor voltage (usually a few kV) with low-frequency components. Although passive methods were first proposed [17,20,21], a DC/DC interface converter was compulsory to optimize the design of the ESE, to decouple its energy management, and to improve its lifetime [10,16,22,23]. From a technological point of view, ref. [16] showed that a modular DC/DC interface converter based on MOSFETs was remarkably suited, when the ratio between the converter station power rating and the active power service provided by the energy storage was low.

Since including ESEs in hundreds of SMs may not be compact or economically viable, uneven distribution among arms has been proposed. The motivation is to obtain a smaller and more cost-effective solution by reducing the number of ES-SMs [24,25]. The internally stored energy can be balanced, but at the cost of high circulating currents. This can be avoided if each arm has the same structure. Thus, an MMC with partial integration of energy storage (MMC-PIES) has been thoroughly studied. The six arms of the converter contain a mixture of standard SMs and ES-SMs. This topology is promising because it would reduce the impact on the existing rating of the station, while extending its capability [13,26–29]. The concept has been experimentally validated in [30]. However, it has been identified that, at a reduced power level of the converter, the arm currents are too low to allow the required energy exchange between SMs and ES-SMs [13,26]. Therefore, additional circulating currents, with no impact on the DC and AC sides of the converter, have commonly been injected. The relevancy of this solution was confirmed in [26] where it was shown that an MMC-PIES with half-bridge ES-SMs and adequate circulating current injection could be a promising solution. Moreover, the required number of energy storage elements could be decreased, while having a minor impact on the capacitance values and the volume of the submodules. Nonetheless, this solution also has constraints. For example,

the maximal amplitude of the arm current is restricted by the current limitation of the submodule switches, while the voltage ripple at the submodule capacitor is dependent on the amplitude of the arm current. Therefore, the first challenge addressed in this paper is to minimize these circulating currents. Then, optimization of the circulating currents to fully exploit the operational limits of the converter and limit losses is proposed in the following sections.

In the literature, all design methodologies [13,26] have used grid parameters and system level requirements (nominal power of the converter, active power to be provided by the energy storage system, etc.) to design a converter with the maximal and average currents in the arms (and then in switches), and submodule capacitor sizing (capacitance value, maximum voltage ripple and continuous current, etc.) as the main output. Consequently, there has been a degree of freedom considered with respect to the choice of the components of a submodule. This solution is not viable from a manufacturer's point of view since submodules are not specifically designed for a given project. They already have their own range of prebuilt submodules. The second challenge addressed in this paper is to define a methodology to design a MMC-PIES with prebuilt SMs and ES-SMs. The proposed design flow described in the following sections includes defining the minimum number of ES-SMs per arm to achieve requirements for the provision of ancillary services.

The paper is organized as follows: In Section 2, we review the fundamentals of the MMC-PIES and detail the proposed method for the circulating current injection; in Section 3, we present the proposed design methodology, in Section 4, we depict different case studies, which are explored and supported with power capability graphs of the converter and, at the same time, simulation results are presented to validate the presented design methodology; finally, in Section 5, we highlight the advantages of the proposed methods and provide perspectives.

2. MMC-PIES

2.1. Topology

The general structure of a three-phase MMC-PIES is shown in Figure 1. As a classical MMC, each converter leg comprises identical upper and lower arms formed by the series connection of N submodules. Each arm contains the same mixture of N_{sm} standard SMs, without energy storage, and N_{ES-SM} submodules with integrated energy storage (ES-SMs). This means that the SM capacitor is directly interfaced to an energy storage element (ESE) through a DC/DC interface converter (Figure 1). These interface converters can control the power exchange between the submodule capacitor and the ESE and can optimize the sizing of the latter [16]. In this paper, half-bridge and full-bridge ES-SMs are explored, while standard half-bridge SMs are retained. Note that when ESEs are not used, an ES-SM acts as a standard SM.

Since in an HVDC-MMC, the total number of submodules N in an arm is large and the submodule capacitors are kept at a given voltage, each chain of submodules can be modeled as a controllable voltage source. By adjusting these voltage waveforms, arm currents (I_{arm}) can be controlled due to the arm inductor (L_{arm}) series connected in the arm. Note that a small difference between arm voltages generates balancing currents (I_{circ}) which circulate from one phase leg to another and remain internal to the converter. Thus, these currents can be used to transfer energy inside the converter: between phases, between the upper arm and the lower arm, and between EM-SMs and SMs; for this, circulating currents have DC components, AC components at the grid frequency, and AC components at twice the grid frequency, respectively. V_{ZS} refers to a zero-sequence voltage that is commonly used to inject harmonics of rank three or multiples of three in the AC modulated voltage by the converter to reach a higher AC fundamental amplitude [31,32]. Finally, L_{ac} describes the AC inductances.

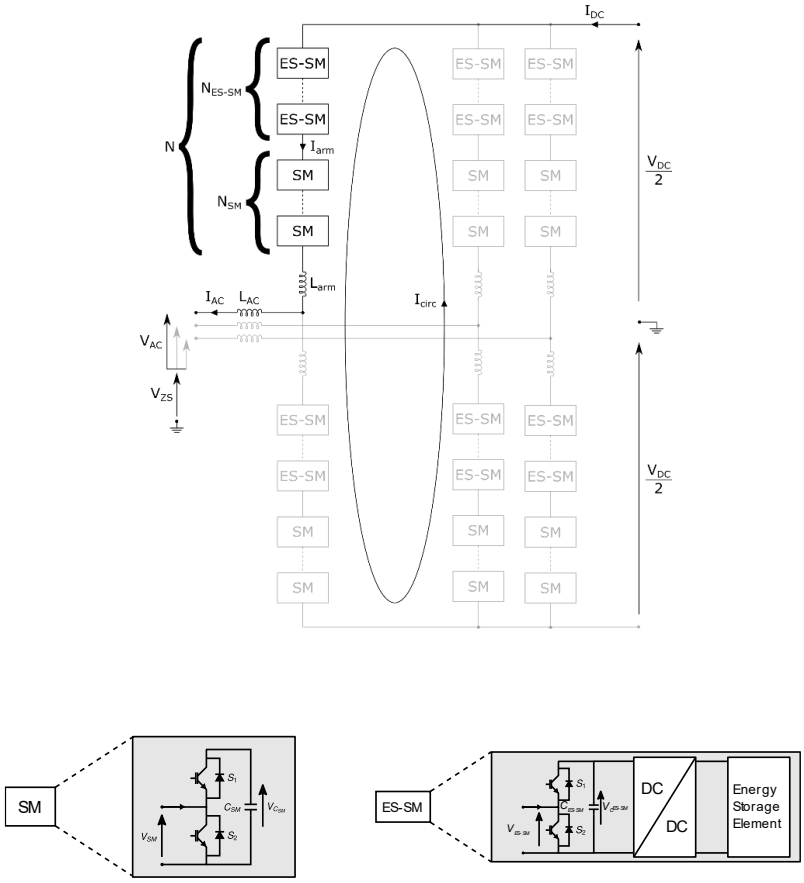

Figure 1. Topology of a modular multilevel converter with partial integration (MMC-PIES) (note that half-bridge energy storage submodule (ES-SM) is depicted here).

Conventionally in an MMC, the AC and DC powers are controlled to be equal (if internal power losses are neglected) since the converter has limited energy storage capability (i.e., the variation of energy stored in SM capacitors is very limited). The power imbalance ΔP (as defined in (1)) is null in normal operation:

$$\Delta P = P_{AC} - P_{DC} \tag{1}$$

By adding a distributed energy storage system, a new degree of freedom in active power exchange between the MMC and the grid is achieved. The energy storage system can cover up the imbalanced ΔP, while the AC and DC power setpoints can be decoupled. However, the correct amount of power must be extracted from the ESEs as well as ensuring a net-zero energy deviation of the submodule capacitors of an arm (to maintain SM capacitor voltages at their reference value). This implies appropriate voltage waveforms generated by SMs and ES-SMs.

2.2. Analytical Analysis

In order to simplify the analysis of an MMC, the so-called average modeling approach is commonly employed [33]. It is assumed that every submodule capacitor in an arm shares the same voltage due to an adequate low-level controller. Thus, each stack of submodules can be replaced by a controllable voltage source. The generated voltage is proportional to the submodule capacitor voltage through a coefficient called the modulation index. Figure 2 presents a schematic for the upper arm of an MMC-PIES.

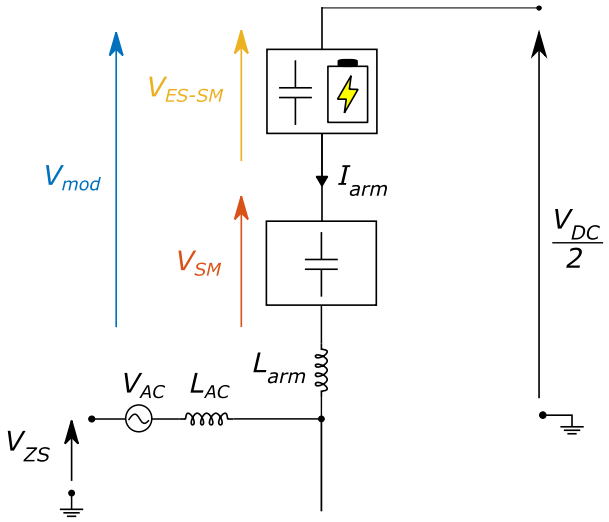

Figure 2. Simplified equivalent average model of an upper arm of an MMC-PIES.

Since an MMC-PIES relies on a mixture of submodules (see Figure 1), two equivalent controllable voltage sources per arm must be defined. On the one hand, V_{SM} corresponds to the inserted voltage by the N_{SM} standard submodules, while, on the other hand, V_{ES-SM} stands for the inserted voltage by the N_{ES-SM} ES-SMs. Similarly, the sum of these two voltages corresponds to the total arm voltage (V_{mod}). Note that, in this study, we focus only on one arm, since all six arms are equivalent, with the same number of SMs and ES-SMs. Furthermore, studies are made in steady state, while ideal waveforms (i.e., switching events are not considered) are considered. Therefore, the arm modulated voltage over time is defined by (2), while the current that flows through it can be calculated as in (3):

$$V_{mod}(t) = \frac{V_{DC}}{2} - \sqrt{2}V_{AC}\sin(\omega t) - V_{ZS}(t) - L_{arm}\frac{dI_{arm}(t)}{dt} - L_{AC}\frac{dI_{AC}(t)}{dt} \tag{2}$$

$$\begin{aligned} I_{arm}(t) &= \frac{I_{DC}}{3} + \frac{I_{AC}(t)}{2} + I_{circ}(t) \\ I_{arm}(t) &= \frac{P_{DC}}{3V_{DC}} + \frac{\sqrt{2}P_{AC}}{6V_{AC}\cos(\varphi)}\sin(\omega t - \varphi) + I_{circ}(t). \end{aligned} \tag{3}$$

Even though the control flexibility of an MMC permits a power imbalance between the AC and DC grids, a net energy deviation in an arm occurs at each end of period T. As a result, the submodule capacitor voltages may drift over time. In an MMC-PIES, this must be compensated for by using the ES-SMs to allow power decoupling and to prevent the deviation. This means that, in an arm, after a period of the grid voltage, the energy deviation of the stack of the standard SMs (ΔE_{SM}) must be equal to zero:

$$\Delta E_{SM} = \int_0^T V_{SM}(t) * I_{arm}(t)dt = 0 \tag{4}$$

while the energy deviation of the ES-SMs (ΔE_{ES-SM}) must equal the net energy deviation of the arm at each end of cycle (ΔE_{arm}):

$$\begin{cases} \Delta E_{ES-SM} = \Delta E_{arm} = \frac{\Delta P}{6} * T \\ \Delta E_{ES-SM} = \int_0^T V_{ES-SM}(t) * I_{arm}(t)dt \\ \Delta E_{arm} = \int_0^T V_{mod}(t) * I_{arm}(t)dt. \end{cases} \tag{5}$$

This directly affects the calculation of the minimum number of ES-SMs (i.e., the required ES-SM voltage rating) per arm and their topology. For example, half-bridge cells can only generate zero or positive voltage ($V_{ES-SM}(t) \geq 0$). This means that the energy exchange between the ESEs and the rest of the system occurs only during time intervals when $I_{arm}(t)$ has the same sign as ΔP. In opposition, full-bridge cells can insert positive

or negative voltages in the arm. Therefore, they can be used to exchange power between the ESEs and the rest of the system during the full period (except when $I_{arm}(t) = 0$). Then, potentially more half-bridge ES-SMs are needed than if full-bridge ES-SMs are considered. For this purpose, a switching variable $s(t)$ is defined to provide the voltage sign of the constant voltage V^*_{ES-SM} to insert as:

$$V_{ES-SM}(t) = V^*_{ES-SM} * s(t) \tag{6}$$

$$s_{Full-Bridge}(t) = \begin{cases} 1 \; if \; sgn(I_{arm}(t)) \neq sgn(\Delta P) \\ -1, \; otherwise \end{cases}$$

$$s_{Half-Bridge}(t) = \begin{cases} 1 \; if \; sgn(I_{arm}(t)) \neq sgn(\Delta P) \\ 0, \; otherwise \end{cases}$$

This principle is summarized in Figure 3 with full-bridge ES-SMs. This example was used for a 1 GW MMC with 401 levels, inspired by the INELFE project [34] used for the case study in Section 4. The AC/DC power was decoupled using 200 MW. Since full-bridge ES-SMs can generate positive or negative voltage (V_{ES-SM}), it should be noted that the power generated by the ES-SMs is independent of the current polarity. Furthermore, it can be easily stated that the condition of having zero energy deviation within the standard SMs at the end of a cycle is effectively fulfilled ($\Delta E_{SM} = 0$). The energy deviation of the arm (ΔE_{arm}) is compensated for by the ES-SM stacks (ΔE_{ES-SM}) as mentioned in Equation (5).

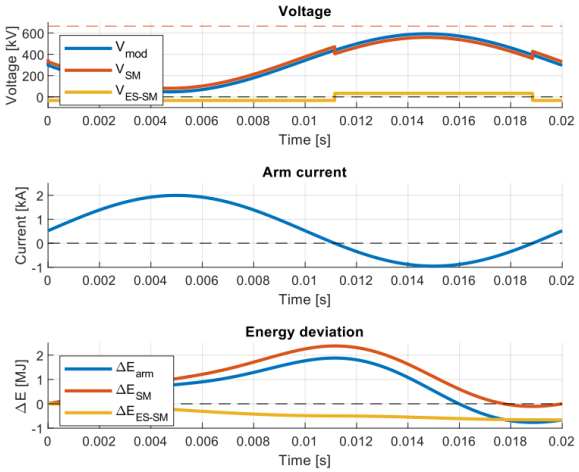

Figure 3. Example of voltage, current, and energy deviation waveforms for SMs and ES-SMs of one arm during one period considering full-bridge ES-SMs.

Nonetheless, determining the minimum number of required ES-SMs is not the only task for sizing an MMC-PIES. Voltage constraints on the standard SM and ES-SM capacitors must be considered, and the abovementioned computation revised. Indeed, the voltage generated by the stack of standard SMs of an arm cannot be negative (half-bridge SMs are considered here) or exceed the maximum voltage available in all the SM capacitors (red dotted line in Figure 4). The voltage waveforms that must be obtained to account for these voltage limits are illustrated in Figure 4 (right). Note that full-bridge ES-SMs are employed since both positive and negative ES-SM voltages can be generated. Note that V^*_{ES-SM} (the maximal value of $V_{ES-SM}(t)$) is higher in Figure 4 (right) than in Figure 4 (left) to compensate for the time intervals where not all the ES-SMs are inserted (when $|V_{ES-SM}(t)| < V^*_{ES-SM}$).

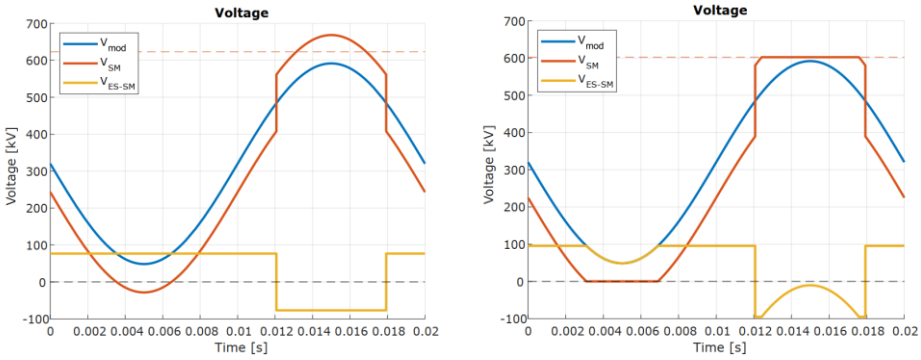

Figure 4. Example of voltage waveforms of an MMC-PIES with full-bridge ES-SMs where $V_{ES-SM}(t)$ is computed by using Equation (6) (**left**) and considering voltage constraints (**right**).

Usually, numerical methods are used because of voltage waveforms, with discontinuities, that cannot be solved analytically [13,26]. Moreover, the voltages at the SM and ES-SM capacitors are not constant over time, but with low oscillating components inherent in the working principle of an MMC. However, in [13], the submodule capacitance must be predefined. This means that the latter can be drastically oversized. Therefore, Ref. [26] proposed an adaptative method which could minimize the values of SM and ES-SM capacitances, while respecting the voltage constraints imposed by the physics of the converter.

Nevertheless, voltage constraints are not the only problems to solve to design an MMC-PIES. It is shown in Equation (5) that the arm energy deviation is only a function of the period T and the power imbalance ΔP. Thus, this is independent of the power level of the converter. This implies that ES-SMs must also achieve this energy deviation at a reduced arm current. However, the amplitude and the DC offset of the arm current is directly linked to the power that flows through the MMC. As a result, V^*_{ES-SM} must be inherently increased during operation at reduced power. If all the operating points of the converter are considered (for example, $\Delta P = P_{AC}$ when $P_{DC} = 0$), this would lead to a converter with only ES-SMs (MMC-FIES for MMC with full integration of energy storage), making the MMS-PIES not feasible.

2.3. Circulating Current Optimization

In order to operate at a low power level, and to avoid a voltage increase in V^*_{ES-SM} (i.e., high number of ES-SMs) to permit sufficient energy exchange, a solution has been proposed in the literature [13]. It involved injecting additional circulating currents (i.e., internal to the converter) into the converter arm waveforms. The goal was to withdraw more power from the ES-SMs without affecting the external AC/DC current waveforms or the energy balance of the converter (just affecting the energy balance between SMs and SM-SMs). To achieve this, therefore, a second or higher harmonics must be used.

In [13], the value of circulating currents was computed in order to reach the maximum peak arm current permitted by the submodule switches. By maximizing its value, the number of ES-SMs was minimized. Nonetheless, adding an important circulating current into the arm current will drastically impact the loses, as well as the energy deviation in the arm. As a result, the required ES-SM and SM capacitors to limit the voltage ripple at the capacitor will be bulkier. This questions the feasibility of the MMC-PIES [26]. Therefore, in this paper, an optimization of the circulating current is used to minimize its value, but still with the objective to keep a reduced number of ES-SMs. The proposed current per phase (with $k \in \{a, b, c\}$) is described in Equation (7):

$$I_{circ_k}(t) = \hat{I_{circ}} \sin(2(\omega t + \phi_k - \varphi + \psi_{circ})) \tag{7}$$

where $\hat{I_{circ}}$ is its peak value, φ is the phase shift between the arm current and the arm voltage, ϕ_k is the phase shift of a three-phase system, and ψ_{circ} is the phase shift between

the circulating current and the arm current. This current is used in a numerical approach to minimize $\hat{I_{circ}}$ as described below.

First, the number of ES-SMs is computed for the operating point with the maximum arm current amplitude and no circulating current injection (i.e., $I_{circ}(t) = 0$). It occurs at $P_{DC} = P_{nom}$, $P_{AC} = P_{nom} + \Delta P_{max}$, and maximum Q_{AC}, where P_{nom} is the nominal power of the converter. For all the other operating points, the voltage V_{ES-SM} is first set as high as possible, and then $\hat{I_{circ}}$ is iteratively computed to reach the number of ES-SMs initially defined (for the maximal arm current). This is done until the energy deviation of the SM capacitor stack is equal to zero. On the basis of this method, the amplitude of the circulating current is reduced and the number of required ES-SMs is optimized, even when the converter is used at reduced active power. Note that, first, optimization studies were also carried out to find the required phase shifts. As a result, the latter was tuned as follows:

$$\psi_{circ} = \begin{cases} \frac{\pi}{4}, \; if \; P_{DC} \geq 0 \\ -\frac{\pi}{4}, \; otherwise \end{cases} \tag{8}$$

It can be noted that, in [13], the circulating current was always computed in a way that the arm current was equal to the maximum peak current allowed by the submodule semiconductor devices. With the method proposed here, such a high arm current is only reached for the worst-case operating point. Otherwise, the arm current has a reduced magnitude. This stage is crucial since it extends the possible area of operation of the converter, and can also optimize its design. In fact, by adjusting the amplitude and the phase shift of the circulating current, the arm current can be adapted to reach the minimum number of ES-SMs needed, and to drastically reduce the voltage ripple at the SM and ES-SM capacitors. Consequently, smaller capacitors are required or, if given capacitors are considered such as in this paper, the range of operating points is extended.

3. Proposed Design Methodology

3.1. Framework of the Study

Design methodologies for an MMC-PIES have been previously presented [13,26] to numerically determine the minimum number of ES-SMs required in an arm. This is done according to specifications, i.e., the operating power and the associated grid voltages:

- The converter nominal power (without the energy storage system);
- The maximum power imbalance to cover by the energy storage system;
- The reactive power requirement;
- The AC/DC grid voltages.

Usually, the following converter specifications are derived as:

- The minimum number of ES-SMs;
- ES-SM and SM capacitances;
- Arm current for semiconductor devices rating;
- Power exchanged by the ESE of an ES-SM;
- Arm inductances (most of the time neglected).

Then, this approach considers that submodules are designed for a specific project, thus, losing an important advantage of modular converters such as convenient construction and scalability. From a manufacturer point of view, a relevant approach involves designing submodules and arranging them to build several project-specific converters. Thus, design methodologies must be adapted to such constraints.

Therefore, a so-called inverse approach is proposed in this paper. The minimum number of required ES-SMs is computed according to the characteristics of prebuilt components. The following input variables are considered as known, in addition to system level parameters:

- SMs an ES-SM capacitances (C_{SM} and C_{ES-SM});

- Maximum voltage ripple at the SM and ES-SM capacitors (the ripples considered here are the ripples on the equivalent capacitors in the average model of an arm, and the actual ripple on a single submodule capacitor is higher and related to the low-level control);
- Semiconductor device ratings;
- Maximum power of an ESE (P_{ESE}).

This approach provides a converter design that allows to satisfy all the operating points for a given nominal power and power imbalance. This means that an operating point is considered to be feasible if the following conditions are respected:

- The peak, average, and rms values of the arm current do not exceed the maximum rating allowed;
- The instantaneous voltage at the equivalent capacitor of a stack of SM or ES-SM cannot exceed the maximum allowed voltage deviation;
- The sum of the individual power of each ESE must be equal (or greater) to the considered power imbalance ΔP.

The abovementioned conditions must be verified for the defined range of reactive power. Therefore, in the next section, we describe the novel design methodology developed in this paper.

3.2. Numerical Method

The proposed method to determine the minimum number of ES-SMs, considering prebuilt components, is depicted in Figure 5. Note that this flowchart is valid for testing only one operating point, and according to a given number of ES-SMs. Therefore, N_{ES-SM} can possibly take any values ranging from 0 to N in an ascending order during the process. This implies that the approach is repeated for many operating conditions in the desired operating range to determine the appropriate configuration. Consequently, if the converter is not able to work correctly for all these points, the number of ES-SMs is increased iteratively. Otherwise, the algorithm is stopped, while the correct number of ES-SMs is kept. Here, the operating range of the MMC-PIES is defined as the sum of ΔP and P_{nom} in terms of active power, and a reactive power requirement proportional to P_{nom}.

First, the considered operating point, the number of ES-SMs and SMs, as well as their characteristics are defined. After that, the initial values of the inserted voltages V_{SM} and V_{ES-SM} are first computed considering the voltage constraints. As detailed in Section 2, Equations (5) and (6) must be complemented by a numerical approach [26]. One of the objectives is to ensure that the sum voltage inserted by the standard SMs V_{SM} does not exceed the maximum voltage that can be generated by the SM capacitors V_{SM}^{max} and respect physical limits:

$$0 \leq V_{SM} \leq V_{SM}^{max} \tag{9}$$

Then, an estimate of the SM stack voltage $\widetilde{V_{SM}}(t)$ is computed by Equation (10) and used to define the correct value of the ES-SM and SM stack voltages using Equations (11) and (12), respectively.

$$\widetilde{V_{SM}}(t) = V_{mod}(t) - V_{ES-SM}^{*} * s(t) \tag{10}$$

$$V_{ES-SM}(t) = \begin{cases} V_{mod}(t), \; if \; \widetilde{V_{SM}}(t) < 0 \\ V_{mod}(t) - V_{SM}^{max}, \; if \; \widetilde{V_{SM}}(t) > V_{SM}^{max} \\ V_{ES-SM}^{*} * s(t), \; otherwise \end{cases} \tag{11}$$

$$V_{SM}(t) = V_{mod}(t) - V_{ES-SM}(t) \tag{12}$$

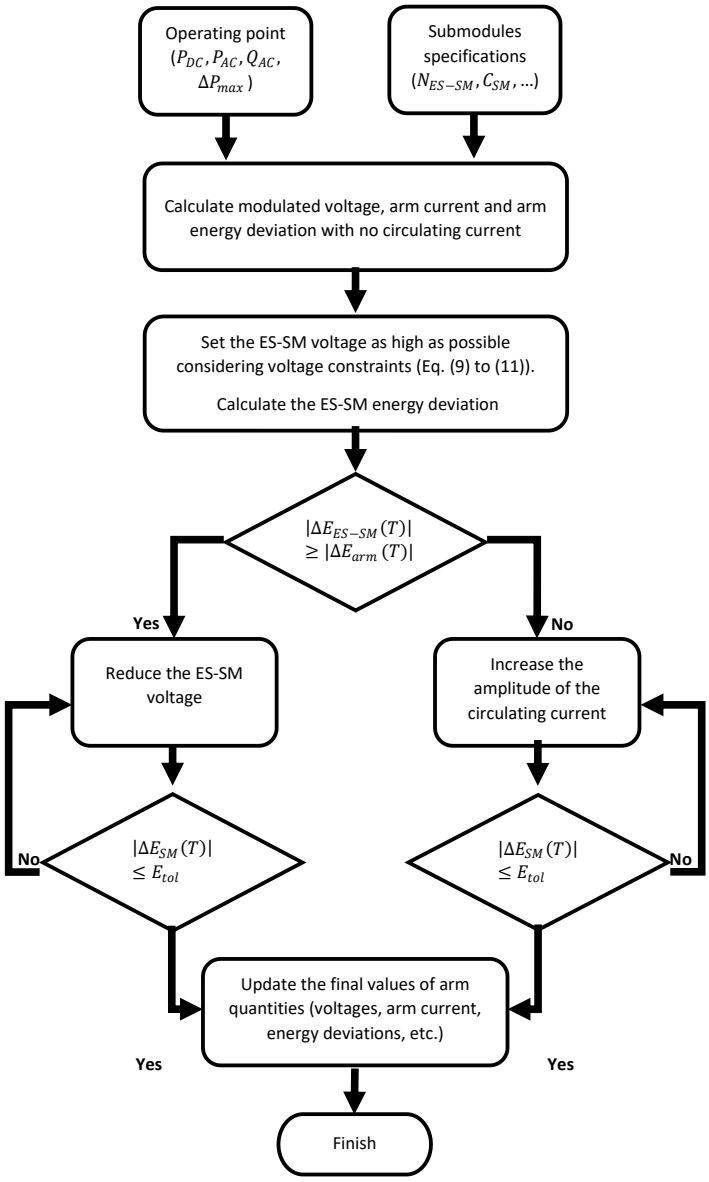

Figure 5. Flowchart of the sizing methodology of an MMC-PIES based on prebuilt components.

However, a small change on the ES-SM stack voltage will inevitably affect the energy deviation within the converter arm. It must be verified that ΔE_{ES-SM}, the energy deviation of the ES-SMs, is equal to the energy deviation in the arm ΔE_{arm} at the end of each cycle. If not, the voltage $V_{ES-SM}(t)$ must be updated or circulating current injected.

This choice depends on the energy deviation of the energy storage portion of the arm (ΔE_{ES-SM}). If it exceeds ΔE_{arm} (the arm energy deviation after one period), the voltage V_{ES-SM} is decreased iteratively to adapt the energy deviation of the stack of the ES-SMs. Otherwise, circulating current is injected, as discussed in Section 2.3.

Note that during both iterative processes, the method involves computing first the ES-SMs, SMs, and arm voltages. Afterwards, the energy deviations within the arm are determined, as well as the voltage fluctuations at the SM and ES-SM capacitors ($V_{c_{SM}}$ and $V_{c_{ES-SM}}$). The latter is based on the total energy stored in both stacks as follows (note that the subscript "stack" can be replaced by the terms "SM" or "ES-SM") [35]:

$$V_{c_{stack}}(t) = \sqrt{\frac{2}{C_{cell} N_{stack}} (\Delta E_{stack}(t) + E_{stack}(0))} \tag{13}$$

$$E_{stack}(0) = \frac{-\Delta\check{E}_{stack}\left(1+\Delta V_{p.u}\right)^2 + \Delta\check{E}_{stack}\left(1+\Delta V_{p.u}\right)^2}{4\Delta V_{p.u.}} \quad (14)$$

where $\Delta\check{E}_{stack}$, $\Delta\check{E}_{stack}$ are the peak and negative energy deviation of a stack of capacitors, whose value of the submodule capacitance is C_{cell} and $E_{stack}(0)$ the nominal stored energy. $\Delta V_{p.u.}$ represents the maximum voltage deviation allowed at the terminals of a stack.

Once all the waveforms are obtained, the design criteria and constraints are compared. Finally, to confirm that the design is correct and to have a sensible stop criterion, a tolerance variable is introduced to determine if the SM energy deviation is zero such as $|\Delta E_{SM}(t)| \leq E_{tol}$. In this way, it ensures that there is also no drift of the SM capacitor voltages.

4. Results Obtained with the Design Methodology Based on Prebuilt Components

This section is dedicated to an application case, of the abovementioned methodology, to illustrate the results that can be obtained. Most of the parameters of the MMC come from [34] and are provided in Table 1. Note that the injection of circulating current and third harmonic voltage are also considered, as previously in Section 2.

Table 1. Main parameters of the considered MMC-PIES.

Parameters	Values
Converter nominal active power, P_{nom}	1 GW
Maximum power imbalance, ΔP_{max}	0.1 GW
Converter reactive power requirements, Q	+/−0.3 GVAR
AC phase-to-neutral voltage	222 kV
Arm inductance, L_{arm}	50 mH
AC inductance, L_{AC}	50 mH
DC bus voltage, V_{DC}	640 kV
Total number of submodules in an arm, N	200
Submodule nominal voltage	3.5 kV
Voltage ripple of equivalent submo$L$dule capacitors	+/−10%

In this example, only the values of the SM and ES-SM capacitances (respectively, denoted C_{sm} and C_{ES-SM}) are varied, while applying the following constraints on the arm currents (these values are related to limitations of semiconductor devices):

- Maximum peak current, 1.8 kA;
- Maximum RMS current, 1.1 kA;
- Maximum average current, 0.6 kA.

4.1. Feasibility Plot

The derivation of the novel methodology described in Section 3 allows the P/Q capability of an MMC-PIES to be analyzed. In particular, it can be used to define the minimum number of ES-SMs to be used in the converter with prebuilt SMs and ES-SMs. Before starting, in this subsection, we present the feasibility plot of an MMC-PIES based on prebuilt components for a given set of requirements $\{P_{DC}\ (\sim P_{nom}); \Delta P_{max}; N_{ES-SM}\}$ that can be delivered. As mentioned in Section 3, this graph is obtained by checking if an operating point is feasible after executing the algorithm described in Figure 5.

Figure 6 illustrates the feasibility plot of the proposed converter in Table 1 considering 55 half-bridge ES-SMs per arm. The x-axis stands for the DC power of the converter (P_{dc}), while the y-axis represents the active power injected by the energy storage system (ΔP as compared with Equation (1)). In this case study, the SM and the ES-SM capacitance values are considered to be equal with a value of 4 mF and the ESEs of an ES-SM can provide 0.5 MW. Note that the causes of the operating points that are not feasible are highlighted. Obviously, an operating point may be unfeasible due to several causes. Therefore, a priority order has be defined to avoid combination of colors and to gain more clarity. According

to the legend for Figure 6, the highest priority is placed on the right (i.e., "maximum current") meaning, for instance, that an operating point in a blue area can be unacceptable because the ESE power is too low or because both the ESE power and the voltage ripple do not comply with requirements. Finally, the focus is on the active power, but all the feasible points (i.e., in green) respect the required reactive power requirements mentioned in Table 1.

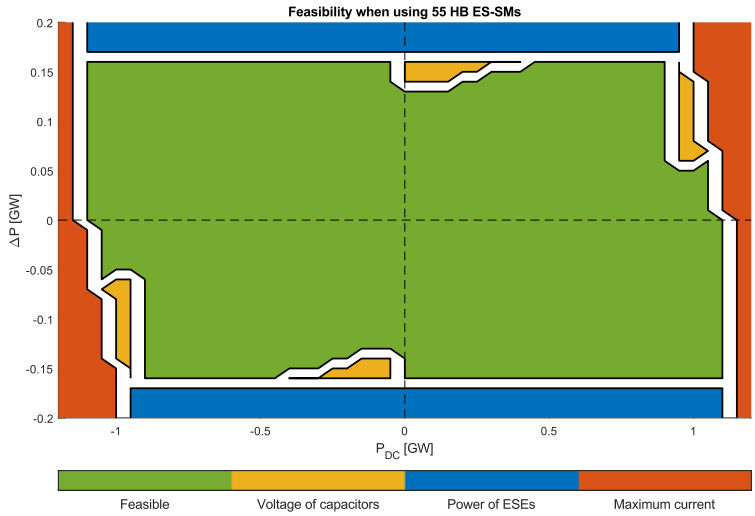

Figure 6. Example of an MMC-PIES with 55 half-bridge submodules per arm with ES-SM and SM capacitance values of 4 mF considering the converter with parameters as listed in Table 1. The ES-SM power capability is 0.5 MW. Operating points in green are feasible. For operating points in yellow, the voltage ripple in equivalent arm capacitors exceeds the limit. Operating points for which the ESEs are not able to provide the required power are plotted in blue. If the arm current exceeds the limit, the corresponding operating points are depicted in red.

It can be observed that the average arm capacitor voltage ripple exceeds the limits (yellow area) for a maximum power imbalance ΔP_{max} of 0.1 GW at nominal power in inverter mode ($P_{DC} = 1$ GW). This means that, at this operating point, the submodule voltage ripple is greater than the 10% of the submodule nominal voltage required in Table 1. However, the converter is required to provide a ΔP_{max} of 0.1 GW irrespectively of the AC/DC converter setpoint. This implies that the tested configuration is not acceptable. The converter cannot operate properly at all the expected operating points.

In the same way, when the converter works in rectifier mode at nominal power ($P_{DC} = -1$ GW) and maximum power imbalance ΔP_{max} of -0.1 GW, the converter is restricted by the capacitor voltage ripple and by the maximum current allowed by the switches (red area).

Conversely, it should be mentioned that the converter can also operate for a power imbalance higher than ΔP_{max} at some operating points (i.e., $P_{DC} = 0.7$ GW and $\Delta P_{max} = 0.15$ GW). This is because the sum of the power of the ESEs is greater than the desired value of ΔP_{max} here (i.e., 165 MW since there is 55 ES-SMs per arm).

Consequently, since prebuilt submodules are considered, the solution involves adapting the number of ES-SMs or the circulating current injection, based on the numerical method developed in Section 3, to have a green area for all the points comprised $P_{dc} \in [-1; 1]$ and $\Delta P \in [-0.1; 0.1]$.

4.2. Case Study

In this example, the specifications are identical to the ones introduced at the beginning of Section 4. As mentioned, only the ES-SM and SM capacitance values as well as the power of an ESE are varied with the aim of representing different types of submodules. The expected output is the minimum number of ES-SMs required in each arm to achieve

the specifications (as shown in Table 1). The considered examples are defined in Table 2. This table also gathers all the results.

Table 2. The minimum number of ES-SMs obtained with the proposed methodology according to different prebuilt components (HB, half-bridge and FB, full bridge).

	Example 1		Example 2		Example 3	
Type of ES-SMs	**HB**	**FB**	**HB**	**FB**	**HB**	**FB**
Specifications						
SM capacitance, C_{SM} (mF)	3	3	4	4	6	6
ES-SM capacitance, C_{ES-SM} (mF)	3	3	4	4	4	4
Power of an ESE (MW)	3	3	1	1	0.5	0.5
Results						
Minimum number of ES-SMs, N_{ES-SM}	/	/	31	73	34	34

One can easily notice in Example 1 that SM and ES-SM capacitance values that are too low would not lead to a possible solution with mixed arms. This emphasizes the importance of the sizing of the submodule capacitance in the design of an MMC-PIES.

In Example 2, this value was increased, while the power of an ESE was decreased. The results showed that the required number of full-bridge ES-SMs was more than twice the number of half-bridge ES-SMs. This confirms that an MMC-PIES with full-bridge ES-SMs is not necessarily the best approach. Indeed, it has been shown in [26] that full-bridge cells can reduce the minimum number of ES-SMs, but with significantly higher values of submodule capacitors and of the total stored energy. It is shown here that with similar (low) values of submodules capacitances, the number of required ES-SMs is higher with full-bridge cells than with half-bridge cells. As ES-SMs with half-bridge cells usually require a lower capacitance than ES-SMs with full-bridge cells, the increased number of full-bridge ES-SMs is explained by the need to compensate for this low value.

Finally, in Example 3, the values of SM and ES-SM capacitances are disparate, while the power of ESEs is still lowered. The standard SM capacitance was raised to 6 mF. Since the voltage ripple is acceptable with these configurations, each configuration necessitates the same number of ES-SMs.

4.3. Validation

To verify the analysis made within the above sections, simulations were carried out in MATLAB/Simulink. Then, the results were directly compared to what was obtained with the analytical method. Therefore, arm average modeling of an MMC-PIES was developed to model the six arms of the converter, as depicted in Figure 7.

This model assumes that the capacitance values of all the ES-SMs (similarly for the standard SMs) are identical and kept at the same voltage. Then, the stacks of SMs and ES-SMs can both be represented by an ideal equivalent converter and an equivalent capacitor, respectively, designated $C_{\sum SM}$ and $C_{\sum ES-SM}$. Note that, now, the voltage generated by the ES-SMs and SM stacks (V_{ES-SM} and V_{SM}) is proportional to the available voltages at both equivalent capacitors ($V_{C_{\sum SM}}$ and $V_{C_{\sum ES-SM}}$) according to modulation indexes, respectively, named m_{SM} and m_{ES-SM}. They correspond to the ratio between the number of submodules inserted in the arm over the number of submodules in the stack. Finally, a current source in an ES-SM represents the current extracted from the interface converter that connects the ESE to the ES-SM capacitor. On the basis of the ES-SM and SM stack voltages and the equivalent ES-SM and SM capacitor voltages, the modulation indexes are computed and used in the simulation model. The remaining variables of the current and voltage sources are determined by using the simulator. Note that no control algorithm is included. The test is done in open loop and in steady state for the given operating points.

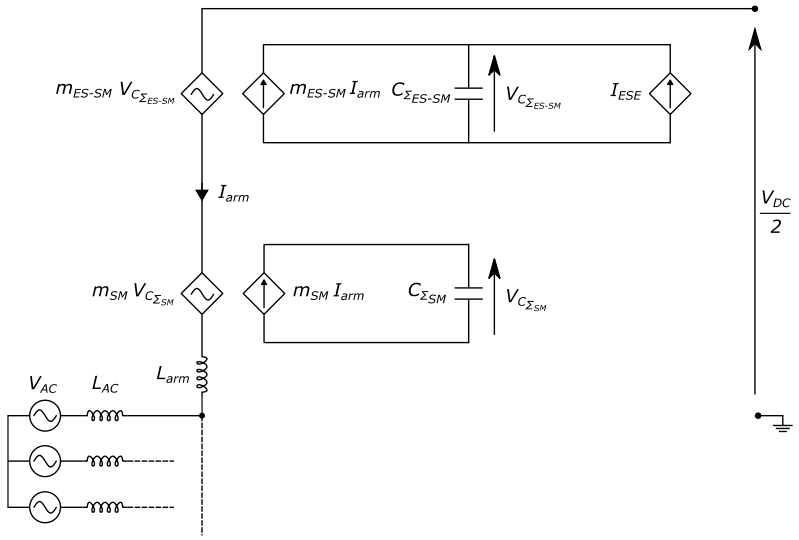

Figure 7. An average model of one upper arm of an MMC-PIES.

Waveforms during one cycle are presented in Figure 8 for an MMC-PIES with half-bridge ES-SMs. The parameters of the case study of Table 1 are kept. Here, the ES-SM and SM capacitances have, respectively, values of 4 and 6 mF, while the power of an ESE is 0.5 MW, as mentioned in Example 3 of Table 2. According to the abovementioned algorithm, the minimum number of ES-SMs considered is 34. The results in Figure 8 correspond to a converter operating at low power level, such as $P_{DC} = 0.2$ GW, $P_{AC} = 0.3$ GW, and $Q_{AC} = -0.3$ GVAR, which is one of the most constraining operating points.

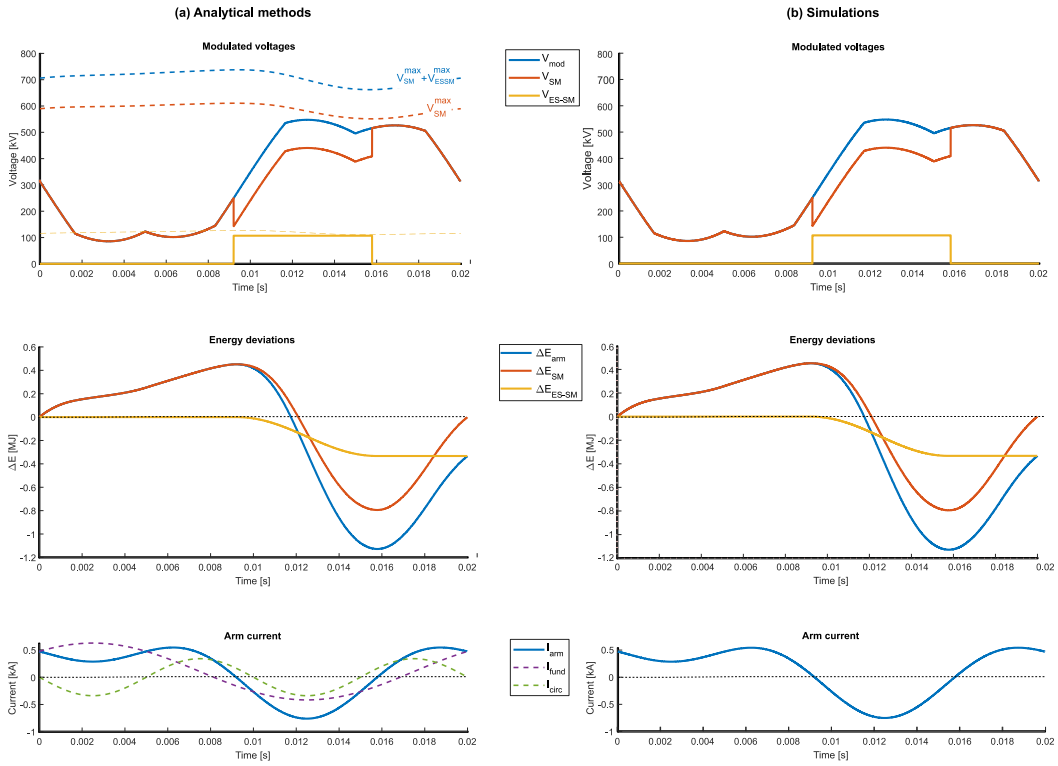

Figure 8. Waveforms of an upper arm of an MMC-PIES, with 34 half-bridge ES-SMs, with $C_{\sum SM}$ and $C_{\sum ES-SM}$ equal to 6 and 4 mF, respectively, at $P_{DC} = 0.2$ GW, $P_{AC} = 0.3$ GW, and $Q_{AC} = -0.3$ GVAR.

It can be observed that the analytical and simulation waveforms are strictly identical. This validates the equations of the proposed analytical method.

It can be noted that the energy deviation of the SM stack (ΔE_{SM}) is equal to zero at the end of each cycle, while the energy deviation in the ES-SM stack (ΔE_{ES-SM}) equals the energy deviation in the arm (ΔE_{arm}). Moreover, it can be shown that the energy deviation corresponds to the power imbalance ΔP divided by the number of arms during a period, as mentioned in Equation (5).

Regarding the modulated arm voltages (V_{mod} and V_{SM}), it can be easily stated that voltage constraints were properly taken into considerations (i.e., particularly the maximum voltage available from the standard submodule capacitors V_{SM}^{max} shown as a red dotted line and the maximum voltage available from all the submodule capacitors $V_{SM}^{max} + V_{ES-SM}^{max}$ shown as a blue dotted line) as shown with the analytical model (cf. Figure 8a). Therefore, the feasible limits of the converter are not exceeded. Furthermore, the shape of the modulated arm voltage indicates the presence of a third harmonic injection, as mentioned in Section 2, and a second harmonic (due to the fact that circulating currents create voltages across arm inductors).

Similarly, the influence of the circulating currents can be easily stated, since arm current includes a DC and an AC component at the line frequency. Figure 8a shows that a circulating current at twice the line frequency is injected to optimize the use of the ES-SMs. At the same time, it can be observed that the arm peak current is lower than the maximum semiconductor limits indicated at the beginning of Section 4, just as the average and rms currents.

Finally, Figure 9 highlights the same results, but with full-bridge ES-SMs, and using the proposed analytical method. The goal is to illustrate the difference between half-bridge and full-bridge ES-SMs. It can be easily noted that, in this case, the voltage generated by the ES-SMs can be positive or negative. Moreover, it can be shown, for this operating point, that fewer ES-SMs must be inserted but over a longer time period. To conclude, no circulating current is injected in this case. This operation without circulating current is feasible because the voltage inserted by the ES-SMs is lower than the equivalent capacitor voltage of ES-SMs (for this operating point, the modulation index of ES-SMs is always lower than one).

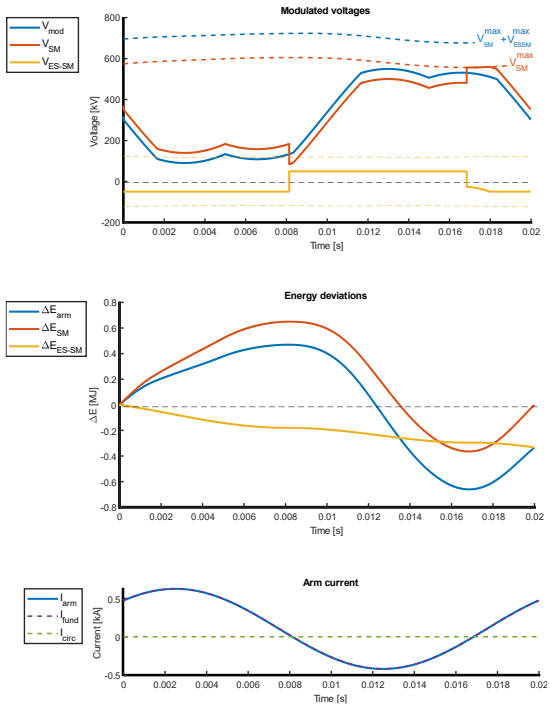

Figure 9. Waveforms of an upper arm of an MMC-PIES, with 34 full-bridge ES-SMs, with $C_{\sum SM}$ and $C_{\sum ES-SM}$ equal to 6 and 4 mF, respectively, at $P_{DC} = 0.2$ GW, $P_{AC} = 0.3$ GW, and $Q_{AC} = -0.3$ GVAR.

5. Conclusions

- In this paper, a novel method for designing an MMC-PIES is presented that complies with given specifications. It illustrates its feasibility even if a restricted number of components is available, i.e., prebuilt SMs and ES-SMs are considered, and their structures are imposed.
- First, the working principle of the converter is detailed in the Introduction, as well as its main challenges such as operating at reduced power level or the voltage deviation at the average arm capacitor. Therefore, a set of equations to apply realistic voltage constraints and a method based on circulating currents is proposed to operate at low power in the AC system. This improved method also optimizes the design of the converter by adapting the amplitude of circulating currents and their phase shifts.
- Once the framework of the study is presented, the design methodology based on prebuilt components is introduced. Afterward, each step of the process is developed to determine the minimum number of ES-SMs to satisfy an expected range of operation. Based on this methodology, the feasibility graph of the converter is drawn, to visualize the feasible operating range of the MMC-PIES and to determine if a converter can operate properly without exceeding its physical limits. It also shows the exceeded limit giving indications to the designer to find a solution.
- Finally, a case study is presented to show the potential of the proposed method. It is confirmed that half-bridge ES-SMs are a much more promising solution than full-bridge ES-SMs by requiring fewer switches and less energy stored within the converter.

6. Perspectives

In this paper, the magnitude of circulating currents is optimized. However, further phase shift investigations should be conducted to improve the proposed method. Similarly, the combination of circulating currents at different frequencies is a potential perspective. Since the circulating currents have a non-negligible impact on the energy deviation, this may increase the attractiveness of the proposed converter. Furthermore, it can be shown that fewer ES-SMs can lead to high ESE power capacity. The technical feasibility of the interface converter that would connect the ESEs to the submodule capacitors must be carried out. Finally, having two types of submodules in an arm with different characteristics is not straightforward, from a control point of view, for ensuring the appropriate power deviation, while respecting the intrinsic constraints of the converter. Therefore, an appropriate balancing algorithm and control scheme must be investigated.

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