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Series-Connected High Frequency Converters in a DC Microgrid System for DC Light Rail Transit

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Abstract: This paper studies and presents a series-connected high frequency DC/DC converter connected to a DC microgrid system to provide auxiliary power for lighting, control and communication in a DC light rail vehicle. Three converters with low voltage and current stresses of power devices are series-connected with single transformers to convert a high voltage input to a low voltage output for a DC light rail vehicle. Thus, Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) with a low voltage rating and a turn-on resistance are adopted in the proposed circuit topology in order to decrease power losses on power switches and copper losses on transformer windings. A duty cycle control with an asymmetric pulse-width modulation is adopted to control the output voltage at the desired voltage level. It is also adopted to reduce switching losses on MOSFETs due to the resonant behavior from a leakage inductor of an isolated transformer and output capacitor of MOSFETs at the turn-on instant. The feasibility and effectiveness of the proposed circuit have been verified by a laboratory prototype with a 760 V input and a 24 V/60 A output.

Keywords: DC microgrid; zero-voltage switching; half-bridge converter; light rail transit

1. Introduction

Direct current (DC) microgrids are studied to combine alternative current (AC) utility power, renewable energy sources, energy storage units and local DC and AC loads in order to reduce global warming and climbing temperature issues. The common DC voltage on DC microgrids can be 1500 V for traction vehicles; 760 V for light rail vehicles and industry applications; 380 V for residential and commercial buildings. For light rail transits, low frequency power transformers are used in conventional light rail vehicles to provide electrical isolation. The main drawback of line frequency transformers [1–3] is bulk volume. To avoid using bulky line frequency transformers, transformerless converter topologies [4–8] with primary-series and secondary-parallel connections have been proposed to lessen the blocking-voltage capability of active devices on the high voltage side and the current stress of power components on the low voltage side. Half-bridge (HB) or full-bridge (FB) converters have been widely adopted for medium power applications to provide a stable and low voltage output. Conventional FB converters and HB converters using high voltage rating devices such as insulated gate bipolar transistors (IGBTs) are widely adopted to convert a high voltage input to a low voltage output. However, the switching frequency of general IGBT devices is less than 50 kHz. To improve the low switching frequency problem of IGBT devices, multilevel converters [9–11] using Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) devices have been developed in medium power converters to reduce converter volume. However, the high switching frequency will also increase core losses on magnetic components and switching losses on power MOSFETs. Zero-voltage switching converters [12–15] have been proposed to achieve a low switching loss. Asymmetric pulse-width modulation [16–18], frequency modulation [19–21] and a phase-shift pulse-width modulation (PWM) scheme [22–24] are general PWM control schemes used in DC/DC converters to regulate load voltage

and also realize the mechanism of the zero-voltage turn-on switching. Therefore, the high efficiency converters can be obtained. The asymmetrical PWM scheme can reset the magnetizing flux in every switching cycle. Therefore, the voltage spike on drain-to-source of power MOSFET can decrease the safety operation region and the electromagnetic interference can be reduced.

This paper presents a series-connected soft switching converter using a single transformer for light rail vehicle applications. The adopted circuit topology includes three series-connected HB circuits on the primary side to reduce the blocking-voltage stress of power MOSFETs. Thus, low turn-on resistance and low voltage rating MOSFETs can be adopted to lessen conduction losses on power devices. The input split voltage balance is achieved by two flying capacitors. The asymmetric PWM scheme is employed to control power switches. The output capacitor of power MOSFETs and the leakage inductor of the transformer are resonant at the transition interval. Thus, the mechanism of the zero-voltage turn-on switching is realized and the electromagnetic interference can be reduced. Current doubler rectifier topology is used on the low voltage side to achieve a ripple current cancellation. Therefore, the resultant ripple current at the output capacitor is reduced. Three HB circuits share one transformer on the primary side so that the primary currents of the three HB circuits are reduced to one-third of the primary current in a conventional HB converter. Therefore, the conduction losses on active switches are reduced and the circuit efficiency is improved. The feasibility of the proposed circuit is verified with a 1.44 kW converter. This paper is organized as follows: in Section 2, the circuit configuration and operation principle of the developed converter used in the DC microgrid are presented and discussed in detail. In Section 3, the circuit characteristics of the developed circuit are presented. Experimental results based on a laboratory prototype are shown and discussed in Section 4. Finally, Section 5 presents the conclusions.

2. Proposed Converter

The basic circuit structure of a DC microgrid is given in Figure 1. The bidirectional AC/DC converters are used between the AC utility system and the DC microgrid to stabilize the DC bus voltage. Renewable energy sources from solar cell panels and wind power generators provide clear energy to the DC microgrid system through the unidirectional DC/DC converters and the AC/DC converters. Energy storage units are used to store/release energy from/to the DC microgrid through the bidirectional DC/DC converters in order to stabilize the DC bus voltage. In order to increase the voltage reliability, the bipolar voltage system ($+V_{dc}$, $-V_{dc}$ and neutral line) can be adopted on the DC microgrid. When a fault condition in one of the DC poles occurs, the DC power is still suppled to the local load by the other two wires and an auxiliary converter. It is clear that the reliability of the DC mircogrid system is increased during fault condition. Therefore, three voltage levels ($2V_{dc}$, $+V_{dc}$ and $-V_{dc}$) can be used to provide industry and transportation with the $2V_{dc}$ voltage level and future residential and commercial buildings with the $+V_{dc}$ or $-V_{dc}$ voltage level. To keep two voltage levels ($+V_{dc}$ and $-V_{dc}$) balanced during unbalanced loads, a voltage balancing circuit is normally needed to realize this goal. The DC/DC converter can be used to convert a high input voltage to a low output voltage and it does not relate to the bipolar voltage system. For a DC light rail vehicle, the input voltage is normally around 760 V. Power devices such as the 1500 V IGBT can be adopted in two-level power converters to supply auxiliary low voltage power for control units, telecommunication units and lighting systems in the light rail vehicle. The MOSFETs with a 600 V rating can be adopted in the three-level power converter to achieve the same goal but with a much higher switching frequency to reduce converter size. The studied converter is concentrated on power conversion for light rail vehicle applications. Figure 2a shows the basic block diagrams of power distribution in a conventional light rail vehicle. First, 750 V_{dc} is converted to the three-phase AC voltage 380 V_{ac} by the DC/AC inverter. Second, the AC/DC converter is adopted to convert 380 V_{ac} to a low DC voltage in an auxiliary power distribution system to supply a necessary amount of DC voltage for the battery bank, lighting equipment, door equipment, control power units and communication equipment in a light rail vehicle system. The AC/DC/AC converter is also adopted to convert 380 V_{ac} to a variable

AC voltage output for the AC motor drive. If the power of the DC light rail vehicle is supplied directly from the DC microgrid, then some power conversion stages can be saved to reduce costs and increase circuit efficiency. The basic power distribution diagrams in the proposed light rail vehicle are illustrated in Figure 2b. The auxiliary power in a light rail vehicle is directly converted from 760 V through a DC/DC converter. The AC motor drive and the air compressor are controlled by the DC/AC converters. Therefore, the AC/DC conversion can be saved to reduce costs and increase circuit efficiency and reliability.

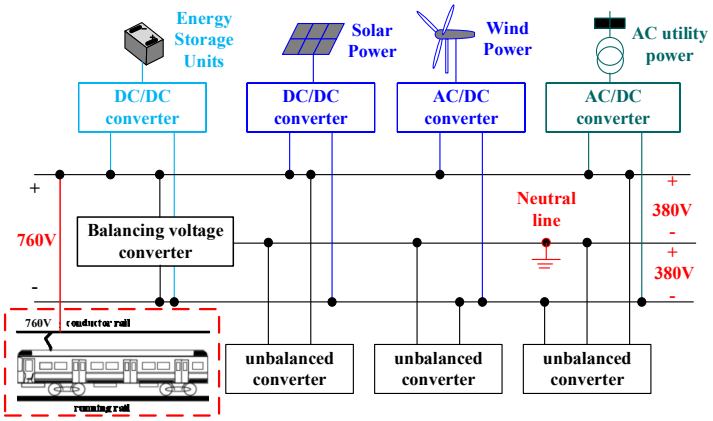

Figure 1. Basic circuit structure of a DC microgrid.

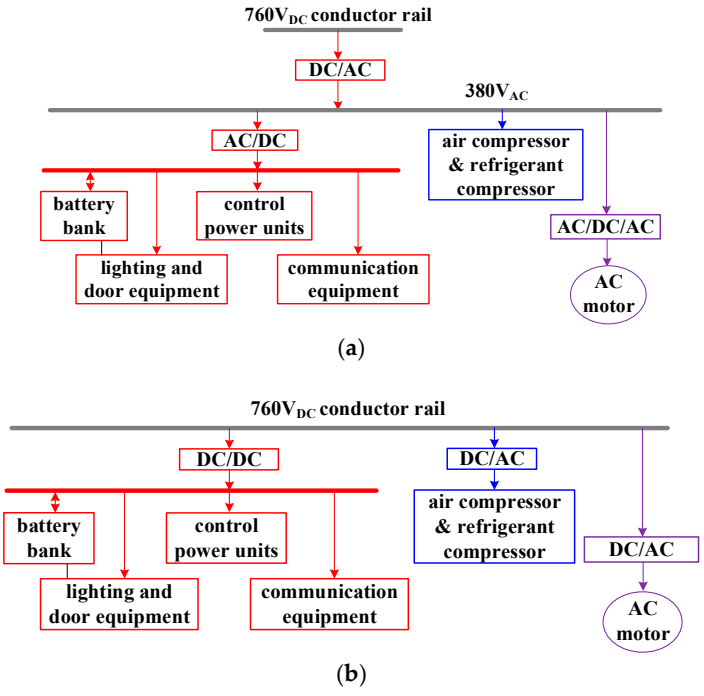

Figure 2. Light rail transit. (**a**) Block diagram of the power distribution in a conventional light rail vehicle; (**b**) block diagram of the power distribution in the studied light rail vehicle.

The studied DC/DC converter is given in Figure 3. It directly converts a 760 V voltage input from the DC microgrid to a low voltage output by using low voltage rating power MOSFETs to provide auxiliary power in a light rail vehicle. The studied converter includes three HB circuits connected in a primary-series secondary-parallel with a single transformer. The primary sides of the HB circuits are connected in a series so that the voltage stress of the power switches Q_1~Q_6 is reduced to $V_{in}/3$ and

the low turn-on resistance of power MOSFETs is adopted to reduce conduction losses and increase circuit efficiency. Each HB circuit provides $P_o/3$ to the output load. Flying capacitors are widely used in a multilevel inverter to reduce voltage stress and balance input split voltages. Thus, two flying capacitors C_{f1} and C_{f2} are used on the high voltage side to achieve an input voltage balance of V_{C1}~V_{C3}. The current doubler rectifier is used on the low voltage side to reduce the output ripple current. The driving signals of each HB circuit use asymmetric pulse-width modulation. Due to the resonant behavior between the output capacitor of the power MOSFETs and the primary leakage inductor at switch on/off instant, the power MOSFETs can be turned on at zero-voltage switching to reduce the switching loss. Figure 4 shows the timing sequence of switches Q_1~Q_6 and the main PWM waveforms in the proposed converter. The operation principle and circuit analysis of the studied circuit are assumed under the following conditions: (1) the output capacitor C_o is large enough to be treated as a constant voltage V_o, (2) power devices Q_1~Q_6, D_1 and D_2 are ideal, (3) $C_{f1} = C_{f2} = C_f$, $C_{b1} = C_{b2} = C_{b3} = C_b$, $L_{r1} = L_{r2} = L_{r3} = L_r$, and $L_{m1} = L_{m2} = L_{m3} = L_m$, (4) $n_1 = n_2 = n_3 = n_p/n_s$, and (5) $V_{Cb1} = V_{Cb2} = V_{Cb3} = V_{Cb}$ and $V_{C1} = V_{C2} = V_{C3} = V_{Cf1} = V_{Cf2} = V_{in}/3$. The duty cycles of Q_1, Q_3 and Q_5 are d. Conversely, the duty cycles of Q_2, Q_4 and Q_6 are $1 - d$. The equivalent circuits of the operating steps in the proposed circuit are shown in Figure 5. There are eight operating stages for every switching period.

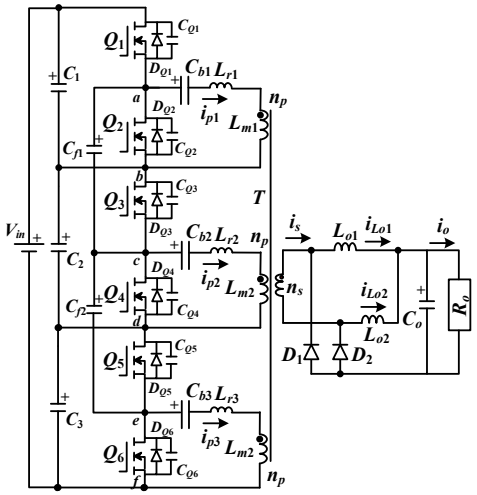

Figure 3. Circuit schematic of the studied converter.

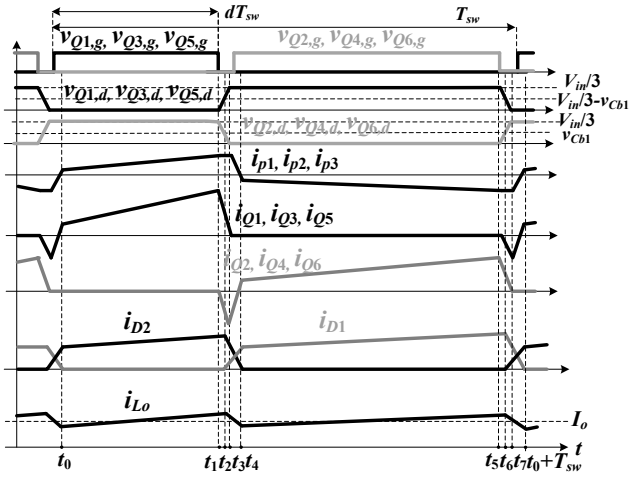

Figure 4. Main waveforms during one switching period.

Step 1 [t_0~t_1]: Before step 1, power switches Q_1, Q_3 and Q_5 are conducting and the output current freewheels through D_1 and D_2. After time t_0, i_{D1} is decreased to zero and D_1 becomes reverse biased. i_o flows through D_2. Power is transferred from V_{in} to R_o in this step. In step 1, $V_{Cf1} = V_{C1}$, $V_{Cf2} = V_{C2}$, $v_{Q2,ds} = V_{C1}$, $v_{Q4,ds} = V_{C2}$, $v_{Q6,ds} = V_{C3}$, $v_{Lm1} \approx V_{C1} - v_{Cb1}$, $v_{Lm2} \approx V_{C2} - v_{Cb2}$, $v_{Lm3} \approx V_{C3} - v_{Cb3}$, $v_{Lo1} \approx [V_{C1} - v_{Cb1}]/n_1 - V_o$ and $v_{Lo2} = -V_o$. Thus, i_{p1}~i_{p3} and i_{Lo1} increase and i_{Lo2} decreases. Since all circuit components in three HB circuits are identical and $n_1 = n_2 = n_3 = n_p/n_s$, it can obtain $v_{Lm1} = v_{Lm2} = v_{Lm3} = nv_{ns}$ and $i_{p1} = i_{p2} = i_{p3} \approx i_s/(3n_1)$. Since i_{Lo1} increases and i_{Lo2} decreases in this step, the ripple current of $i_{Lo1} + i_{Lo2}$ is reduced.

Step 2 [t_1~t_2]: When Q_1, Q_3 and Q_5 are turned off at time t_1; the positive primary currents i_{p1}~i_{p3} rapidly discharge C_{Q2}, C_{Q4} and C_{Q6}, respectively. On the other hand, C_{Q1}, C_{Q3} and C_{Q5} are charged by i_{p1}~i_{p3} respectively. The secondary winding voltage v_{ns} is decreased in this step.

Step 3 [t_2~t_3]: When C_{Q2}, C_{Q4} and C_{Q6} are discharged to v_{Cb1}, v_{Cb2} and v_{Cb3} respectively, then the secondary winding voltage $v_{ns} = 0$. Then the output current i_o freewheels through D_1 and D_2. In this operation step, $v_{Lo1} = v_{Lo2} = -V_o$ and i_{Lo1} and i_{Lo2} decrease.

Step 4 [t_3~t_4]: At time t_3, C_{Q2}, C_{Q4} and C_{Q6} are discharged to zero voltage. Since $i_{p1}(t_3)$~$i_{p3}(t_3)$ are all positive, the body diodes D_{Q2}, D_{Q4} and D_{Q6} are forward biased. Therefore, Q_2, Q_4 and Q_6 can be turned on at this moment to realize a zero-voltage turn-on. Because i_o is still freewheeling through D_1 and D_2, it can obtain $v_{ns} = 0$, $v_{Lo1} = v_{Lo2} = -V_o$, $v_{Lr1} = -v_{Cb1}$, $v_{Lr2} = -v_{Cb2}$ and $v_{Lr3} = -v_{Cb3}$. i_{p1}~i_{p3}, i_{Lo1} and all i_{Lo2} decrease. This step is ended when $i_{D2} = 0$. During this freewheeling interval, the currents i_{Lr1}~i_{Lr3} are decreased from $i_{Lo1}/(3n_1)$ to $-i_{Lo2}/(3n_1)$ and the current variation on L_{r1}~L_{r3} is about $I_o/(3n_1)$. The duty loss in step 4 is obtained as (1) shows:

$$d_{loss,4} = \frac{\Delta t_{34}}{T_{sw}} = \frac{I_o L_r f_{sw}}{3n_1 v_{Cb1}} \tag{1}$$

Step 5 [t_4~t_5]: After t_4, i_{D2} is decreased to zero so that D_2 is reverse biased. i_o flows through D_1, L_{o1} and L_{o2}. In step 5, power is transferred from V_{in} to R_o, $V_{Cf1} = V_{C2}$, $V_{Cf2} = V_{C3}$, $v_{Q1,ds} = V_{C1}$, $v_{Q3,ds} = V_{C2}$, $v_{Q5,ds} = V_{C3}$, $v_{Lm1} \approx -v_{Cb1}$, $v_{Lm2} \approx -v_{Cb2}$, $v_{Lm3} \approx -v_{Cb3}$, $v_{Lo1} = -V_o$ and $v_{Lo2} \approx v_{Cb1}/n_1 - V_o$. Thus, i_{p1}~i_{p3} and i_{Lo1} decrease and i_{Lo2} increases.

Step 6 [t_5~t_6]: When Q_2, Q_4 and Q_6 turn off at time t_5, the negative primary currents i_{p1}~i_{p3} rapidly charge C_{Q2}, C_{Q4} and C_{Q6}, respectively. On the other hand, C_{Q1}, C_{Q3} and C_{Q5} are discharged by i_{p1}~i_{p3} respectively. The secondary winding voltage v_{ns} is increased in this step.

Step 7 [t_6~t_7]: When C_{Q2}, C_{Q4} and C_{Q6} are charged to v_{Cb1}, v_{Cb2} and v_{Cb3} respectively at t_6, it can obtain $v_{ns} = 0$. Thus, i_o freewheels through D_1 and D_2 in this step and $v_{Lo1} = v_{Lo2} = -V_o$.

Step 8 [t_7~$t_0 + T_{sw}$]: When C_{Q1}, C_{Q3} and C_{Q5} are discharged to zero voltage at t_7, the body diodes D_{Q1}, D_{Q3} and D_{Q5} are forward biased. Power switches Q_1, Q_3 and Q_5 can be turned on at this moment to realize zero-voltage turn-on. Since i_o still freewheels through D_1 and D_2, it can obtain $v_{ns} = 0$, $v_{Lo1} = v_{Lo2} = -V_o$ and $v_{Lr1} = v_{Lr2} = v_{Lr3} = V_{in}/3 - v_{Cb1}$. Thus, i_{p1}~i_{p3} increase and i_{Lo1} and i_{Lo2} decrease. This step is ended when $i_{D1} = 0$. During this freewheeling interval, i_{Lr1}~i_{Lr3} increase from $-i_{Lo2}/(3n_1)$ to $i_{Lo1}/(3n_1)$. The duty loss in step 8 is obtained as (2) shows.

$$d_{loss,8} = \frac{I_o L_r f_{sw}}{3n_1(V_{in}/3 - v_{Cb1})} \tag{2}$$

At time $t_0 + T_{sw}$, i_{D1} is decreased to zero and this switching period is completed. Since the duty cycle of all switches equals 0.5, the voltage balance of C_1, C_2 and C_3 is well achieved with two balance capacitors C_{f1} and C_{f2}. If Q_1, Q_3 and Q_5 are in the on-state and Q_2, Q_4 and Q_6 are in the off-state, it obtains $v_{Cf1} = V_{C1}$ and $v_{Cf2} = V_{C2}$. If $V_{C1} > V_{C2}$ or $V_{C1} < V_{C2}$, then C_1 charges or discharges C_{f1} through Q_1 and Q_3. When Q_1, Q_3 and Q_5 are in the off-state and Q_2, Q_4 and Q_6 are in the on-state, it obtains $v_{Cf1} = V_{C2}$ and $v_{Cf2} = V_{C3}$. If $V_{C1} > V_{C2}$ or $V_{C1} < V_{C2}$, C_{f1} charges or discharges C_2 through Q_2 and Q_4. In a similar way, C_{f2} can be used to balance V_{C2} and V_{C3}. Therefore, V_{C1}~V_{C3} are all controlled at $V_{in}/3$.

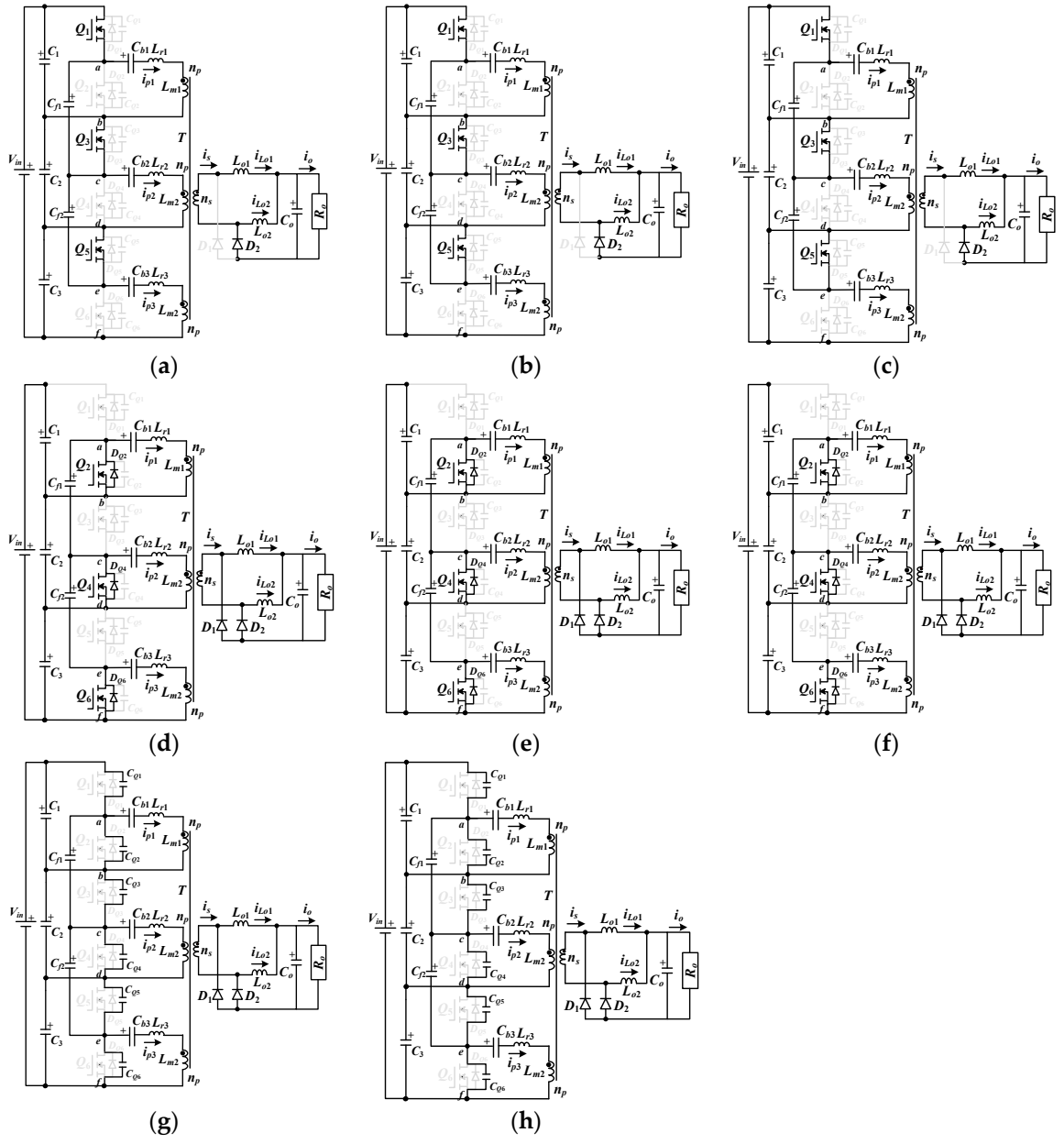

Figure 5. Operation steps of the power converter during one switching cycle (**a**) step 1 (**b**) step 2 (**c**) step 3 (**d**) step 4 (**e**) step 5 (**f**) step 6 (**g**) step 7 (**h**) step 8.

3. Circuit Characteristics

The asymmetric PWM scheme is adopted to drive Q_1~Q_6. Based on the flux balance of primary inductors such as (L_{r1} and L_{m1}), (L_{r2} and L_{m2}) and (L_{r3} and L_{m3}), the DC capacitor voltages V_{C1}~V_{C3} in a steady state can be obtained as $V_{Cb1} = V_{Cb2} = V_{Cb3} = dV_{in}/3$, where d is the duty cycle of Q_1, Q_3 and Q_5. In the same way, the output voltage can be derived from the flux balance of output inductors L_{o1} and L_{o2} in a steady state.

$$V_o = \frac{V_{in}}{3n_1} d(1-d) - \frac{I_o L_r f_{sw}}{3n_1^2} - V_f \tag{3}$$

where V_f is the voltage drop on D_1 and D_2.

Since the average winding currents i_{p1}~i_{p3} equal zero and $I_{Lo1} + I_{Lo2} = I_o$, the average inductor currents I_{Lo1} and I_{Lo2} are derived as $I_{Lo1} = (1 - d)I_o$ and $I_{Lo2} = dI_o$. The ripple currents on L_{o1} and L_{o2} are given in (4) and (5).

$$\Delta i_{Lo1} = \frac{V_o(1 - d + d_{loss,8})T_{sw}}{L_{o1}} = \frac{(1-d)V_oT_{sw} + \frac{V_oL_rI_o}{n_1(1-d)V_{in}}}{L_{o1}} \tag{4}$$

$$\Delta i_{Lo2} = \frac{V_o(d + d_{loss,4})T_{sw}}{L_{o2}} = \frac{dV_oT_{sw} + \frac{V_oL_rI_o}{n_1dV_{in}}}{L_{o2}} \tag{5}$$

The asymmetric PWM is adopted to regulate load voltage. From Figure 4, the turn-on time of D_1 is related to the duty cycle of Q_2 and the turn-on time of D_2 is related to the duty cycle of Q_1. Therefore, the average diode currents I_{D1} and I_{D2} are expressed as $I_{D1} = (1 - d)I_o$ and $I_{Lo2} = dI_o$. The voltage stress of diodes D_1 and D_2 is related to the secondary winding voltage. The secondary winding voltage v_{ns} is dependent on the input voltage V_{in} and clamped voltage V_{Cb1}. Thus, the voltage stress of D_1 and D_2 can be given in (6) and (7).

$$v_{D1} = (1 - d)V_{in}/(3n_1) \tag{6}$$

$$v_{D2} = dV_{in}/(3n_1) \tag{7}$$

The conduction losses on rectifier diodes D_1 and D_2 are approximately equal to I_oV_f. If the transformer is constructed, then the magnetizing inductances L_{m1}~L_{m3} are given. Thus, the ripple currents i_{Lm1}~i_{Lm3} are obtained in (8).

$$\Delta i_{Lm1} = \Delta i_{Lm2} = \Delta i_{Lm3} \approx \frac{(V_{in}/3 - v_{Cb1})(d - d_{loss,8})T_{sw}}{L_{m1}} = \frac{d(1-d)V_{in}T_{sw}}{3L_{m1}} - \frac{I_oL_r}{3n_1L_{m1}} \tag{8}$$

Three HB circuits are connected in a series on the high voltage side to reduce the voltage stress of active switches. Therefore, it is able to obtain the voltage stress of each active switch clamped at $V_{in}/3$. If the ripple currents on magnetizing inductors and output inductors are neglected, the root-mean-square (*rms*) currents $i_{Q1,rms}$~$i_{Q1,rms}$ can be derived as (9) and (10) show.

$$i_{Q1,rms} = i_{Q3,rms} = i_{Q5,rms} \approx \frac{(1-d)I_o\sqrt{d}}{3n_1} \tag{9}$$

$$i_{Q2,rms} = i_{Q4,rms} = i_{Q6,rms} \approx \frac{dI_o\sqrt{1-d}}{3n_1} \tag{10}$$

The conduction losses on Q_1~Q_6 are approximately equal to $d(1 - d)I_o^2R_{on}/(3n_1^2)$, where R_{on} is turn-on resistance of Q_1~Q_6. The positive peak currents of i_{p1}~i_{p3} at time t_1 are given in (11).

$$\begin{aligned} i_{p1}(t_1) = i_{p2}(t_1) = i_{p3}(t_1) \approx \quad & i_{Lm1,\max} + \tfrac{i_{Lo1,\max}}{3n_1} \approx \tfrac{d(1-d)V_{in}T_{sw}}{6L_{m1}} - \tfrac{I_oL_r}{6n_1L_{m1}} \\ & + \tfrac{(1-d)I_o}{3n_1} + \tfrac{(1-d)V_oT_{sw} + \frac{V_oL_rI_o}{n_1(1-d)V_{in}}}{6n_1L_{o1}} \end{aligned} \tag{11}$$

Likewise, the negative peak currents of i_{p1}~i_{p3} at time t_5 are given in (12).

$$i_{p1}(t_5) = i_{p2}(t_5) = i_{p3}(t_5) \approx i_{Lm1,\max} + \tfrac{i_{Lo1,\max}}{3n_1} \approx -\tfrac{d(1-d)V_{in}T_{sw}}{6L_{m1}} + \tfrac{I_oL_r}{6n_1L_{m1}} - \tfrac{dI_o}{3n_1} - \tfrac{dV_oT_{sw} + \frac{V_oL_rI_o}{n_1dV_{in}}}{6n_1L_{o2}} \tag{12}$$

The minimum primary current to realize zero-voltage turn-on switching of Q_1, Q_3 and Q_5 is given in (13).

$$i_{p1}(t_5) \geq \frac{V_{in}}{3}\sqrt{\frac{2C_Q}{L_{r1}}} \tag{13}$$

Similarly, the minimum primary current to realize zero-voltage turn-on switching of Q_2, Q_4 and Q_6 is given in (14).

$$i_{p1}(t_1) \geq \frac{V_{in}}{3}\sqrt{\frac{2C_Q}{L_{r1}}} \tag{14}$$

where $C_Q = C_{Q1} = C_{Q2} = C_{Q3} = C_{Q4} = C_{Q5} = C_{Q6}$.

4. Experimental Results

A laboratory prototype with 1.44 kW rated power was constructed and tested in order to verify the feasibility of the studied converter to supply the auxiliary power in a light rail vehicle from the DC microgrid system. The experimental circuit diagram of the developed converter is provided in Figure 6. The TL431 voltage regulator and photocoupler PC817 are used to regulate load voltage. The PWM UCC2893 is used to achieve asymmetric pulse-width modulation (APWM) generation. Pulse transformers are adopted to achieve electrical isolation and gate drive. The specifications of the experimental prototype are given in Table 1. The power rating of the magnetic transformer is the same as the transformer in the three-level converter and the two-level full-bridge converter. The turns-ratio of the transformer in the developed converter is one-third of the turns-ratio in the two-level full-bridge converter. The magnetizing voltage and primary turns of the transformer in the studied converter are only one-third of the magnetizing voltage and primary turns in the two-level full-bridge converter. The PC40 EER-42 magnetic core is used with 15 primary turns and 8 secondary turns to build the isolated transformer. The experimental results of the proposed converter while it supplies 1.44 kW to the output load under a 760 V input are shown in Figures 7–12. Based on the test results, the measured waveforms agree well with the theoretical waveforms as given in Figure 4. Figure 7 shows the gate voltages of Q_1~Q_6 at 20% and 100% loads. It is clear that Q_1, Q_3 and Q_5 have the same PWM waveforms. In the same manner, Q_2, Q_4 and Q_6 have the same PWM waveforms. The input split voltages and balance capacitor voltages at a full load are shown in Figure 8. From the experimental results, the input split voltages and two flying voltages are balanced well. The primary side currents of three HB circuits are illustrated in Figure 9. It is observed that the three primary currents are balanced well. Figure 10 gives the measured waveforms of three DC block capacitor voltages. It can be observed that the three voltages are balanced and the capacitor voltages are related to the duty cycle of Q_1, Q_3 and Q_5. Figure 11 shows the experimental waveforms of the secondary side currents. The ripple currents on L_{o1} and L_{o2} partially cancel each other so that the resultant ripple current on the load side is reduced. Figure 12 shows the test results of Q_1 and Q_2 at 20% and 100% loads. Before the switch is turned on, the switch current is negative to discharge the output capacitor C_Q to zero voltage. Thus, the mechanism of the zero-voltage turn-on switching is clearly achieved for both Q_1 and Q_2 from a 20% load. It can also be observed that all drain voltages of Q_1 and Q_2 are clamped at $V_{in}/3$. Since the PWM signals of the three HB circuits are identical and the input split voltages are also balanced, Q_3~Q_6 can also be turned on at zero-voltage from a 20% load. Figure 13 shows the circuit efficiency of the studied converter under different load cases. The measured maximum efficiency is about 93.6%. The main advantage of the studied converter is the lower voltage rating of power switches compared to the conventional three-level converter with eight MOSFETs and the two-level full-bridge converter with four IGBTs. Considering the turns-ratio of the transformer, the root-mean-square current of the studied converter is the same as the three-level and two-level converters. However, the lower conduction resistance of MOSFETs with lower voltage rating is used in the developed converter. Therefore, the total conduction losses (six MOSFETs) in the studied converter can be reduced compared to the three-level converter with eight MOSFETs and the full-bridge converter with four IGBTs.

Table 1. Prototype Specifications.

Items	Symbol	Parameter
Input voltage	V_{in}	760 V
Output voltage	V_o	24 V
Output current	I_o	60 A
Switching frequency	f_{sw}	100 kHz
Power switches	Q_1~Q_6	IRFP460
Rectifier diodes	D_1, D_2	MBR40100T
Split capacitors	C_1, C_2, C_3	330 μF/400 V
Flying capacitors	C_{f1}, C_{f2}	2.2 μF/630 V
Block capacitors	C_{b1}, C_{b2}, C_{b3}	750 nF/630 V
Turns ratio of T	n_p:n_p:n_p:n_s	15:15:15:8
Primary inductances	L_{r1}, L_{r2}, L_{r3}	30 μH
Magnetizing inductances	L_{m1}, L_{m2}, L_{m3}	0.8 mH
Output filter inductances	L_{o1}, L_{o2}	32 μH
Output filter capacitance	C_o	4400 μF/50 V

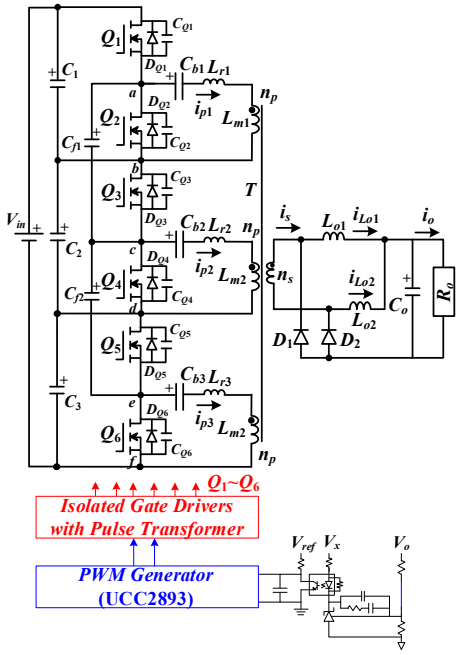

Figure 6. The experimental circuit diagram of the developed converter.

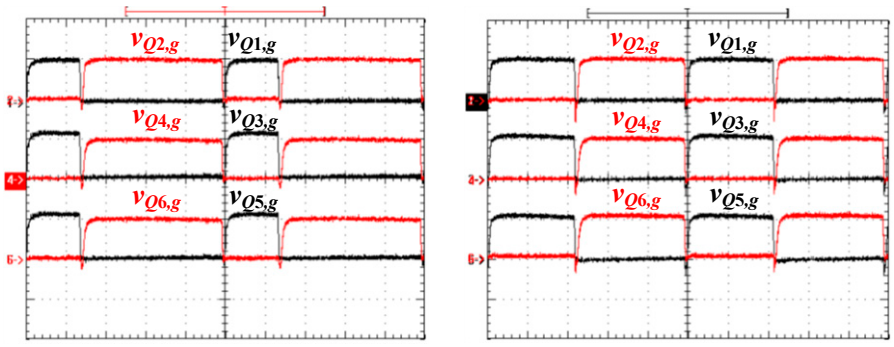

Figure 7. PWM signals of $Q1$~$Q6$ under (**a**) 20% load; (**b**) full load [v_{Q1}~v_{Q6}: 10 V/div; time: 2 μs].

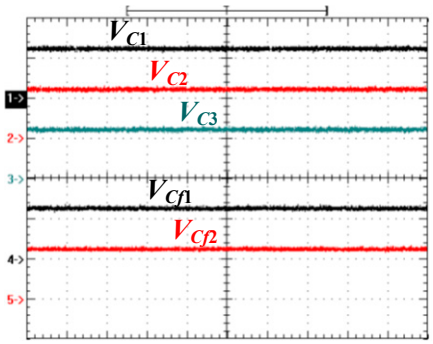

Figure 8. Measured input capacitor voltages under full load [V_{C1}~V_{Cf2}: 200 V/div; time: 2 μs].

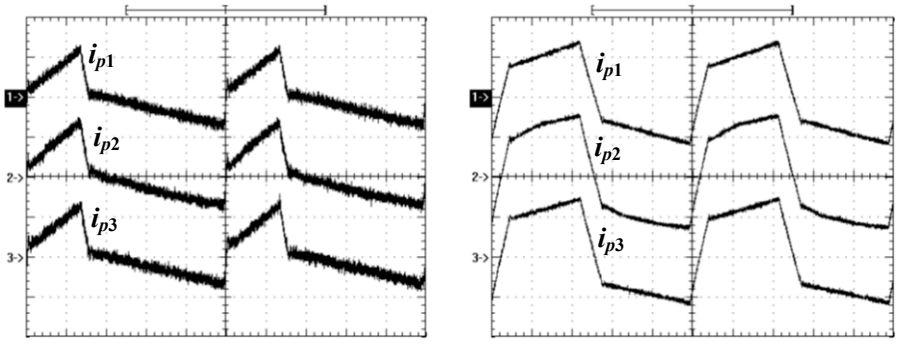

Figure 9. Test results of the primary side currents under (**a**) 20% load [i_{p1}~i_{p3}: 2 A/div; time: 2 μs]; (**b**) full load [i_{p1}~i_{p3}: 5 A/div; time: 2 μs].

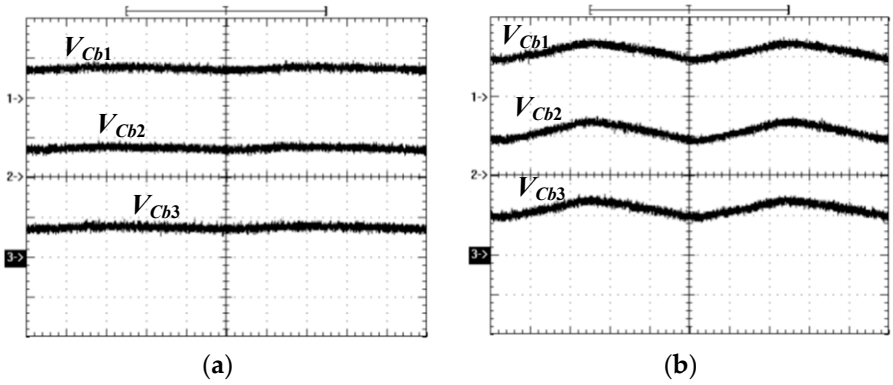

Figure 10. Test results of the primary capacitor voltages under (**a**) 20% load [V_{Cb1}~V_{Cb3}: 100 V/div; time: 2 μs]; (**b**) full load [V_{Cb1}~V_{Cb3}: 100 V/div; time: 2 μs].

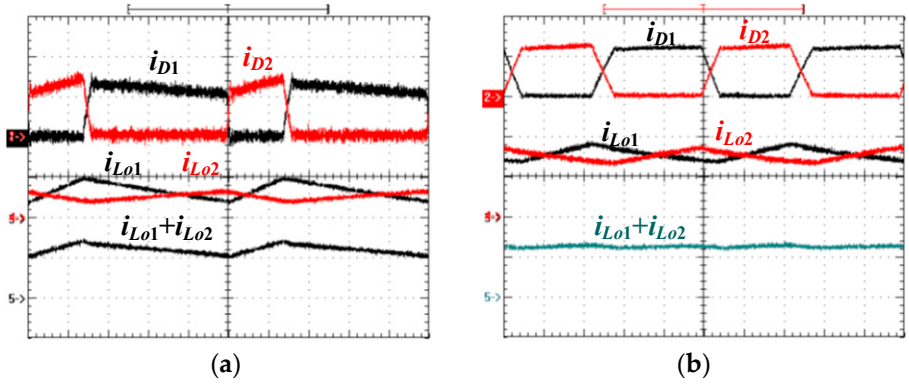

Figure 11. Measured secondary side currents at (**a**) 20% load [i_{D1}, i_{D2}, i_{Lo1}, i_{Lo2}, i_{Lo1} + i_{Lo2}: 10 A/div; time: 2 μs]; (**b**) 100% load [i_{D1}, i_{D2}, i_{Lo1} + i_{Lo2}: 50 A/div; i_{Lo1}, i_{Lo2}: 20 A/div; time: 2 μs].

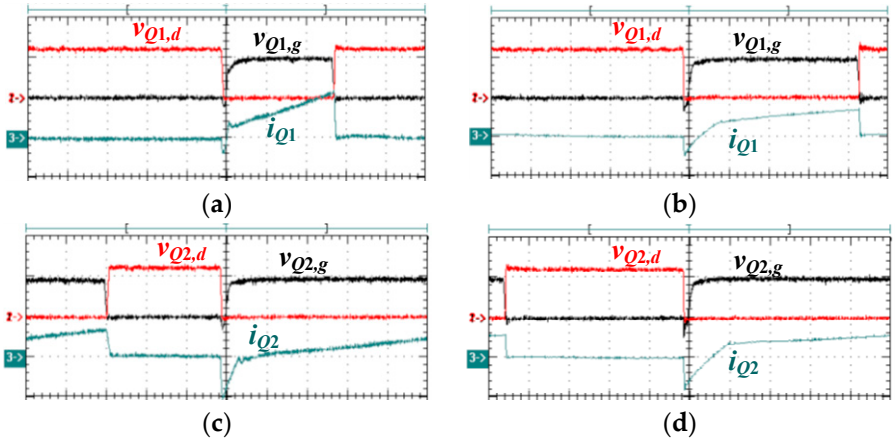

Figure 12. Measured switch voltages and current (**a**) Q_1 at 20% load [$v_{Q1,g}$: 10 V/div; $v_{Q1,d}$: 200 V/div; i_{Q1}: 2 A/div; time: 1 μs]; (**b**) Q_1 at full load [$v_{Q1,g}$: 10 V/div; $v_{Q1,d}$: 200 V/div; i_{Q1}: 10 A/div; time: 1 μs]; (**c**) Q_2 at 20% load [$v_{Q2,g}$: 10 V/div; $v_{Q2,d}$: 200 V/div; i_{Q2}: 2 A/div; time:1 μs]; (**d**) Q_2 at full load [$v_{Q2,g}$: 10 V/div; $v_{Q2,d}$: 200 V/div; i_{Q2}: 10 A/div; time: 1 μs].

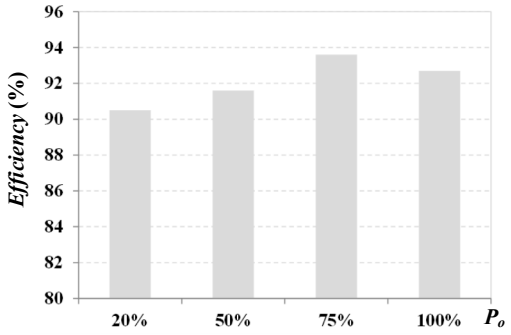

Figure 13. Test results of circuit efficiency.

5. Conclusions

In this paper, a series-connected HB converter with a single transformer is proposed for light rail transit applications. The proposed circuit's main benefits are the low voltage rating of power semiconductors, low switching losses, high circuit efficiency and balance split voltages compared to conventional converter topologies used in light rail vehicles. The asymmetric PWM scheme is used to control power switches, regulate output voltage and achieve the mechanism of the zero-voltage

turn-on switching. The circuit analysis, operation principle and design example of the proposed circuit are presented and discussed in detail. Finally, the feasibility of the studied circuit is verified by experimental results with a 1.44 kW laboratory prototype. The current harmonics on the input side is dependent on the switching frequency and the load current. The large current harmonics will result in unstable voltage on the input DC voltage bus. Therefore, in a future study, the interleaved DC/DC converter of the studied circuit will be developed to reduce the input current harmonics.

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References

1. Srwanson, J.D.; Thornes, C. Light-rail transit systems. *IEEE Veh. Technol. Mag.* **2010**, *5*, 22–27. [CrossRef]
2. Chaudhary, P.; Samanta, S.; Sesarma, P. Input-series-output-parallel-connected buck rectifiers for high-voltage applications. *IEEE Trans. Ind. Electron.* **2015**, *62*, 193–202. [CrossRef]
3. Dujic, D.; Kieferndorf, F.; Canales, F.; Drofenik, U. Power electronic traction transformer technology. In Proceedings of the Power Electronics and Motion Control Conference (IPEMC Conference), Harbin, China, 2–5 June 2012; pp. 636–642.
4. Chaudhary, P.; Sesarma, P. Front-end buck rectifier with reduced filter size and single-loop control. *IEEE Trans. Ind. Electron.* **2013**, *60*, 4359–4368. [CrossRef]
5. Akagi, H. Classification, terminology, and application of the modular multilevel cascade converter (MMCC). *IEEE Trans. Power Electron.* **2011**, *26*, 3119–3130. [CrossRef]
6. Winkelnkemper, M.; Korn, A.; Steimer, P. A modular direct converter for transformerless rail interties. In Proceedings of the 2010 IEEE International Symposium on Industrial Electronics (IEEE ISIE Conference), Bari, Italy, 4–7 July 2010; pp. 562–567.
7. Coppola, M.; Del Pizzo, A.; Iannuzzi, D. A power traction converter based on modular multilevel architecture integrated with energy storage devices. In Proceedings of the Electrical systems for Aircraft, Railway and Ship Propulsion Conference, Bologna, Italy, 16–18 October 2012; pp. 1–7.
8. Alexandre, C.; Drazen, D. Galvanically isolated modular converter. *IET Proc. Power Electron.* **2016**, *9*, 2318–2328.
9. Nakanishi, T.; Itoh, J.I. Evaluation of isolation three-phase AC/DC converter using modular multilevel converter topology. In Proceedings of the 2014 International Power Electronics Conference (IEEE IPEC Conference), Hiroshima, Japan, 18–21 May 2014; pp. 1095–1111.
10. Mcneill, N.; Yuan, X.; Anthony, P. High-efficiency multilevel converter technology for electric vehicle applications using super-junction MOSFETs. In Proceedings of the IET Hybrid and Electric Vehicle Conference, London, UK, 5–6 November 2014; pp. 1–7.
11. Madhusoodhanan, S.; Tripathi, A.; Patel, D.; Mainali, K.; Kadavelugu, A.; Hazra, S.; Bhattacharya, S.; Hatua, K. Solid-state transformer and MV grid tie applications enabled by 15kV SiC IGBTs and 10kV SiC MOSFETs based multilevel converters. *IEEE Trans. Ind. Appl.* **2015**, *51*, 3343–3360. [CrossRef]
12. Satarupa, B.; Akshay, K.R.; Srinivasan, D. Naturally clamped snubberless soft-switching bidirectional current-fed three-phase push–pull DC/DC converter for DC microgrid application. *IEEE Trans. Ind. Appl.* **2016**, *52*, 1577–1587.
13. Zhang, J.; Wu, H.; Qing, X.; Xing, Y. PWM plus secondary-side phase-shift controlled soft-switching full-bridge three-port converter for renewable power systems. *IEEE Trans. Ind. Electron.* **2015**, *62*, 7061–7072. [CrossRef]
14. Gu, L.; Jin, K.; Liu, C. Current-tripler-rectifier pulse width modulation ZVS three-phase full-bridge DC/DC converter with Y–Δ connected transformer. *IET Proc. Power Electron.* **2015**, *8*, 1111–1118. [CrossRef]
15. Hiroyuki, H.; Kurokawa, F. Modulation method of a full-bridge three-level LLC resonant converterfor battery charger of electrical vehicles. *IEEE Trans. Power Electron.* **2017**, *32*, 2498–2507.

16. Korotkov, S.; Meleshin, V.; Nemchinov, A.; Fraidlin, S. Small-signal modeling of soft-switched asymmetrical half-bridge DC/DC converte. In Proceedings of the APEC'95, Conference Proceedings 1995, Tenth Annual Applied Power Electronics Conference and Exposition, 1995 (IEEE APEC), Dallas, TX, USA, 5–9 March 1995; Volume 2, pp. 707–711.
17. Tschirhart, D.J.; Jain, P.K. Design procedure for high-frequency operation of the modified series-resonant APWM converter to reduce size and circulating current. *IEEE Trans. Power Electron.* **2012**, *27*, 4181–4191. [CrossRef]
18. Kim, B.C.; Park, K.B.; Moon, G.W. Asymmetric PWM control scheme during hold-up time for LLC resonant converter. *IEEE Trans. Ind. Electron.* **2012**, *59*, 2992–2997. [CrossRef]
19. Haga, H.; Kurokawa, F. A novel modulation method of the full bridge three-level LLC resonant converter for battery charger of electrical vehicles. In Proceedings of the 2015 IEEE Energy Conversion Congress and Exposition (IEEE ECCE Conference), Montreal, QC, Canada, 20–24 September 2015; pp. 5498–5504.
20. Johnson, S.; Erickson, R. Steady-state analysis and design of the parallel resonant converter. *IEEE Trans. Power Electron.* **1988**, *3*, 93–104. [CrossRef]
21. Gu, Y.; Lu, Z.; Hang, L.; Qian, Z.; Huang, G. Three-level LLC series resonant DC/DC converter. *IEEE Trans. Power Electron.* **2005**, *20*, 781–789. [CrossRef]
22. Mishima, T.; Akamatsu, K.; Nakaoka, M. A high frequency-link secondary-side phase-shifted full-bridge soft-switching PWM DC-DC converter with ZCS active rectifier for EV battery charged. *IEEE Trans. Power Electron.* **2013**, *28*, 5758–5773. [CrossRef]
23. Lin, B.R.; Shiau, T.Y. Zero-voltage switching full-bridge DC/DC converter with parallel-connected output and without output inductor. *IET Proc. Power Electron.* **2013**, *6*, 505–515. [CrossRef]
24. Safaee, A.; Jain, P.; Bakhshai, A. A ZVS pulsewidth modulation full-bridge converter with a low rms current resonant auxiliary circuit. *IEEE Trans. Power Electron.* **2016**, *31*, 4031–4047. [CrossRef]