Analysis of Power Loss and Improved Simulation Method of a High Frequency Dual-Buck Full-Bridge Inverter

Authors:

Zhun Meng, Yi-Feng Wang, Liang Yang, Wei Li

Date Submitted: 2019-12-10

Keywords: Simulation, loss analysis, high frequency conversion, dual-buck inverter, grid-connected generation, SiC power device

Abstract:

A high frequency dual-buck full-bridge inverter for small power renewable energy application is proposed in this paper. A switching frequency of 400 kHz is achieved with the adoption of the SiC power device. A two-pole two-zero (2P2Z) compensator is employed in the outer voltage loop to generate the current reference for inner current loop. A 3P3Z compensator is adopted in the inner current loop to track the current reference. A systematic way for calculating the losses of high frequency inverter is presented, and the losses of the components are thoroughly analyzed. The turn-on and turn-off procedures of the inverter are discussed in detail. The losses caused by high frequency are calculated accurately, and the loss distribution is established as well. The procedure of the loss analysis gives a practical example for calculating the loss of similar type inverters. Moreover, deviation between pulse width modulation (PWM) control signal and switching response in high frequency switching is thoroughly analyzed. The influence of deviation is verified by designed experiment. Hence, a compensation method is proposed in order to minimize the influence. The compensation effect is validated by experiment and simulation. Finally, a 1-kW prototype is built to verify the feasibility of the theoretical analyses. The grid-connected maximum output power experiment is completed at 1 kW with the efficiency of 96.1% and the total harmonic distortion (THD) of 1.8%. The comparison experiments of power loss between Si and SiC power devices are carried out. The experiment results confirm the loss calculation method to be valid.

Record Type: Published Article

Submitted To: LAPSE (Living Archive for Process Systems Engineering)

Citation (overall record, always the latest version):	LAPSE:2019.1444
Citation (this specific file, latest version):	LAPSE:2019.1444-1
Citation (this specific file, this version):	LAPSE:2019.1444-1v1

DOI of Published Version: https://doi.org/10.3390/en10030311

energies

MDPI

Article

Analysis of Power Loss and Improved Simulation Method of a High Frequency Dual-Buck Full-Bridge Inverter

Zhun Meng, Yifeng Wang *, Liang Yang and Wei Li

School of Electrical Engineering and Automation, Tianjin University, Tianjin 300072, China; quakermaster@hotmail.com (Z.M.); zyangliang@tju.edu.cn (L.Y.); liweitju@hotmail.com (W.L.)

* Correspondence: wayif@tju.edu.cn; Tel.: +86-132-0769-7161; Fax: +86-022-2740-1479

Academic Editor: Gabriele Grandi

Received: 24 January 2017; Accepted: 2 March 2017; Published: 6 March 2017

Abstract: A high frequency dual-buck full-bridge inverter for small power renewable energy application is proposed in this paper. A switching frequency of 400 kHz is achieved with the adoption of the SiC power device. A two-pole two-zero (2P2Z) compensator is employed in the outer voltage loop to generate the current reference for inner current loop. A 3P3Z compensator is adopted in the inner current loop to track the current reference. A systematic way for calculating the losses of high frequency inverter is presented, and the losses of the components are thoroughly analyzed. The turn-on and turn-off procedures of the inverter are discussed in detail. The losses caused by high frequency are calculated accurately, and the loss distribution is established as well. The procedure of the loss analysis gives a practical example for calculating the loss of similar type inverters. Moreover, deviation between pulse width modulation (PWM) control signal and switching response in high frequency switching is thoroughly analyzed. The influence of deviation is verified by designed experiment. Hence, a compensation method is proposed in order to minimize the influence. The compensation effect is validated by experiment and simulation. Finally, a 1-kW prototype is built to verify the feasibility of the theoretical analyses. The grid-connected maximum output power experiment is completed at 1 kW with the efficiency of 96.1% and the total harmonic distortion (THD) of 1.8%. The comparison experiments of power loss between Si and SiC power devices are carried out. The experiment results confirm the loss calculation method to be valid.

Keywords: SiC power device; grid-connected generation; dual-buck inverter; high frequency conversion; loss analysis; simulation

1. Introduction

In order to make the social development less fossil fuel-dependent and more environment-friendly, renewable energy becomes an important alternative energy source [1,2]. With the development of distributed renewable energy generation, small-scale inverter becomes a focus of research. Being able to convert all kinds of distributed energy into a unified AC power, the grid-connected inverter extensively broadens the application range of renewable energies, and thus acts as an indispensable role in the renewable energy generation system [3,4].

For the rapid development of the new power devices, the wide band gap power devices, such as SiC and GaN, begin to replace the traditional Si power devices. Its outstanding performance, including high switching speed, low switching loss, high stability in high temperature operating and so on, makes the high frequency inverter a new research hot spot. A three-level SiC inverter is proposed in [5]. By employing the SiC MOSFET and FPGA control platform, a 100 kHz switching frequency is achieved. GaN high-electron mobility transistors (HEMT) power devices are adopted in a single-phase

T-Type inverter in [6]. Switching performance and efficiency performance are analyzed among Si, SiC and GaN HEMT. The results demonstrate the advantage of the wide band gap power devices in high frequency inverting. It can be seen that all these inverters adopt the wide band gap power devices and have a working frequency, which is much higher than the traditional ones. As a result, the THD of the inverters is significantly reduced and the output power quality is improved obviously. Meanwhile, smaller components can be used and the volume of the inverter is significantly decreased, which broaden the application range of the inverter. On the other hand, as frequency increases, the losses of the inverter under high frequency circumstances become a major problem, which is not discussed in detail in this paper.

With the application of high frequency switching, loss analysis is even more important, because it can offer a guideline for the system efficiency improvement [7–14]. In [7], a detailed investigation into loss distribution for diverse components is conducted, which includes losses of switches, diodes, inductors and capacitors. In [8,9], the switch and diode losses of several inverter topologies are studied and compared, which gives an evident insight into the loss distribution for each low-frequency topology. Nevertheless, this comparison may show less accuracy when it comes to high frequency case, because more details of the switching procedure must be taken into account in the high frequency operation, which will affect the losses and are not included in this literature. In [10], the mechanism reflecting the relation between transition characteristics and power losses is discussed. Diode losses based on traditional Si semi-conductor are analyzed as well. In [11], comparative experiments of losses between Si and SiC power devices are carried out, which proves that the SiC devices are superior in switching speed, operating temperature and switching losses than the traditional Si. Although the loss analyses previously mentioned are very comprehensive and detailed, all these works are also based on traditional low frequency simplified method, which show less accuracy for the high frequency loss analysis. This is because some losses, overlooked in low frequency condition, may become an indispensable part of the total losses in high frequency implementation. Hence, deviations will be introduced if low frequency loss calculation method is implanted directly into the high frequency operation.

Moreover, the influence of the high frequency switching is not confined to losses analysis. The impact of high frequency on the simulation model is also noteworthy. Model of the wide band gap power devices are established in [15–19]. A compact model of the SiC metal-oxide-semiconductor field-effect transistor (MOSFET) is built including the carrier-trap influences in [15], the simulation results is verified by the experiments. Jun Wang et al. [16] discusses a 10-kV 4H-SiC MOSFET and key characteristics are extensively investigated. A simple behavioral SPICE model for the SiC MOSFETs is proposed to predict their realistic application prospect. The impact of nonlinear junction capacitance on switching transient is studied in [17], and a simulation circuit for switching transient analysis is built. A dynamic model of GaN cascaded current aperture vertical electron transistor (CAVET) is established in ATLAS-SPICE-integrated simulator. The simulation model successfully models and projects the switching performance of the GaN CAVET. These simulation models are very thorough. However, most of the researches concentrate on the component level influence. The impact of high frequency switching on the output of the converter is not detailed discussed. On the other hand, the component level model is too complicated and time-consuming for converter analysis. The influence of high frequency switching on the inverter simulation model is rarely studied.

In this paper, a high frequency single phase dual-buck full-bridge grid-connect inverter for small power renewable energy is proposed. The SiC components, as the power devices, are employed to achieve high switching frequency and to limit the conversion loss simultaneously. For the controller, the proposed inverter adopts a current voltage dual-loop. The 3P3Z compensator is adopted in the inner current loop in order to track the current reference which is generated by the 2P2Z compensator. The 2P2Z compensator is employed in the outer voltage loop in order to regulate the DC bus voltage by balancing the input and output power. A systematic way for calculating the losses of high switching frequency inverter is presented. The losses of each component in the inverter are thoroughly analyzed.

The switching procedure and the corresponding losses are discussed in detail. The high frequency losses are also taken into account during the analysis. The distribution of the losses is established based on the presented method. Moreover, the deviation between PWM control signal and switching response, which emerges in high frequency switching, is thoroughly analyzed. A designed experiment verifies the influence of deviation. Thus, a compensation method is proposed in order to minimize the influence of deviation. Experiment and simulation confirm the compensation effect. Finally, a 1-kW prototype is made and a 400 kHz switching frequency is achieved. The comparison experiments of the power losses are carried out between Si and SiC power devices to verify the loss calculation method. The results proved the loss analysis is valid.

2. Circuit Configuration and Control Method

2.1. Operation Principles

The topology of the dual-buck full-bridge inverter is presented in Figure 1a. The inverter can be regarded as two individual buck converters. Buck 1 consists of S_1, S_3, D_1 and L_{i1}, connecting to the DC bus positively. Buck 2 consists of S_2, S_4, D_2 and L_{i2}, connecting to the bus negatively. The output inductors of the buck converters L_{i1} and L_{i2} constitute a LCL filter with C_f, L_{g1} and L_{g2}.

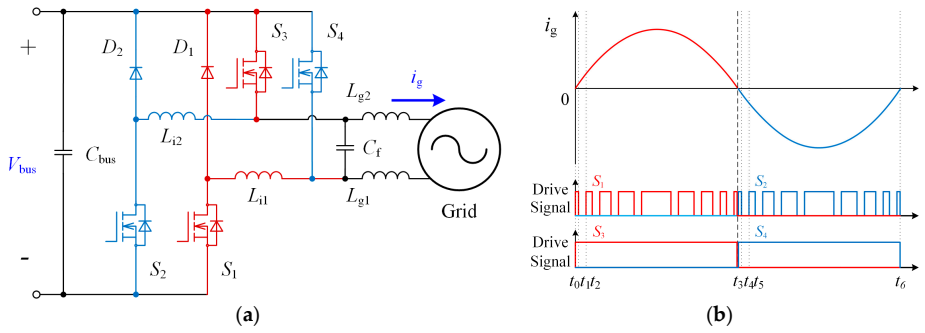


Figure 1. The topology and key waveforms of the proposed inverter: (**a**) the topology of the inverter; and (**b**) the key waveforms of the inverter.

To drive the inverter, the unipolar modulation has been adopted and the waveforms of the driving signal are shown in Figure 1b. In one AC cycle, both bucks work in their own half cycles separately. When Buck 1 works, S_3 keeps turn-on in the half AC cycle and S_1 switches at high frequency to follow a sinusoidal reference in order to generate the positive half of the grid current i_g. D_1 offers the free-wheeling path when S_1 turns off. Unlike the H-bridge inverter, no switches are at the same leg. Accordingly, the dead time is no longer needed. Moreover, the free-wheeling current is running through D_1 instead of the body diode. Because the independent diodes have a better performance, the total losses of the inverter can be reduced. The operation principle of Buck 2 is similar to Buck 1 and will not be discussed further.

2.2. Control Theory

The control system structure of the inverter is shown in Figure 2. For the renewable energy distributed generation application, two-stage system structure is often adopted. The gird-connected inverter as the post-stage is responsible for transferring the energy into power grid. The inverter can stabilize the DC bus voltage by balancing the input and output power. A voltage-current dual loop is employed to fulfill the function which is mentioned above.

A notch filter is used to filter out the ripple in the bus voltage V_{bus}. By comparing with the bus voltage reference V_{bus_ref}, the bus voltage error is acquired and compensated by a 2P2Z compensator. Then, the current reference amplitude i_{ref} is generated by the 2P2Z compensator. The grid voltage signal is injected into a second-order generalized integrator software phase lock loop

(SOGI-SPLL) to generate the phase reference which is used to synchronize i_{ref} with the grid voltage. The instantaneous current reference i_{ref_inst} is compensated by a 3P3Z compensator. The result goes through a feedback linearization module and becomes the duty cycle which is used to generate PWM signal to control the inverter. The detail of the control method is described in another article and will not be discussed further.

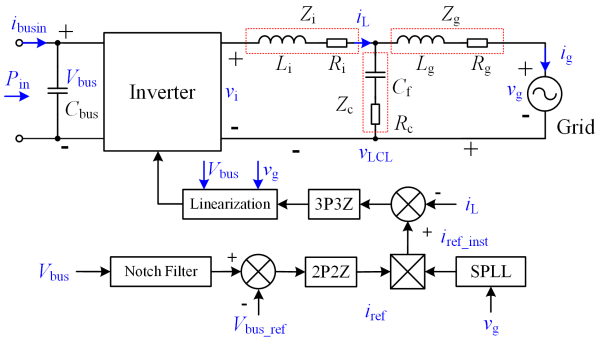


Figure 2. Control structure of the inverter.

3. Loss Analysis

The loss analysis is an essential way to improve the system efficiency. For low frequency inverter, the traditional calculation and approximation method are proven to be effective. However, when high speed switching is adopted, the losses, which are overlooked in low frequency condition, may become an indispensable part of the total losses and cause the inaccurate of loss analysis. In this section, the losses of inverter are systematically analyzed. The switching procedure, including the miller effect, is discussed in detail. The high frequency loss is thoroughly analyzed, some of which are not taken into consideration in low frequency applications. Moreover, the loss distribution based on the new method can offer a more accurate and detailed guide line for the improvement of high frequency application.

Before the analysis, several assumptions are made in order to simplify the procedure:

1. The influence of some parasitic parameters such as leakage inductance is not considered.
2. The temperature influence on device parameters is not discussed. If the parameter is temperature dependent, the calibration is only based on the datasheet. The analysis is conducted considering the inverter operating temperature is 60 °C.
3. The parameters of the symmetry components are same and match the datasheet.
4. The losses of the symmetry components are considered to be the same.

3.1. High Side MOSFET Loss

Basing on operation principles in Section 2, the high side MOSFETs S_3, S_4 are working at AC frequency. Comparing with the conduction loss, the switching loss can be ignored for their low switching frequency. The D-S current of the high side MOSFET S_3 i_{hi_S3} is shown in Figure 3.

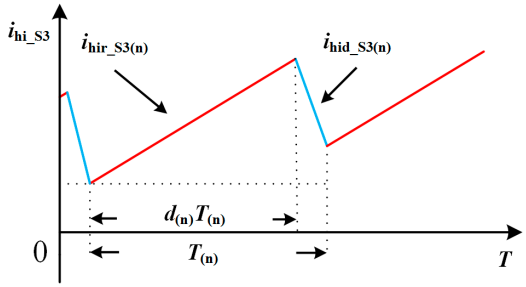


Figure 3. The D-S current of the high side MOSFET S_3.

When S_3 is turned on, the switching of the low side MOSFET S_1 divides i_{hi_S3} into two parts. When S_1 turns on, i_{hi_S3} rises, i_{hi_S3} flows through S_1, and the current is in rising period; when S_1 turns off, i_{hi_S3} falls, i_{hi_S3} flows through D_1, and the current is in falling period. The switching of S_1 causes the fluctuation of i_{hi_S3}. T_{grid} is the gird period. T(n) is the nth switching period of the low side switch S_1 and the duty cycle is d(n), the nth conducting time is d(n)T(n). $i_{hir\_S3(n)}$ is the nth rising period of i_{hi_S3} which is also the turn-on current of S_1. $i_{hid\_S3(n)}$ is the falling period which is also the free-wheeling current of D_1. N_s is the number of S_1 switching period which is contained in one AC period. The conduction loss of the high side MOSFET S_3 P_{hicon_S3} can be divided into two parts:

$$P_{hircon\_S3} = \frac{1}{T_{grid}}[\sum_{n=1}^{N_s}(\int_0^{d(n)T(n)} i_{hir(n)}^2(t)R_{DS\_S3}dt)] \quad (1)$$

$$P_{hidcon\_S3} = \frac{1}{T_{grid}}[\sum_{n=1}^{N_s}(\int_0^{[1-d(n)]T(n)} i_{hid(n)}^2(t)R_{DS\_S3}dt)] \quad (2)$$

$$P_{hicon\_S3} = P_{hircon\_S3} + P_{hidcon\_S3} \quad (3)$$

where P_{hircon_S3} is the i_{hi_S3} rising period loss and P_{hidcon_S3} is the falling period loss, R_{DS_S3} is the D-S resistance of S_3 which can be obtained from datasheet.

3.2. Low Side MOSFET Loss

The conduction loss of the low side MOSFET S_1, P_{locon_S1} can be easily deduced from Equation (1). The conduction current is the same as P_{hircon_S3} and the only difference is the D-S resistance. R_{DS_S1} is the D-S resistance of S_1. P_{locon_S1} can be calculated as:

$$P_{locon\_S1} = \frac{1}{T_{grid}}[\sum_{n=1}^{N_s}(\int_0^{d(n)T(n)} i_{hir(n)}^2(t)R_{DS\_S1}dt)] \quad (4)$$

According to the operation principles, low side MOSFETs S_1, S_2 are working at 400 kHz. Figure 4a shows the voltage waveforms of S_1 during the turn-on transition and the Figure 4b is the simplified diagram of the transition.

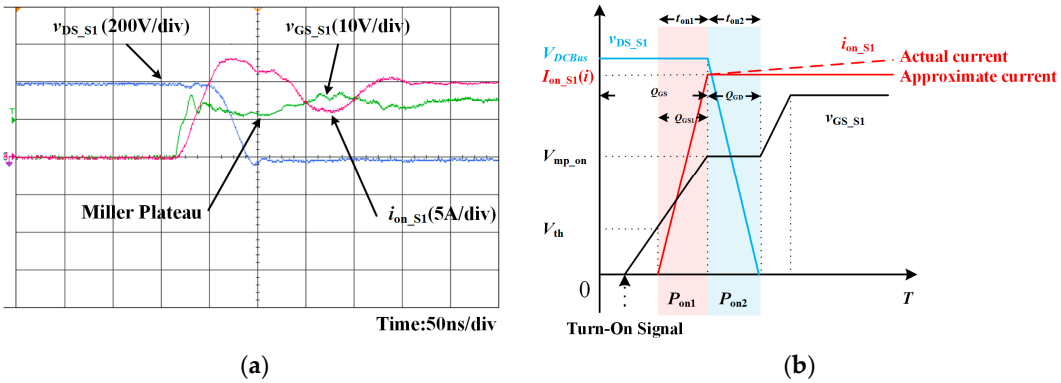


Figure 4. The waveforms during turn-on transition: (**a**) the measured waveform during the turn-on transition; and (**b**) the simplified diagram of the turn-on transition.

As Figure 4b shows, an approximation is made in order to simplify the analysis. The D-S current of S_1 i_{on_S1} is considered to be a constant current after i_{on_S1} is fully turn-on. When a signal starts to turn on S_1, there is a time delay before G-S voltage of S_1 v_{GS_S1} increases to the gate threshold voltage V_{th}. Then, the output capacitance of S_1, C_{OSS_S1} begins to be charged. The output capacitance loss P_{OSS_S1} can be calculated as:

$$P_{OSS\_S1} = f_{SW} \times \int_0^{V_{DCBus}} v_{DS\_S1} C_{OSS\_S1}(v_{DS\_S1}) dv_{DS\_S1} \quad (5)$$

where f_{SW} is the switching frequency of S_1, V_{DCBus} is the input DC bus voltage and v_{DS_S1} is the D-S voltage of S_1. The output capacitance C_{OSS_S1} is a v_{DS_S1} related parameter which is provided by the datasheet.

When v_{GS_S1} reaches V_{th}, the i_{on_S1} starts to rise linearly. After the rising period, i_{on_S1} turns on completely, the v_{GS_S1} reaches the turn-on miller plateau voltage V_{mp_on} and the voltage v_{DS_S1} starts to decrease. The miller plateau is caused by the charging or discharging procedure of the capacitance between G-D, which is C_{GD} [20]. In actual waveform, as Figure 4a shows, miller plateau have a slope. The steepness of the slope is depending on the value of C_{GD} and C_{GS}, where C_{GS} is the capacitance between G-S. Typically, C_{GD} is larger than C_{GS}, the phenomenon appears as a plateau. The duration time can be considered as the charging time to charge Q_{GD}, which is the gate to drain charge.

At the end of the miller plateau, the v_{GS_S1} reduces to zero and the turn-on procedure is completed. During the turn-on transition, the turn-on loss P_{on} can be divided into two parts: P_{on1} and P_{on2}. The v_{GS_S1} is constant and i_{S1} is linearly changed during t_{on1}. Similarly, the i_{S1} is constant and v_{GS_S1} is linearly changed within t_{on2}. The turn-on loss of S_1 P_{on_S1} can be deduced form Equation (6).

$$P_{on\_S1} = \frac{1}{T_{grid}} \sum_{n=1}^{Ns} \frac{V_{DCBus} I_{on\_S1(n)}}{2} (t_{on1} + t_{on2}) = \frac{1}{T_{grid}} \sum_{n=1}^{Ns} \frac{V_{DCBus} I_{on\_S1(n)}}{2} \left(\frac{Q_{GS2} R_{Gon}}{\frac{V_{mp\_on} + V_{th}}{2}} + \frac{Q_{GD} R_{Gon}}{V_{mp\_on}} \right) \quad (6)$$

where $I_{on\_S1(n)}$ is the nth switching period turn-on current of S_1. Q_{GS2} represents the corresponding charge during t_{on1} which can be calculated according to the transfer characteristic figure of devices, R_{Gon} is the gate loop resistance during turn-on period.

Figure 5a shows the waveforms of S_1 during the turn-off transition and the Figure 5b is the simplified diagram of the transition. A similar approximation is made which considers the D-S turn-off current of S_1 i_{off_S1} to be constant before t_{off2}. When the signal starts to turn off S_1, v_{GS_S1} starts to decrease. The v_{GS_S1} begins to increases when v_{GS_S1} reaches the turn-off miller plateau voltage V_{mp_off}. At the end of the plateau, v_{GS_S1} stops increasing and i_{off_S1} starts to decrease. The turn-off transition is completed when v_{GS_S1} goes down to V_{th} and i_{off_S1} decreases to zero. The turn-off loss P_{off_S1} can be regarded as two parts: P_{off1} during t_{off1} and P_{off2} during t_{off2} which can be calculated by Equation (7).

$$P_{off\_S1} = \frac{1}{T_{grid}} \sum_{n=1}^{Ns} \frac{V_{DCBus} I_{off\_S1(n)}}{2} (t_{off1} + t_{off2}) = \frac{1}{T_{grid}} \sum_{n=1}^{Ns} \frac{V_{DCBus} I_{off\_S1(n)}}{2} \left(\frac{Q_{GD} R_{Goff}}{V_{mp\_off}} + \frac{Q_{GS2} R_{Goff}}{\frac{V_{mp\_off} + V_{th}}{2}} \right) \quad (7)$$

where $I_{off\_S1(n)}$ is the nth switching period turn-off current of S_1. R_{Goff} is the gate loop resistance during turn-off period. The total loss of S_1 P_{loss_S1} is regarded as:

$$P_{loss\_S1} = P_{locon\_S1} + P_{OSS\_S1} + P_{on\_S1} + P_{off\_S1} \quad (8)$$

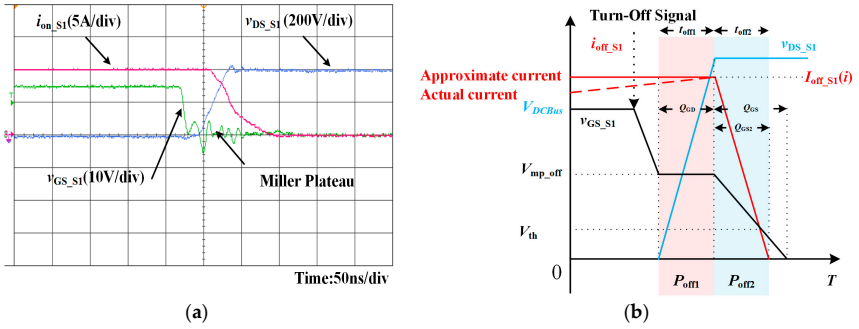


Figure 5. The voltage and current waveforms during turn-off transition: (**a**) the measured waveform during the turn-off transition; and (**b**) the simplified diagram of the turn-off transition.

3.3. Free-Wheeling Diode Loss

The conduction loss of the free-wheeling diode D_1, $P_{\mathrm{dcon\_D1}}$ can be deduced from Equation (2), which is shown in Equation (9):

$$P_{\mathrm{dcon\_D1}} = \frac{1}{T_{\mathrm{grid}}}[\sum_{n=1}^{N_{\mathrm{s}}}(\int_{0}^{[1-d(\mathrm{n})]T(\mathrm{n})} i_{\mathrm{hid(n)}} U_{\mathrm{f}} \mathrm{d}t)] \tag{9}$$

U_{f} is the forward voltage of the diode. The turn-on loss of the diode $P_{\mathrm{ond\_D1}}$ can be represented as (10):

$$P_{\mathrm{ond\_D1}} = \frac{1}{T_{\mathrm{grid}}}\sum_{\mathrm{n}=1}^{N_{\mathrm{s}}}\frac{1}{2}U_{\mathrm{d}} I_{\mathrm{don(n)}} t_{\mathrm{r}} \approx \frac{1}{T_{\mathrm{grid}}}\sum_{\mathrm{n}=2}^{N_{\mathrm{s}}}\frac{1}{2}U_{\mathrm{DCBus}} I_{\mathrm{off\_S1(n-1)}} t_{\mathrm{on1}} \tag{10}$$

where U_{d} is the voltage on the diode. $I_{\mathrm{don(n)}}$ is the nth diode turn-on current which can be approximated as the (n − 1)th turn-off current of S_1 $I_{\mathrm{off\_S1(n-1)}}$. t_{r} is the rising time of the S_1 which can be approximated as t_{on1}.The turn-on loss of the diode $P_{\mathrm{offd\_D1}}$ can be represented as (11):

$$P_{\mathrm{offd\_D1}} = \frac{1}{T_{\mathrm{grid}}}\sum_{\mathrm{n}=1}^{N_{\mathrm{s}}}\frac{1}{2}U_{\mathrm{d}} i_{\mathrm{RM(n)}} t_{\mathrm{rr}} = \frac{1}{T_{\mathrm{grid}}}\sum_{\mathrm{n}=1}^{N_{\mathrm{s}}}\frac{1}{2}U_{\mathrm{DCBus}} i_{\mathrm{RM(n)}} t_{\mathrm{rr}} \tag{11}$$

I_{RM} is the diode peak reverse current and t_{rr} is the reverse recovery time.

3.4. Inductor Loss

The copper loss P_{LCu} of filter inductor can be calculated as

$$P_{\mathrm{LCu}} = \frac{1}{T_{\mathrm{grid}}}\int_{0}^{T_{\mathrm{grid}}} i_{\mathrm{L}}^{2}(t) R_{\mathrm{L}} \mathrm{d}t \tag{12}$$

where i_{L} is the inductor current and the R_{L} is the resistance of the inductor winding.

Figure 6 shows the trajectory of inductor current i_{L} on the B-H plane during one switching cycle. At the end of the switching cycle, the i_{L} is not the same as the initial value because the inverter is working in continuous current mode in order to follow the sinusoidal reference. The work mode leads to the unclosed B-H curve as Figure 6 shows. Accordingly, the traditional hysteresis loss calculation based on closed B-H curve is not suitable for inverter hysteresis loss calculation. The unclosed B-H curve should be adopted [21–23].

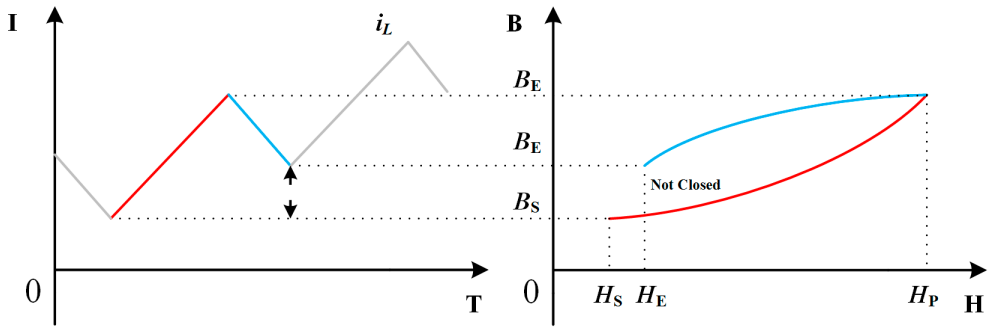


Figure 6. The B-H curve during on switch cycle.

Magnetic flux density B can be obtained by integral of the inductor voltage u_{L}. The magnetic flux density at t_{n} can be calculated as:

$$B(t_{\mathrm{n}}) = \frac{1}{N \cdot A}\int_{0}^{t_{\mathrm{n}}} u_{\mathrm{L}} \mathrm{d}t \tag{13}$$

where N is the number of winding turns and A is the cross-section area of the inductor core. $i_{\mathrm{L}}(t_{\mathrm{n}})$ is the inductor current at t_{n}, the magnetic field intensity $H(t_1)$ can be obtained by:

$$H(t_{\mathrm{n}}) = \frac{N i_{\mathrm{L}}(t_1)}{l} \tag{14}$$

where l is the length of the equivalent magnetic circuit. The hysteresis loss P_{hysis} can be calculated as:

$$P_{\mathrm{hysis}} = \frac{1}{T_{\mathrm{gird}}} \sum_{n=1}^{N_{\mathrm{s}}} \int_{B_{\mathrm{S}}}^{B_{\mathrm{P}}} H dB - \int_{B_{\mathrm{P}}}^{B_{\mathrm{E}}} H dB \tag{15}$$

3.5. Capacitor Loss

The loss which is caused by the leakage current of the capacitor P_{cleak} can be calculated as:

$$P_{\mathrm{cleak}} = U_{\mathrm{c}} \cdot I_{\mathrm{cleak}} \tag{16}$$

U_{c} is the voltage on the capacitor, and I_{cleak} is the leakage current of the capacitor, which is a U_{c} related parameter and can be found in the datasheet.

R_{cs} is the resistance of the capacitor lead and electrode, I_{rip} is the ripple current of the capacitor, and the loss on these conductors can be represented as:

$$P_{\mathrm{cs}} = I_{\mathrm{rip}}^2 R_{\mathrm{cs}} \tag{17}$$

R_{ESR} is the equivalent series resistance of the capacitor, which can be deduced form dissipation factor tanδ:

$$R_{\mathrm{ESR}} = \frac{\tan \delta}{2\pi f C} \tag{18}$$

where f is the frequency which the ESR is calculated at. C is the capacitance of the capacitor. The ESR loss of the capacitor can be calculated as:

$$P_{\mathrm{ESR}} = I_{\mathrm{rip}}^2 R_{\mathrm{ESR}} \tag{19}$$

The total losses on the capacitor is

$$P_{\mathrm{closs}} = P_{\mathrm{cleak}} + P_{cs} + P_{\mathrm{ESR}} \tag{20}$$

3.6. Loss Calculation Results

Based on the previous methods, the calculation results of the Full SiC power devices inverter losses are shown in Figure 7 as calculation Example 1.

As we can see from Figure 7, the switching loss takes the major part of the total loss. The output capacitance loss P_{OSS}, which is often overlooked in low frequency loss analysis, is over 1% and should be taken account in high frequency application. For the special characteristic of the SiC diode, the reverse recovery time t_{rr} is consider to be 0. Hence, the free-wheeling diode turn-off loss P_{doff} is 0. This superiority, which is proven in later experiment, is vital for the total loss of the inverter. Finally, the calculation efficiency is 97.32% at rated power of 1 kW.

Two comparative calculation examples are set up. In Example 2, the free-wheeling diodes D_1, D_2 are replaced by two normal Si diodes. In Example 3, all the power devices are replaced by the normal Si devices. The loss distribution of the comparative calculation examples are shown in Figure 8.

As Figure 8a shows, when the SiC diodes are replace by the normal Si diodes, the total loss on the diodes is over 50%. The turn-on loss and the turn-off loss of the diodes contribute the most part of the losses increase. As a result, the calculation efficiency of Example 2 is down to 93.57% at 1 kW.

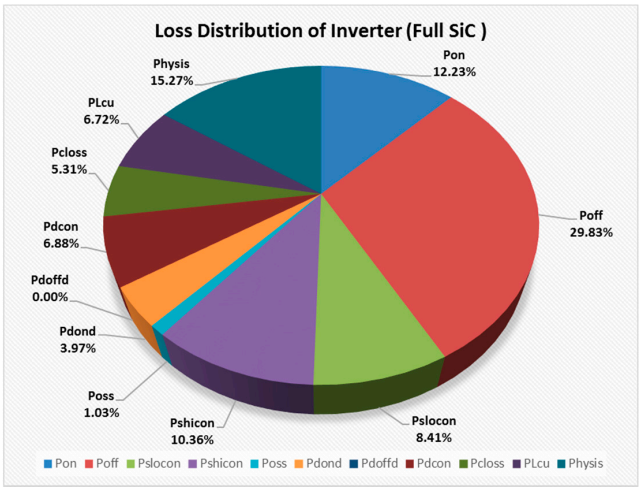
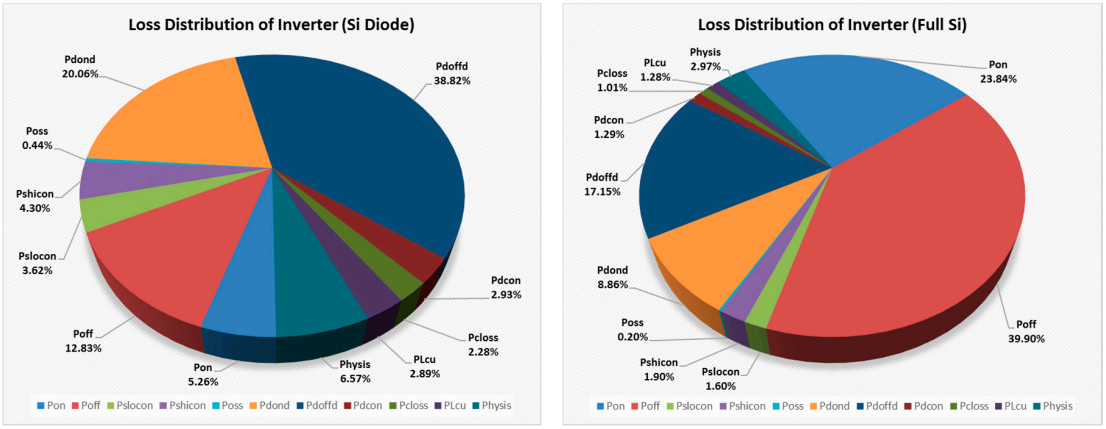


Figure 7. Loss distribution of Example 1.



(**a**) (**b**)

Figure 8. Loss distributions of the comparative calculation examples: (**a**) Example 2; and (**b**) Example 3.

After all the power devices are replaced by the Si devices. The losses of the switches become the major part of the total losses. Consequently, as Figure 8 shows, the total loss of Example 3 is almost three times larger than Example 2. The calculation efficiency of Example 3 is 85.27% at 1 kW.

The total loss comparison is shown in Figure 9. For Example 2, the diode losses contribute the most. For Example 3, the losses on the switches are numerous. The total losses difference between the Full SiC and Full Si power device is over five times. These results are confirmed in later comparative experiments, which indicate that the Si power devices are not suitable for high frequency application.

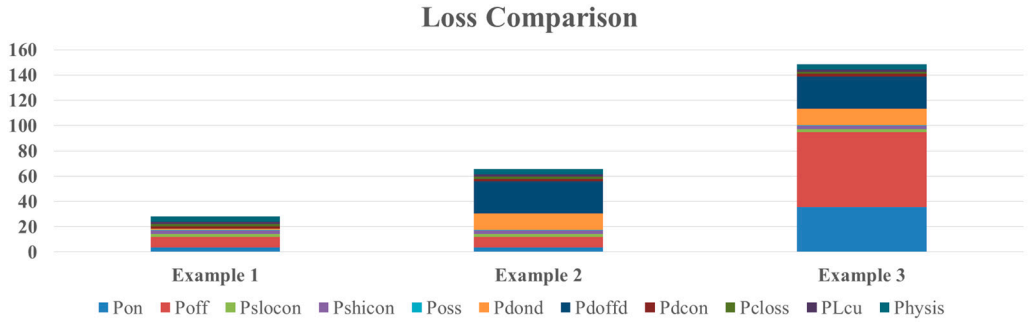


Figure 9. Loss comparison between calculation examples.

4. Improved Simulation Method

A simulation model is often built in software environment in order to verify the validity of theoretical analyses and accelerate the compensator tuning. In low frequency converting, the simplified component models are considered to be effective and timesaving. However, as the switching frequency increases, some details of the switching procedure may have a serious influence on the simulation, which could make the results become inaccurate, even unreliable. The inconsistency between the simulation results and experiment results emerges during the design process. The deviation between PWM control signal and switching response in high frequency switching is consider to be the reason which cause the inconsistency. The influence of the deviation on the simulation is verified by experiment. Moreover, based on the theoretical analysis and test results, a compensator method is proposed in order to minimize the deviation which is caused by the influence. Consequently, the simulation results are significantly improved. The improved simulation model is used in prototype design to verify the compensators. The method is proven to be effective by the experiments in later section.

4.1. Influence of High Frequency Switching

A simulation model is built in software environment of PSIM. The parameters of the components and control compensator are the same as the experimental prototype. The grid-connecting power experiments are carried out. The 3P3Z compensator in the current loop, which is designed to follow the current reference, are tuned and tested on the simulation model. As Figure 10a shows, the compensation effect is desirable. However, during the experiment, the same compensator, which has the same parameters, causes the current oscillation during zero-crossing procedure.

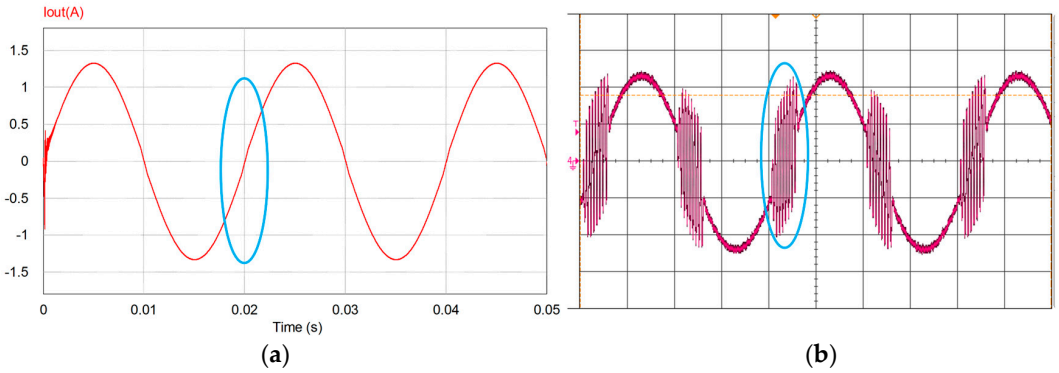


Figure 10. Simulation and Experiment results comparison: (**a**) simulation waveform before improving; and (**b**) experiment waveform.

The same simulation method is used in the previous 50 kHz inverter design and no similar issue arises. Through analysis, the deviation between PWM control signal and switching response in high frequency switching, is the main reason which causes the simulation to be inaccurate.

4.2. Equivalent Opening Time

Figure 11 shows the waveforms of a complete switching cycle. The PWM signal is considered to be an ideal square wave. When the rising edge of the PWM signal begins to turn on the switch, there is a turn-on propagation delay t_{pg_on} before the G-S voltage starts to rise. The delay is caused by the drive circuits when converting the PWM signal into drive signal. When V_{GS} rises, the D-S voltage V_{DS} starts to descend. The time, which is from 10% V_{GS} to 90% V_{DS}, is defined as the turn-on delay t_{d_on}. The time, which is form 90% V_{DS} to 10% V_{DS}, is the rise time t_{rise}. The turn-off propagation delay t_{pg_off}, turn-off delay t_{doff} and fall time t_{fall} can be obtained by similar definitions. The equivalent opening time is define as the period which the V_{DS} fall below 90% then rise over 90%. As Figure 11

shows, the relationship between PWM opening time t_{PMW} and the equivalent opening time t_{EQ} can be represented as Eqaution (21)

$$t_{EQ} = t_{PWM} + [t_{pg\_off} - t_{pg\_on}] + [t_{d\_off}(V_{DS}) - t_{d\_on}(V_{DS})] + t_{rise}(V_{DS}) + t_{fall}(V_{DS}) \quad (21)$$

The equivalent opening time t_{EQ} can be regarded as the actual respond of the switch under the control of PWM signal. In practical circuits, t_{pg_on} and t_{pg_off} are small and assumed to be equal. Hence, Equation (21) can be simplified as:

$$t_{EQ} = t_{PWM} + t_{d\_off}(V_{DS}) - t_{d\_on}(V_{DS}) + t_{rise}(V_{DS}) + t_{fall}(V_{DS}) = t_{PWM} + t_e(V_{DS}) \quad (22)$$

where t_e is the total extend time which is caused by the delay in the switching procedure. t_{d_on}, t_{d_off}, t_{fall} and t_{rise} are all V_{DS} related parameters provided by the datasheet. It is obvious that the PWM opening time is extended during the switching procedure. The proportions of the deviation in the equivalent opening time t_{EQ} under different switching frequencies and duty cycles are shown in Table 1.

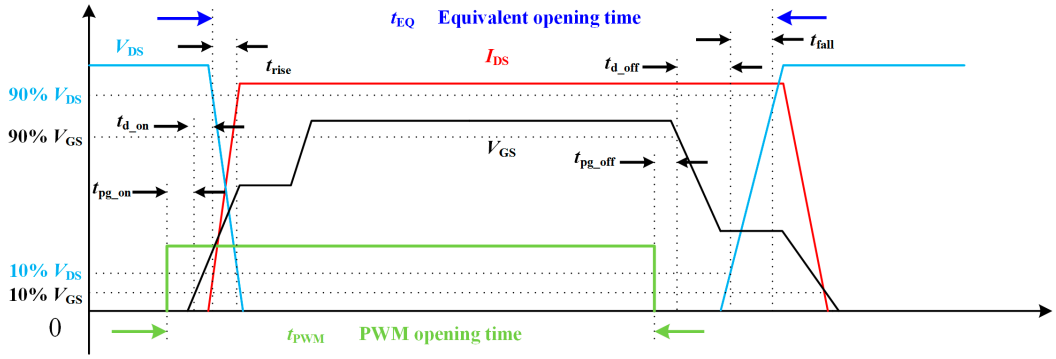


Figure 11. Waveforms of the switching operation.

Table 1. The proportion of the deviation.

t_e	f_{sw}	Duty Cycle	$t_{PWM(ns)}$	$t_{EQ(ns)}$	t_e/t_{EQ}
92 ns	50 kHz	2%	400	492	18.70%
		50%	10,000	10,092	0.91%
		80%	16,000	16,092	0.57%
	400 kHz	2%	50	142	64.79%
		50%	1250	1342	6.86%
		80%	2000	2092	4.40%

As Table 1 shows, when the switching frequency is low, the proportion of t_e in t_{EQ} is very small. During the practical circuit design, this deviation is often ignored. However, in high frequency implementation, this time deviation may even larger than t_{PWM}. When the f_{sw} is at 400 kHz, at 2% duty cycle, the proportion of t_e is over 50%. t_{PWM} is extended about two times. This deviation may lead to the inconsistency between the output and control signal. This difference has an error accumulation effect, which can cause the error response of the controller. As a result, the compensator, which is tested in the simulation and consider to be valid, will fail on the prototype.

In order to verify the analysis, an off-grid DC experiment is set up, for the deviation is more obvious when the duty cycle is constant. The difference between the output currents can prove the pervious analysis. The prototype connects to a 100 Ω resistor instead of the gird, then runs at 50 kHz and 400 kHz respectively. A constant duty cycle is given to the inverter in order to run the inverter in DC output mode. The output current i_{test} is tested at each duty cycle at different switching

frequency. Meanwhile, the same test is carried out on the simulation model. As Figure 12 shows, the output current at the same duty cycle of simulation and experiment are represented by two respective curves. There is almost no difference between the experiment results and simulation results when the switching frequency is at 50 kHz as Figure 12a shows. Because the proportion of the deviation in low frequency is very small, which can be ignored in traditional analysis. However, when the switching frequency is at 400 kHz as Figure 12b shows, there are significant differences between the simulation results and the experiment results. When the test duty cycle is under 45%, the experiment output current is apparently larger than the simulation results at the same duty cycle. This phenomenon can be explained as the control PWM signal in the prototype is extended by the delays which we talked above. The phenomenon is more obvious at low duty cycle which is consistent with previous analysis.

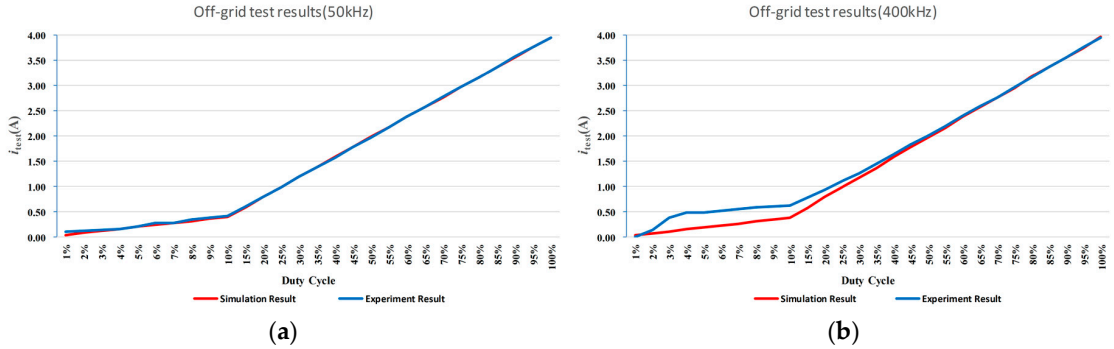


Figure 12. The output current responds between simulation and experiment at different frequencies: (**a**) 50 kHz; and (**b**) 400 kHz.

4.3. Compensating Method

Different from other researches, the proposed method focuses on the impact of the switching procedure on the output power. Instead of simulating the complex switching procedure in detail, a compensating module is used to improve the simulation results. The proposed method is simple and effective. Based on Equation (22), d_{EQ} is the duty cycle based on t_{EQ} and can be calculated as:

$$d_{EQ} = \frac{d \cdot t_{sw} + t_{d\_off}(V_{DS}) - t_{d\_on}(V_{DS}) + t_{rise}(V_{DS}) + t_{fall}(V_{DS})}{t_{sw}} \quad (23)$$

where t_{sw} is the switching period, and d_{PWM} is the duty cycle of the input PWM. The compensator is added between the Linearization module and PWM generating module (Figure 13).

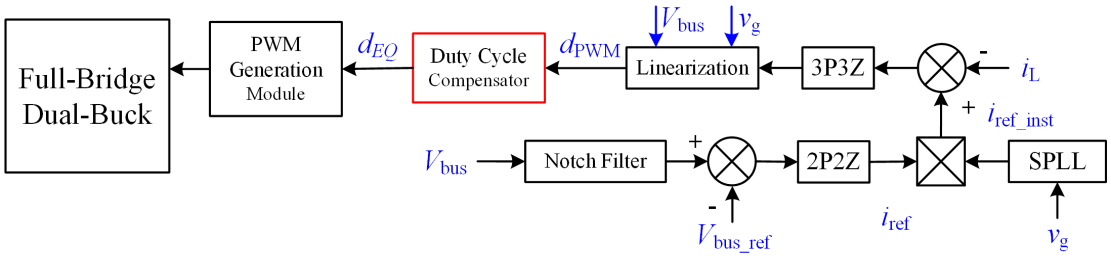


Figure 13. Location of the compensator.

The linearization module [24–26] is used to generate the duty cycle d_{PWM} for controlling the switches. The duty cycle d_{PWM} is compensated by the duty cycle compensator. In order to test the compensation effect, the 400 kHz off-grid DC experiment is carried out on the improved simulation model. The simulation results are shown in Figure 14. Apparently, the compensator module is able

to simulate the prototype output current correctly. The deviation of the output current between the simulation and experiment is minimized successfully.

Because of the deviation, the characteristic of compensator at low duty cycle have to be adjusted. Based on the improved simulation model, the characteristic of the inverter is re-analyzed. The compensator is redesign accordingly. The oscillation during zero-crossing is restrained by the new compensator in the simulation. The compensation effect is proven by the further experiment. The output waveforms of the experiments are shown in the later section.

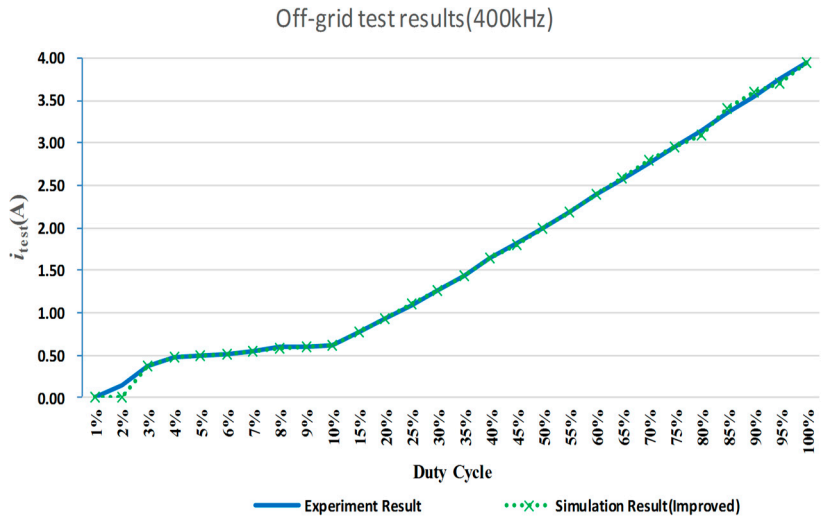


Figure 14. The current respond between improved simulation and experiment.

5. Experiment Results

A 1-kW prototype is built in the laboratory (Figure 15). The parameters of the components are shown in Table 2. The control platform is TMS320F28377D from Texas Instruments. It is a high performance dual-core MCU running at 200 MHz.

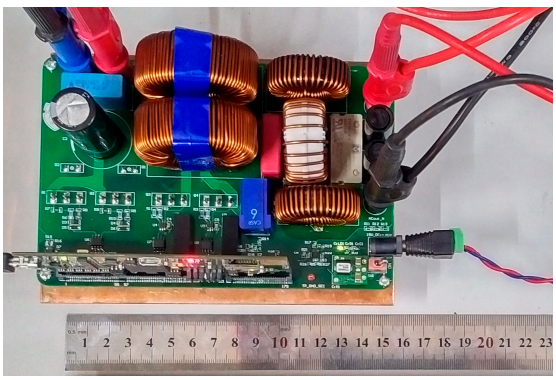


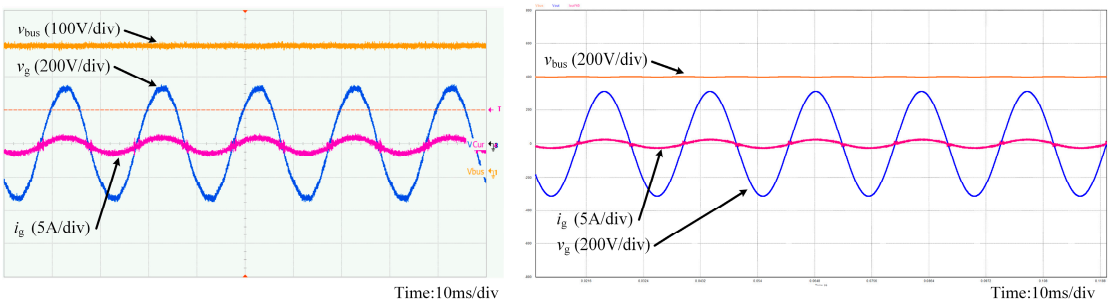
Figure 15. Experimental prototype.

Table 2. Parameters of the proposed system.

Component	Manufacture	Model	Value
S_1, S_2, S_3, S_4	Wolfspeed	C2M0280120D	
D_1, D_2	Wolfspeed	CVFD20065A	
L_{i1}, L_{i2}	Magnetics	77439A7	800 μH
L_{g1}, L_{g2}	Magnetics	77548A7	215 μH
C_f	WIMA	MKP10	0.15 μF

5.1. Grid-Connected Experiment

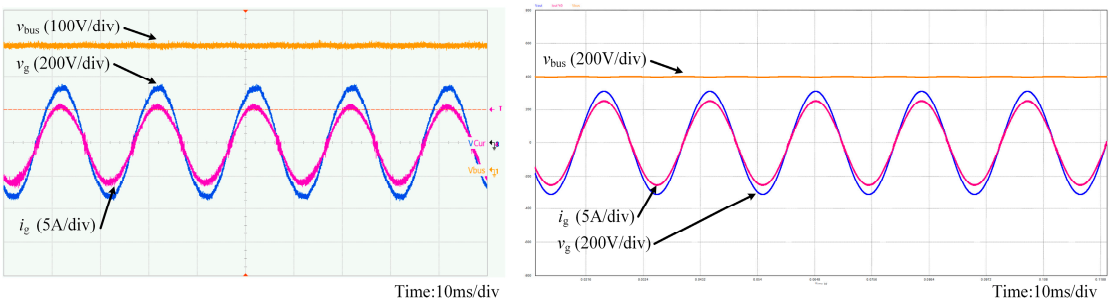
Figure 16a shows the measured waveforms at 100 W and Figure 16b is the corresponding simulation waveforms. The output current i_g can track the grid voltage very well when the power output is low. The power factor is 0.99 and THD is 4.8%. The bus voltage is stabilized at 400 V and the ripple is within ±4 V. The zero-crossing oscillation which happens in pervious compensator design is efficiently restrained. The simulation waveforms in Figure 16b match the experiment results well.



(**a**) (**b**)

Figure 16. Experimental waveforms of the inverter at low power: (**a**) experiment waveform; and (**b**) simulation waveform.

Figure 17a shows the waveform at 1 kW and Figure 17b is the corresponding simulation waveforms. The RMS value of i_g is 4.5 A. Along with the increase of the output power, the waveform of the i_g rises significantly. The power factor is 0.99 and THD is down to 1.8%. The efficiency of the inverter is 96.1% at this moment.



(**a**) (**b**)

Figure 17. Experimental waveforms of the inverter at rated power: (**a**) experiment waveform; and (**b**) simulation waveform.

Figure 18a shows the waveforms of the switch voltage and grid current at rated power of 1 kW. Figure 18b is the partial enlarged waveform of Figure 18a. i_g is the grid current. v_{DS} is the drain-to-source voltage of the switch S_1. v_{GS} is the drive signal of S_1. As the waveform shows, when i_g is above zero, S_1 is switched at high frequency of 400 kHz. The voltage stress of S_1 is 400 V; when i_g is below zero, S_1 is closed.

The relationships between efficiency, THD versus the output power are shown in Figure 19a,b, respectively. The THD decreases from 4.8% to 1.8% when the output power grows from 100 W to 1000 W, while the efficiency increases from 85.2% to 96.1%. Finally, the efficiency reaches the maximum efficiency of 96.1% at rated power. Thus, in small renewable energy application, the proposed inverter achieves an excellent performance, including relatively high conversion efficiency, high power factor and low THD.

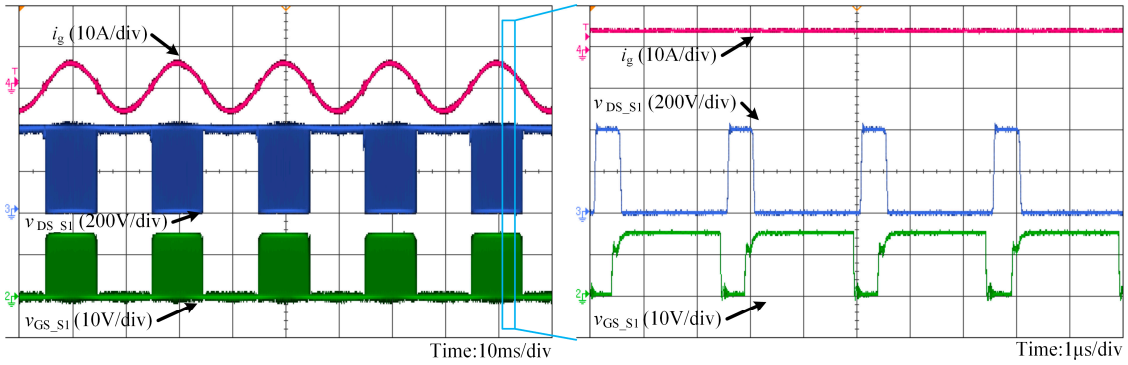


Figure 18. Experimental waveforms: (**a**) Waveform of the switch voltage and grid current at rated power; and (**b**) partial enlarged waveform of the switch voltage and grid current.

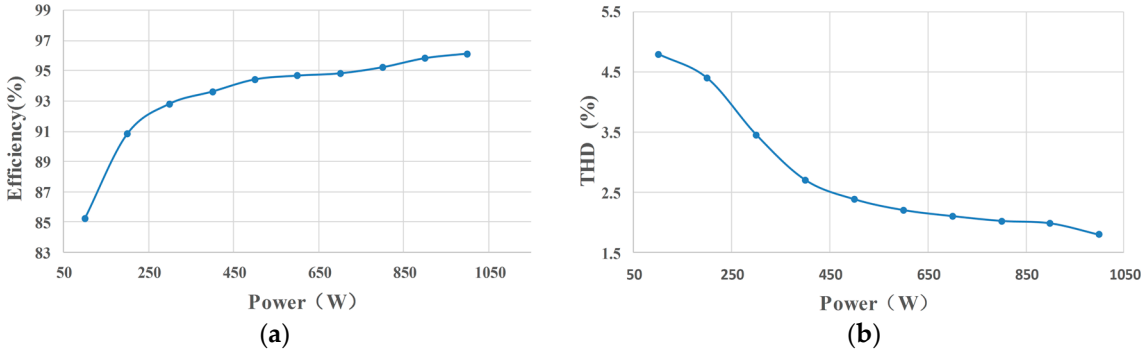


Figure 19. Efficiency and grid current THD curves: (**a**) efficiency under different power level; and (**b**) THD under different power level.

5.2. Comparison Experiments of Power Loss

The comparative experiments are set up in order to verify the loss analyses in Section 3. The power devices of Prototype 1 are all SiC power devices. The free-wheeling diodes D_1 and D_2 are replaced by normal Si diodes on Prototype 2. All the power devices are replaced by normal Si devices on Prototype 3. The power devices used in each Prototype are shown in Table 3.

Table 3. Power Devices of the Prototype.

Prototype	D_1, D_2	S_1–S_4
1	CVFD20065A	C2M0280120D
2	BYV29-600	C2M0280120D
3	BYV29-600	IPW60R040C7

The efficiency curves of the comparison experiments are shown in Figure 20. Prototype 1, which uses power devices that are full SiC components, reaches the rated power at 1 kW. When the temperature of the components is stable, the efficiency of Prototype 1 is 96.1%. Prototype 2, in which the diodes are replaced with Si diodes, reaches the rated power of 1 kW. However, the Si diodes break down within one minute. The efficiency of Prototype 2 at 1 kW is 91.83%. The voltage v_{diode} and current i_{diode} waveforms of the free-wheeling diode D_1 at 150 W in Prototype 1 and 2 are compared in Figure 21. Prototype 3 has the highest efficiency when the output power is low because the Si power devices used in the experiment have a lower conduction loss than the SiC. When the output power rises, Prototype 3 reaches the highest efficiency of 88.9% at 500 W. Then, the efficiency of Prototype 3

starts to decrease and the Si switches break down at 600 W. The efficiency of Prototype 3 at 1 kW cannot be measured. The experiment proves that the Si power devices are not suitable for high switching frequency application.

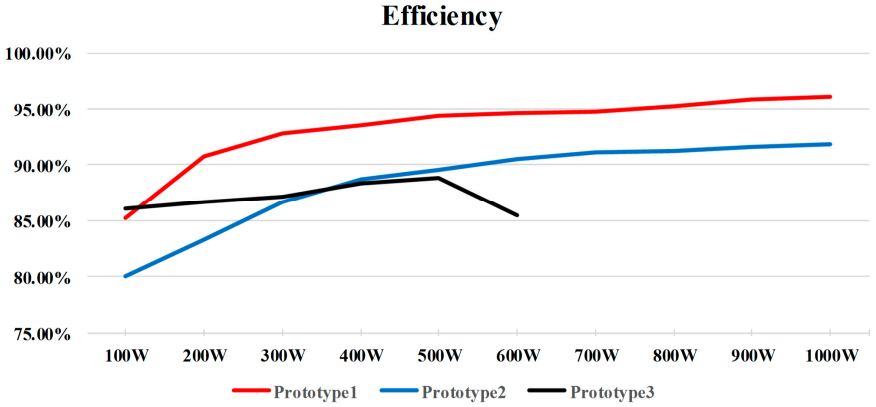


Figure 20. Efficiency comparison.

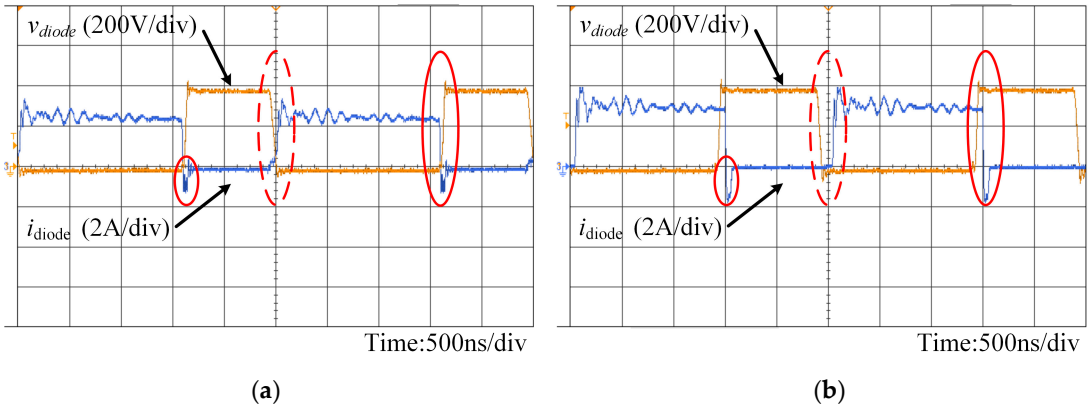


Figure 21. Voltage and current waveforms of the free-wheeling diode D_1: (**a**) switching transition of SiC diode; and (**b**) switching transition of Si diode.

As Figure 21b shows, during the turn-on and turn-off procedure, the voltage and current of the Si diode in Prototype 2 have a large overlap area and big reverse recovery current, which means the switching losses of the diodes are very large. Comparing with the Si diode (Figure 21a), the SiC diode has a faster switching speed, which contributes to a low switching loss. Remarkably, the reverse recovery current of the SiC diode is not zero in the measured high frequency waveforms, but the reverse recovery loss is significantly smaller than Si diode due to the extremely short reverse recovery time.

The comparisons of experiment and calculation efficiencies are shown in Table 4. For prototype 1, the calculation efficiency at 1 kW is 97.32% and the corresponding experiment efficiency is 96.1%. The deviation between experiment and calculation is 1.02% which may be caused by the unmeasured losses such as the losses on the relay, fuse and so on. The calculation efficiency of Prototype 2 is 93.57% and the experiment efficiency at 1 kW is 91.83%. The deviation of Prototype 2 is 1.74%. Because the efficiency experiment of Prototype 2 does not reach a temperature stable state before the Si diodes breaks down, the unstable state of the main circuit may cause extra loss in Prototype 2. Prototype 3 cannot reach the rated power and breaks down at 600 W during the experiment; its efficiency is 88.9% at 500 W. Finally, the deviation between experiment and calculation efficiency is within acceptable range, which proves that the proposed loss calculation methodology is valid.

Table 4. Experiment and calculation efficiency.

Prototype	Calculation Efficiency (1 kW)	Experiment Efficiency (1 kW)	Deviation
1	97.32%	96.1%	1.22%
2	93.57%	91.83%	1.74%
3	85.27%	88.9% (at 500 W)	Unknown

6. Conclusions

A 400 kHz dual-buck full-bridge inverter is proposed for small power renewable energy gird-connected generation. A current voltage dual-loop control strategy is employed, including a 3P3Z compensator in the inner current loop and a 2P2Z compensator in the outer voltage loop. Consequently, the inverter can deliver grid-tie power and regulate the DC bus voltage simultaneously. A systematic method for calculating the losses of high frequency inverter is presented. The influences of high frequency switching on loss analysis are discussed in detail. The loss distribution of the proposed inverter is obtained through the presented method. The simulation error, which is cause by the deviation between PWM control signal and switching response, is thoroughly analyzed. An improved simulation method is proposed in order to minimize the deviation which is caused by the delays of the switch in high frequency switching procedure. The loss analysis and simulation method are both validated by corresponding experiments. Finally, the power experiment of the inverter is finished at rated power of 1 kW, with the power factor above 0.99 and THD of 1.8%. The adoption of SiC power devices contributes to the highest efficiency of 96.1% at rated power. The experiment results prove that the proposed loss calculation method and improved simulation method is effective and suitable for high frequency inverter.

Acknowledgments: This research was supported by the National Natural Science Foundation of China (Grant: 2015AA050603) and supported by Tianjin Municipal Science and Technology Commission (Grant: 14ZCZDGX00035). The authors would also like to thank the anonymous reviewers for their valuable comments and suggestions to improve the quality of the paper.

Author Contributions: Zhun Meng and Yi-Feng Wang designed the main parts of the study. Liang Yang and Wei Li helped in the fabrication.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Pinto, R.; Mariano, S.; Calado, M.; Souza, J.D. Impact of Rural Grid-Connected Photovoltaic Generation Systems on Power Quality. *Energies* **2016**, *9*, 739. [CrossRef]
2. Orioli, A.; Franzitta, V.; Gangi, A.D.; Foresta, F. The Recent Change in the Italian Policies for Photovoltaics: Effects on the Energy Demand Coverage of Grid-Connected PV Systems Installed in Urban Contexts. *Energies* **2016**, *9*, 944. [CrossRef]
3. Faranda, R.S.; Hafezi, H.; Leva, S.; Mussetta, M.; Ogliari, E. The optimum PV plant for a given solar DC/AC converter. *Energies* **2015**, *8*, 4853–4870. [CrossRef]
4. Han, Y.; Chen, W.; Li, Q. Energy Management Strategy Based on Multiple Operating States for a Photovoltaic/Fuel Cell/Energy Storage DC Microgrid. *Energies* **2017**, *10*, 136. [CrossRef]
5. Holtz, J.; Holtgen, M.; Krah, J.O. A Space Vector Modulator for the High-Switching Frequency Control of Three-Level SiC Inverters. *IEEE Trans. Power Electron.* **2014**, *29*, 2618–2626. [CrossRef]
6. Gurpinar, E.; Castellazzi, A. A Single-Phase T-Type Inverter Performance Benchmark Using Si IGBTs, SiC MOSFETs, and GaN HEMTs. *IEEE Trans. Power Electron.* **2015**, *31*, 7148–7160. [CrossRef]
7. Zhou, Y.; Huang, W.; Hong, F.; Wang, C. Modelling analysis and power loss of coupled-inductor single-stage boost inverter based grid-connected photovoltaic power system. *IET Power Electron.* **2016**, *9*, 1664–1674. [CrossRef]

8. Wang, X.; Jiang, C.; Lei, B.; Teng, H. Power-Loss Analysis and Efficiency Maximization of a Silicon-Carbide MOSFET-Based Three-Phase 10-kW Bidirectional EV Charger Using Variable-DC-Bus Control. *IEEE J. Emerg. Sel. Top. Power Electron.* **2016**, *4*, 880–892. [CrossRef]
9. Fatemi, A.; Azizi, M.; Mohamadian, M.; Varjani, A.Y. Single-Phase Dual-Output Inverters with Three-Switch Legs. *IEEE Trans. Ind. Electron.* **2013**, *60*, 1769–1779. [CrossRef]
10. Shammas, N.; Chamund, D.; Taylor, P. Forward and reverse recovery behavior of diodes in power converter applications. In Proceedings of the 24th International Conference on Microelectronics, Niš, Serbia, 16–19 May 2004; Volume 1, pp. 3–10.
11. Bonislawski, M.; Holub, M. Averaged inverter loss estimation algorithm. In Proceedings of the European Conference on Power Electronics and Applications, Karlsruhe, Germany, 5–9 September 2016; pp. 1–9.
12. Li, Y.; Ye, Z.; He, N.; Wu, J.; Hu, C.; Xu, D. Efficiency improvement of a SiC-MOSFET 500 kHz ZVS inverter. In Proceedings of the International Symposium on Power Electronics for Distributed Generation Systems, Vancouver, BC, Canada, 27–30 June 2016; pp. 1–8.
13. Swamy, M.M.; Kang, J.K.; Shirabe, K. Power Loss, System Efficiency, and Leakage Current Comparison between Si IGBT VFD and SiC FET VFD with Various Filtering Options. *IEEE Trans. Ind. Appl.* **2015**, *51*, 3858–3866. [CrossRef]
14. Matsumori, H.; Shimizu, T.; Takano, K.; Ishii, H. Evaluation of Iron Loss of AC Filter Inductor Used in Three-Phase PWM Inverters Based on an Iron Loss Analyzer. *IEEE Trans. Power Electron.* **2016**, *31*, 3080–3095. [CrossRef]
15. Tanimoto, Y.; Saito, A.; Matsuura, K.; Kikuchihara, H. Power-Loss Prediction of High-Voltage SiC-MOSFET, Circuits with Compact Model Including Carrier-Trap Influences. *IEEE Trans. Power Electron.* **2016**, *31*, 4509–4516. [CrossRef]
16. Wang, J.; Zhao, T.; Li, J.; Huang, A.Q. Characterization, Modeling, and Application of 10-kV SiC MOSFET. *IEEE Trans. Electron Devices* **2008**, *55*, 1798–1806. [CrossRef]
17. Chen, K.; Zhao, Z.; Yuan, L.; Lu, T. The Impact of Nonlinear Junction Capacitance on Switching Transient and Its Modeling for SiC MOSFET. *IEEE Trans. Electron Devices* **2015**, *62*, 333–338. [CrossRef]
18. Miyake, M.; Ueno, M.; Feldmann, U.; Mattausch, H.J. Modelling of SiC IGBT Turn-Off Behavior Valid for Over 5-kV Circuit Simulation. *IEEE Trans. Electron Devices* **2013**, *60*, 622–629. [CrossRef]
19. Musumeci, S. Gate charge control of high-voltage Silicon-Carbide (SiC) MOSFET in power converter applications. In Proceedings of the International Conference on Clean Electrical Power, Taormina, Italy, 16–18 June 2015; pp. 709–715.
20. Wang, Z.; Shi, X.; Tolbert, L.M.; Wang, F.; Blalock, B.J. A di/dt Feedback-Based Active Gate Driver for Smart Switching and Fast Overcurrent Protection of IGBT Modules. *IEEE Trans. Power Electron.* **2014**, *29*, 3720–3732. [CrossRef]
21. Shimizu, T.; Ishii, K. An Iron Loss Calculating Method for AC Filter Inductors Used on PWM Inverters. In Proceedings of the Power Electronics Specialists Conference, Jeju, Korea, 18–22 June 2006; pp. 1–7.
22. Hong, F.; Liu, J.; Ji, B.; Zhou, Y. Single Inductor Dual Buck Full-Bridge Inverter. *IEEE Trans. Ind. Electron.* **2015**, *62*, 4869–4877. [CrossRef]
23. Zhang, N.; Tang, H.; Yao, C. A Systematic Method for Designing a PR Controller and Active Damping of the LCL Filter for Single-Phase Grid-Connected PV Inverters. *Energies* **2014**, *7*, 3934–3954. [CrossRef]
24. Bhardwaj, M.; Choudhury, S.; Xue, V.; Akin, B. Online LCL filter compensation using embedded FRA. In Proceedings of the IEEE Applied Power Electronics Conference and Exposition, Fort Worth, TX, USA, 16–20 March 2014; pp. 3186–3191.
25. Raushan, R.; Mahato, B.; Jana, K.C. Comprehensive analysis of a novel three-phase multilevel inverter with minimum number of switches. *IET Power Electron.* **2016**, *9*, 1600–1607. [CrossRef]
26. Ciobotaru, M.; Teodorescu, R.; Blaabjerg, F. A New Single-Phase PLL Structure Based on Second Order Generalized Integrator. In Proceedings of the 37th IEEE Power Electronics Specialists Conference, Jeju, Korea, 18–22 June 2006; pp. 1–6.