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Multiple inverters connected in parallel is a promising method to upgrade the power capacity of inductive power transfer (IPT) systems. Due to a slight unbalance of the control signals, the inner resistances of the inverters and other uncertainties, circulating currents exist among the parallel units which reduce the reliability of IPT systems. Firstly, the series-parallel resonant tank is employed in the multiple inverters based IPT system to eliminate the DC and harmonic circulating currents. The fundamental circulating currents in the paralleled inverter units are analyzed in detail. Then, for eliminating the fundamental circulating currents, a current decomposition method and a control diagram are proposed to avoid acquiring the phase of the current by detecting zero cross current point which increases the accuracy of the control algorithm. Finally, a 1-kW parallel-connected inverter IPT system is provided to verify the proposed approach. The experimental results show that the proposed method is effective for eliminating the fundamental circulating current phasor control (91.65%).

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Article Circulating Current Reduction Strategy for Parallel-Connected Inverters Based IPT Systems

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Abstract: Multiple inverters connected in parallel is a promising method to upgrade the power capacity of inductive power transfer (IPT) systems. Due to a slight unbalance of the control signals, the inner resistances of the inverters and other uncertainties, circulating currents exist among the parallel units which reduce the reliability of IPT systems. Firstly, the series-parallel resonant tank is employed in the multiple inverters based IPT system to eliminate the DC and harmonic circulating currents. The fundamental circulating currents in the paralleled inverter units are analyzed in detail. Then, for eliminating the fundamental circulating currents, a current decomposition method and a control diagram are proposed to avoid acquiring the phase of the current by detecting zero cross current point which increases the accuracy of the control algorithm. Finally, a 1-kW parallel-connected inverter IPT system is provided to verify the proposed approach. The experimental results show that the proposed method is effective for eliminating the fundamental circulating currents. The maximum efficiency of the system is up to 92.18% which is 0.53% higher compared to that without the current phasor control (91.65%).

Keywords: inductive power transfer (IPT); parallel-connected inverter; circulating currents; current phasor and voltage constant control

1. Introduction

Conventional inductive power transfer (IPT) systems, consisting of a DC power supply, a single high frequency inverter, a resonant compensation unit, loosely coupled coils and a secondary energy management unit, have been widely used in industrial high power applications [1–4] and charging systems for public electric vehicles [5–9]. The high frequency inverter converts the input DC voltage into a high frequency AC voltage for the primary coil. The high frequency AC energy can be transferred through loosely coupled coils. Then, the rectifier of the secondary side converts the received high frequency AC voltage into a DC voltage for the load. However, the single inverter feeding based IPT system mentioned above is normally designed to meet the demand of a fixed output power rating. The capability of the IPT system is sometimes decided by the capacity of the inverter. It should be noted that it is not easy to achieve high power transfer with a single inverter in the IPT system, due to the capacity and cost restriction of power switches [10,11]. Except the IPT system, the power extension is restricted by the switches in the other applications of the converters. The parallel connected method is a well-adapted solution, and used in many field, e.g., photovoltaic (PV) plants, DC-DC converters, inductive heating and so on [12–14]. However, there are few reports on the application of this parallel connected method in the field of IPT.

In order to meet the requirements of high-power applications, e.g., the power supplying for high-speed trains, the charging system for public vehicles [15–17], quite a few methods have been proposed to increase the capacity of IPT systems in the past decade. They can be roughly classified

into three categories: the cascaded method, the parallel connected method and the magnetic field enhancement method. For the cascaded method, an effective power improvement method based on the cascaded multi-level inverter technology has been discussed in [18]. The phase shift pulse width modulation method employed in the cascaded multi-level inverter to realize the power regulation and the selective harmonic elimination, simultaneously. Nevertheless, the modulation method of the control signal is some kind of complexities and the dynamic performance was not discussed. For the magnetic field enhancement method, a novel IPT topology based on dual coupled transmitters is proposed in [19,20]. By configuring the additional compensation capacitors, resonant inverters with different power ratings can be connected in parallel to achieve the high power transfer. However, it is difficult to choose the additional capacitors to let the inverter work under resonant condition and achieve power sharing due to the inevitable component tolerances. For the parallel connected method, a straightforward method of improving the power levels is that employing the parallel-connected inverter topology for feeding IPT systems [10,21]. A power regulation and selective harmonic current elimination approach of parallel-connected inverter is proposed in [21] for supplying IPT systems, which not only can upgrade the capacity of the power supply, but also can suppress the total harmonic distortion (THD) of the primary coil current. Unfortunately, the inevitable circulating current issue caused by the component tolerance has not been discussed in detail.

Circulating currents can not only damage the power electronic devices and lower the efficiency of the system by introducing some unnecessary currents. In addition, they can even reduce the reliability of the system by imposing too much current stress on the semiconductor devices. The circulating current usually consists of DC circulating component, harmonic circulating component and fundamental circulating component. An unneglectable DC circulating current between the inverters caused by a slight unbalance of the control signals, the inner resistances of the inverters and the speed difference of the switching drivers [22]. The harmonic circulating current [23] should be considered in the parallel-connected inverter IPT system, due to the high THD of the inverter output voltage [10] and the tolerance of circulating current exists between the parallel inverter units [21] due to the unbalance of parallel connected inverters, such as the gate pulse delay, the pulse width modulator randomness and the control delay. As a result, the electric and thermal stresses are unbalanced between the parallel inverters [24,25], and it will increase the potential damage to the IPT system. Hence, it is necessary to investigate an approach to reduce the circulating current in the parallel-connected inverter IPT system.

It is an effective approach for eliminating the DC and harmonic circulating currents between the parallel units by adding the series-parallel resonant tank proposed in [11] rather than with complex control methods [22,23]. For the fundamental circulating currents, a phasor control method is proposed in [11] with the function of eliminating the fundamental circulating currents. Nevertheless, the proposed circulating current elimination method needs phase locking loop (PLL) circuits to track the phase of the bus voltage to calculate the active and reactive current components [11,26], which increases the computational burden and complexity of the control algorithm. Moreover, it is not easy to obtain the phase of the current accurately due to relatively high fundamental frequency. Usually, comparators are needed to acquire the phase of the current by detecting zero cross current point [27]. However, in practice, the current signal is not always reliable due to the distortion. As a consequence, the false synchronization pulse generated by the comparators can lead to the incorrect calculation of the current phase [28]. The fundamental circulating current problem is deliberately overcome by an active and reactive power decomposition method proposed in [17] without PLL. However, both the DC and harmonic circulating currents are not analyzed or minimized in [17]. An extra LC filter is needed to be added in the compensative circuit.

In order to overcome the aforementioned drawbacks, this paper applies a novel series-parallel tuned parallel-connected inverter IPT system to eliminate the DC and harmonic circulating currents without any control strategy which is proposed in [23]. In addition, the circulating current eliminating

strategy is analyzed in detail in Section 2. In order to eliminate the fundamental circulating current, this paper focuses on developing an active and reactive current decomposing approach without PLL and a phasor control method. With the current decomposing method, the high frequency AC signals can be transformed to DC signals for the phasor controllers, which decreases the computational burden and complexity of the control algorithm. It provides convenience for the power extension through the coordination between the multiple resonant inverter units and the current decomposing circuits which reduces the manufacturing cost.

This paper is organized as follows. Section 2 presents the principle description of the parallel-connected inverter topology. Section 3 analyses the causes of the fundamental circulating currents in the inverter units. A current decomposition method and a control diagram are proposed in Section 4. The experimental results from a 1-kW parallel-connected inverter IPT system are provided in Section 5 to verify the validity of the circulating current reducing and constant voltage control approaches. Finally, this paper is concluded in Section 6.

2. Principle Description of the Parallel-Connected Inverter Topology

The schematic of the IPT system based on the parallel-connected inverter with the series-parallel resonant tank is shown in Figure 1, which consists of *n* identical inverter units with the same operating frequency ω . For tuning purposes, the series-parallel resonant tank (L_{ak} , C_{ak} , L_{bk} and C_{bk}) for the *k*th parallel unit should satisfy:

$$\omega = \frac{1}{\sqrt{L_{ak}C_{ak}}} = \frac{1}{\sqrt{L_{bk}C_{bk}}} \qquad (k = 1, 2, 3 \cdots n)$$
(1)



Figure 1. The inductive power transfer (IPT) system based on parallel-connected inverter with the series-parallel resonant tank.

The *k*th parallel unit is connected in series with a connection inductor L_{ek} , which is used to suppress the circulating current in the parallel-connected inverter IPT system. The value of L_{ek} is very small, so that the voltage drop and power losses over the resistance of connection inductors can be neglected [29]. The compensation capacitor C_P is connected in series with the primary coil L_P . The secondary circuit is consisted of the secondary coil L_S , the compensation capacitor C_S , the rectifier and the load R_L . For tuning purposes, L_P , C_P , L_S and C_S are all designed at the resonant frequency:

$$\omega = \frac{1}{\sqrt{L_{\rm P}C_{\rm P}}} = \frac{1}{\sqrt{L_{\rm S}C_{\rm S}}} \tag{2}$$

Without loss of generality, we take the parallel three-inverter based IPT system as an example, and three cases will be discussed in this section. According to [30], the reflected resistance of the secondary circuit is given as:

$$R_{\rm r} = \frac{\omega^2 \pi^2 M^2}{8R_{\rm L}} \tag{3}$$

Firstly, the parallel three-inverter IPT system without the series-parallel resonant tank has been discussed in [21] and the equivalent circuit is shown in Figure 2.



Figure 2. The equivalent circuit of the IPT system without the series-parallel resonant tank.

By employing the phase-shift control technology in the parallel-connected inverter IPT system [10], the output voltage waveforms are shown in Figure 3. The fundamental magnitude of the inverter output voltage ($u_1(1)$, $u_2(1)$ and $u_3(1)$) can be regulated by changing the conduction angle θ_L varied from 0° to 180° as shown in Equation (4):

$$\begin{aligned} u_{1} &= \frac{E_{1H} - E_{1L}}{2} + \sum_{k=1}^{\infty} \left[\frac{2(E_{1H} + E_{1L})}{k\pi} \cos(\frac{k\theta_{L1}}{2}) \sin(k\omega t) \right] \\ u_{2} &= \frac{E_{2H} - E_{2L}}{2} + \sum_{k=1}^{\infty} \left[\frac{2(E_{2H} + E_{2L})}{k\pi} \cos(\frac{k\theta_{L2}}{2}) \sin(k\omega t + k\theta_{\Delta 12}) \right] \\ u_{3} &= \frac{E_{3H} - E_{3L}}{2} + \sum_{k=1}^{\infty} \left[\frac{2(E_{3H} + E_{3L})}{k\pi} \cos(\frac{k\theta_{L3}}{2}) \sin(k\omega t + k\theta_{\Delta 13}) \right] \end{aligned}$$
(4)



Figure 3. The output voltage waveforms of parallel two inverters.

At the same time, the phase angle θ_{Δ} among the inverter 1, inverter 2 and inverter 3 can be altered accordingly. Due to the inner resistances of the inverters [22], the positive level of the inverter output voltage is not equal to the negative one ($E_{1H} \neq E_{1L}, E_{2H} \neq E_{2L}$ and $E_{3H} \neq E_{3L}$). Meanwhile, the conduction angle of the positive voltage level is not equal to the negative one ($\theta_{L1} \neq \theta_{L1}', \theta_{L2} \neq \theta_{L2}'$ and $\theta_{L3} \neq \theta_{L3}'$) due to a slight unbalance of the control signal and the speed of the switching drivers. Hence, there is a DC voltage offset in the inverter output voltage as shown in Figure 3. Meanwhile, by employing the phase shift control technology, the THD of the parallel inverter output voltage is high [10]. Therefore, the difference of the DC voltage offset Δu_{DC} , the difference of the fundamental voltage Δu_{Fun} , and the difference of the harmonic voltage Δu_{Har} can be derived by:

$$\Delta u_{\rm DC} = \frac{E_{\rm IH} - E_{\rm IL}}{2} - \frac{E_{\rm 2H} - E_{\rm 2L}}{2} - \frac{E_{\rm 3H} - E_{\rm 3L}}{2} = \frac{E_{\rm IH} + E_{\rm 2H} + E_{\rm 3H} - E_{\rm 1L} - E_{\rm 2L} - E_{\rm 3L}}{2} \Delta u_{\rm Fun} = \frac{2(E_{\rm IH} + E_{\rm 1L})}{\pi} \cos(\frac{\theta_{\rm L1}}{2}) \sin(\omega t) - \frac{2(E_{\rm 2H} + E_{\rm 2L})}{\pi} \cos(\frac{\theta_{\rm L2}}{2}) \sin(\omega t + \theta_{\Delta 12}) - \frac{2(E_{\rm 3H} + E_{\rm 3L})}{\pi} \cos(\frac{\theta_{\rm 13}}{2}) \sin(\omega t + \theta_{\Delta 13})$$
 $k = 3, 5, 7...$ (5)
$$\Delta u_{\rm Har} = \sum_{k=3}^{\infty} - \frac{\left[\frac{2(E_{\rm IH} + E_{\rm 1L})}{k\pi} \cos(\frac{k\theta_{\rm L3}}{2}) \sin(k\omega t) - \frac{2(E_{\rm 2H} + E_{\rm 2L})}{k\pi} \cos(\frac{k\theta_{\rm L3}}{2}) \sin(k\omega t + k\theta_{\Delta 13})\right]$$

Compared to the inductive reactance (L_{e1} , L_{e2} and L_{e3}), the resistance of the connection inductors (R_{Le1} , R_{Le2} and R_{Le3}) is much smaller, so that it can be neglected. Therefore, with a slight DC voltage offset difference there will be a huge DC circulating current between the parallel units [22]. Due to the tolerance of circuit parameters and the voltage difference mentioned in Equation (5), the fundamental circulating currents Δi_{Fun1} and Δi_{Fun2} , the harmonic circulating currents Δi_{Har1} and Δi_{Har2} between the parallel units also exist [23]. Three kinds of the circulating currents mentioned above, can be eliminated effectively by increasing the impedance of connection inductors (L_{e1} , L_{e2} and L_{e3}). Nevertheless, the connection inductors will be heavy and bulky, increasing the costs and volume, and soften the characteristic of the output voltage of the inverter [31,32].

Secondly, for the sake of eliminating the DC circulating currents Δi_{DC1} and Δi_{DC2} , a series resonant tank (L_{ak} and C_{ak}) is connected to each parallel unit branch in series, which can isolate the DC current effectively shown in Figure 4. For eliminating the harmonic circulating currents Δi_{Har1} and Δi_{Har2} , the quality factor of the series resonant tank, defined as the ratio of the impedance of the series resonant inductor to the equivalent resistor of the load [29], should be large enough. Nevertheless, the larger the quality factor of the series resonant tank is, the heavier the inductor will be. When the inductance of the series resonant tank is huge, it will be difficult to find a space to host it. Therefore, it is not a good choice to increase the quality factor of the series resonant tank to eliminate the harmonic circulating currents Δi_{Har1} and Δi_{Har2} for the parallel-connected inverter IPT system.



Figure 4. The equivalent circuit of the IPT system with the series resonant tank.

Thirdly, in order to eliminate the harmonic circulating currents Δi_{Har1} and Δi_{Har2} , a parallel resonant tank which can filter out the harmonic other than the fundamental component, added in the Figure 4 IPT system, as shown in Figure 1. With the series-parallel resonant tank added in the IPT system, the DC and harmonic circulating currents are eliminated effectively. To ensure that all the

switches of the inverter can achieve zero-voltage switching (ZVS), the series-parallel resonant tank is well designed. The resonant frequency of the series resonant tank is tuned to a little lower than the operating frequency. In addition, the resonant frequency of the parallel resonant tank is tuned to a little higher than the operating frequency [29]. The equivalent circuit of the IPT system is shown in Figure 5 and the output voltage sources of the parallel units can be expressed only by fundamental ones. Finally, only the fundamental circulating currents Δi_{Fun1} and Δi_{Fun2} are needed to be eliminated, and it will be analyzed specifically in the next section.



Figure 5. The equivalent circuit of the IPT system with the series-parallel resonant tank.

3. Analysis of the Fundamental Circulating Current

In practice, it is unlikely for the parallel unit to be identical. Generally speaking, the tolerance of the commercial inductor can be as high as 20%, and so is the capacitor [11]. For simplicity, assuming the series-parallel resonant tank is identical, only the tolerance of the connection inductors and the difference of the output inverter fundamental voltages are taken into consideration. According to Figure 5, based on the Kirchhoff's voltage and current laws (KVL and KCL), we have:

$$\begin{cases} \dot{U}_{1}(1) = j\omega\dot{I}_{P1}L_{e1} + (\dot{I}_{P1} + \dot{I}_{P2} + \dot{I}_{P3})(R_{r} + j\omega L_{P} + \frac{1}{j\omega C_{P}}) \\ \dot{U}_{2}(1) = j\omega\dot{I}_{P2}L_{e2} + (\dot{I}_{P1} + \dot{I}_{P2} + \dot{I}_{P3})(R_{r} + j\omega L_{P} + \frac{1}{j\omega C_{P}}) \\ \dot{U}_{3}(1) = j\omega\dot{I}_{P3}L_{e3} + (\dot{I}_{P1} + \dot{I}_{P2} + \dot{I}_{P3})(R_{r} + j\omega L_{P} + \frac{1}{j\omega C_{P}}) \\ 0 = j\omega L_{P} + \frac{1}{j\omega C_{P}} \end{cases}$$
(6)

The branch currents can be derived by:

$$\begin{pmatrix} \dot{I}_{P1} = \frac{R_{r}L_{e2}(\dot{u}_{1}(1) - \dot{u}_{3}(1)) + R_{r}L_{e3}(\dot{u}_{1}(1) - \dot{u}_{2}(1)) + j\omega L_{e2}L_{e3}\dot{u}_{1}(1)}{j\omega R_{r}(L_{e1}L_{e2} + L_{e2}L_{e3} + L_{e1}L_{e3}) - \omega^{2}L_{e1}L_{e2}L_{e3}} \\ \dot{I}_{P2} = \frac{R_{r}L_{e1}(\dot{u}_{2}(1) - \dot{u}_{3}(1)) + R_{r}L_{e3}(\dot{u}_{2}(1) - \dot{u}_{1}(1)) + j\omega L_{e1}L_{e3}\dot{u}_{2}(1)}{j\omega R_{r}(L_{e1}L_{e2} + L_{e2}L_{e3} + L_{e1}L_{e3}) - \omega^{2}L_{e1}L_{e2}L_{e3}} \\ \dot{I}_{P3} = \frac{R_{r}L_{e1}(\dot{u}_{3}(1) - \dot{u}_{2}(1)) + R_{r}L_{e2}(\dot{u}_{3}(1) - \dot{u}_{1}(1)) + j\omega L_{e1}L_{e2}\dot{u}_{3}(1)}{j\omega R_{r}(L_{e1}L_{e2} + L_{e2}L_{e3} + L_{e1}L_{e3}) - \omega^{2}L_{e1}L_{e2}L_{e3}}$$

$$(7)$$

For *n*-module inverter IPT system, the *k*th circulating current is defined to be half of the current difference of module currents between module k and (k + 1) according to [11]:

$$\Delta \dot{I}_{k} = \frac{\dot{I}_{Pk} - \dot{I}_{P(k+1)}}{2}$$
(8)

When *n* = 3, the circulating currents are ΔI_1 and ΔI_2 .

Case 1: according to Equations (7) and (8), let $L_{e1} = L_{e2} = L_{e3} = L_e$ and $\dot{U}_1(1) \neq \dot{U}_2(1) \neq \dot{U}_3(1)$, the equation of the circulating currents are given by:

$$\begin{cases} \Delta \dot{I}_{1} = \frac{\dot{I}_{P1} - \dot{I}_{P2}}{2} = \frac{\dot{U}_{1}(1) - \dot{U}_{2}(1)}{j2\omega L_{e}} \\ \Delta \dot{I}_{2} = \frac{\dot{I}_{P2} - \dot{I}_{P3}}{2} = \frac{\dot{U}_{2}(1) - \dot{U}_{3}(1)}{j2\omega L_{e}} \end{cases}$$
(9)

It can be concluded from Equation (9) that when $U_1(1) \neq U_2(1) \neq U_3(1)$, the circulating currents exist, $\Delta I_1 \neq 0$, $\Delta I_2 \neq 0$.

Case 2: according to Equations (7) and (8), let $L_{e1} \neq L_{e2} \neq L_{e3}$ and $\dot{U}_1(1) = \dot{U}_2(1) = \dot{U}_3(1) = \dot{U}(1)$, the equation of the circulating currents are derived as:

$$\begin{cases} \Delta \dot{I}_{1} = \frac{\dot{I}_{P1} - \dot{I}_{P2}}{2} = \frac{R_{r}L_{e3}\dot{U}(1)(L_{e1} - L_{e2})(L_{e1}L_{e2} + L_{e1}L_{e3} + L_{e2}L_{e3})}{2[jR_{r}(L_{e1}L_{e2} + L_{e1}L_{e3} + L_{e2}L_{e3}) - \omega L_{e1}L_{e2}L_{e3}]^{2}} \\ \Delta \dot{I}_{2} = \frac{\dot{I}_{P2} - \dot{I}_{P3}}{2} = \frac{R_{r}L_{e1}\dot{U}(1)(L_{e2} - L_{e3})(L_{e1}L_{e2} + L_{e1}L_{e3} + L_{e2}L_{e3})}{2[jR_{r}(L_{e1}L_{e2} + L_{e1}L_{e3} + L_{e2}L_{e3}) - \omega L_{e1}L_{e2}L_{e3}]^{2}} \end{cases}$$
(10)

According to Equation (10), we can get that when $L_{e1} \neq L_{e2} \neq L_{e3}$, the circulating currents exist too, $\Delta I_1 \neq 0$, $\Delta I_2 \neq 0$. From case 1 and case 2 analyzed above, we can draw a conclusion that the tolerance of the connection inductors or the difference of the output inverter fundamental voltages can cause the circulating currents. Without loss of generality, for the *n*-module inverter IPT system, the circulating currents exist, $\Delta I_1 \neq 0$, $\Delta I_2 \neq 0$, ... $\Delta I_{n-1} \neq 0$.

4. Analysis of a Current Decomposed Method and Control Diagram

4.1. Current Decomposition

In order to reduce the fundamental circulating current, phasor differences between branch currents should be controlled as small as possible. Therefore, a current phasor control strategy based on the current decomposing method is applied in the parallel-connected inverter IPT system. In order to obtain the phasor of each branch current, a novel decomposition method will be analyzed in detail in this section. With the current decomposing method analyzed in this section, the high frequency AC signals can be transformed to DC signals for the phasor controllers, which decreases the computational burden and complexity of the control algorithm. Here, we set the primary coil current as reference, and it can be defined as:

$$i_{\rm P} = I_{\rm Pm} \cos(\omega t) \tag{11}$$

where I_{Pm} is the magnitude of the primary coil current. By employing a phase lagging shift circuit, the orthogonal signal can be generated from the reference current i_P :

$$i_{\rm P}' = I_{\rm Pm} \sin(\omega t) \tag{12}$$

Hence, the orthogonal frame can be derived by:

$$\begin{cases} X_0 = i_{\rm P} = I_{\rm Pm} \cos(\omega t) \\ Y_0 = i_{\rm P}' = I_{\rm Pm} \sin(\omega t) \end{cases}$$
(13)

Herein, the branch current of each parallel unit is defined by:

$$i_{Pk} = I_{Pkm}\cos(\omega t + \phi_k) = i_{PkX}\cos(\omega t) + i_{PkY}\sin(\omega t)$$
(14)

where:

$$\begin{cases} i_{PkX} = I_{Pkm} \cos(\phi_k) \\ i_{PkY} = -I_{Pkm} \sin(\phi_k) \end{cases}$$
(15)

 i_{PkX} and i_{PkY} are the real component and imaginary component of the branch current as per reference current. The magnitude of the branch current i_{Pk} is I_{Pkm} , and the phase is ϕ_k , (k = 1, 2, ..., n). The productions of Equation (13) by the *k*th inverter unit current i_{Pk} can be expressed as:

$$\begin{cases} i_{Pk\cos} = I_{Pkm}\cos(\omega t + \phi_k)X_0 = I_{Pm}I_{Pkm}\cos(\omega t + \phi_k)\cos(\omega t) = \frac{I_{Pm}I_{Pkm}[\cos(2\omega t + \phi_k) + \cos(\phi_k)]}{2}\\ i_{Pk\sin} = I_{Pkm}\cos(\omega t + \phi_k)Y_0 = I_{Pm}I_{Pkm}\cos(\omega t + \phi_k)\sin(\omega t) = \frac{I_{Pm}I_{Pkm}[\sin(2\omega t + \phi_k) - \sin(\phi_k)]}{2} \end{cases}$$
(16)

It can be seen from Equation (16) that both $i_{Pk cos}$ and $i_{Pk sin}$ are composed of DC components and second-order harmonic components. By applying a Low-Pass Filter (LPF), the second-order harmonic components can be filtered out. Then, we can get the DC components:

$$\begin{cases} i_{PkX_Lf} = \frac{I_{Pm}I_{Pkm}\cos(\phi_k)}{2} \\ i_{PkY_Lf} = \frac{-I_{Pm}I_{Pkm}\sin(\phi_k)}{2} \end{cases}$$
(17)

With the magnitude of the primary coil current I_{Pm} , the *k*th inverter unit current i_{Pk} can be decomposed in the orthogonal frame, that is:

$$\begin{cases} i_{PkX} = 2i_{PkX_Lf} / I_{Pm} \\ i_{PkY} = 2i_{PkY_Lf} / I_{Pm} \end{cases}$$
(18)

According to Equations (14) and (18), the high frequency AC current signals have been transformed to DC current signals without PLL, which decreases the computational burden and complexity of the control algorithm. The decomposition circuit of *k*th inverter unit current i_{Pk} is shown in Figure 6.



Figure 6. The decomposition circuit of the *k*th inverter unit current i_{Pk} .

For example, let n = 3, the branch current of the parallel unit can be decomposed as shown in Figure 7. The coordinate shown in the Figure 7 consisted of X_0 and Y_0 is a rectangular system. To make the branch current i_{Pk} equal, the current decomposed components in the X_0 axis or in the Y_0 axis, respectively, should be regulated to be equal. Besides, the Y component separately for each of the converters needs to control to be zero according to Equations (17) and (18), when the phase ϕ_k is zero $(i_{P1X} = i_{P2X} = i_{P3X}, i_{P1Y} = i_{P2Y} = i_{P3Y} = 0)$. For *n*-module inverter IPT system, the number of the decomposition circuits shown in Figure 6 should be *n*. All of the branch currents should be regulated to be equal ($i_{P1X} = i_{P2X} = i_{P3X}... = i_{PnX}$, $i_{P1Y} = i_{P2Y} = i_{P3Y}... = i_{PnY} = 0$). As a result, the problem can be solved for any number of parallel connected inverters.



Figure 7. The decomposition of branch currents when n = 3.

The phase lagging shift prototype is used to generate the orthogonal signal as Equation (13) shows. The operational amplifier LM6142 is employed in this paper for the A_1 – A_5 shown in Figure 6. The phase difference between the input signal and the output signal (the lagging one) is set to be 90° by choosing the proper resistance R_1 and the capacitance C_1 in the phase lagging shift circuit, and the designed principle is $\omega R_1 C_1 = 1$. For eliminating the 5% tolerance in C_1 , the potentiometer R_1 which is adjustable is employed. The four quadrant analog multiplier MLT04 is employed to realize the multiplication of Equation (16). The butterworth low pass filter is designed to filter out the second-order harmonic components shown in Equation (16), and the cut off frequency of the filter is 80 Hz. It may take 20–30 periods to filter out the second-order harmonic components for the filter and the DC components can be get as shown in Equation (17). However, for the low frequency application e.g., PV plants, the proposed approach may not be good enough. Because the operating frequency of the system is 50 Hz/60 Hz which is so closed to 0 Hz. As a result, it takes more time to filter out the second-order harmonic components for the controllers. The parameters of the decomposition circuit shown in Figure 6 are listed in Table 1.

Parameters	Value
The resistance of R_2 , R_3 , R_7 , $R_8/k\Omega$	10
The resistance of R_1/Ω	995.2
The resistance of R_4 , R_6 , R_{13} , $R_{15}/k\Omega$	2.16
The resistance of R_5 , $R_{14}/k\Omega$	1.03
The resistance of R_9 , $R_{10}/k\Omega$	2
The resistance of $R_{11}/k\Omega$	1
The resistance of $R_{12}/k\Omega$	4.7
The capacitance of C_1/nF	8
The capacitance of C_2 , C_5 /uF	2.67
The capacitance of C_3 , C_6/uF	1
The capacitance of C_4/uF	10
Multiplier 1 and 2: ML1 Operational amplifier A1–A5:	704 LM6142

Table 1. Design specifications and parameters of the decomposition circuit.

4.2. Control Diagram

The control block diagram of the proposed algorithm is shown in Figure 8. Firstly, by employing the decomposition circuit as show in Figure 6, the *k*th branch current i_{Pk} can be decomposed into two DC components, i_{PkX} and i_{PkY} . Secondly, the current decomposed component in the X_0 axis i_{PkX} , is used for the magnitude sharing control loop of the *k*th inverter. In addition, the current decomposed component in the Y_0 axis i_{PkY} , is used for the phase difference minimized control loop of the *k*th inverter unit current i_{Pk} . Generally speaking, the received high frequency AC voltage of the secondary side cannot be used directly, but the rectifier converts it into a DC voltage for the load. As a result, the load voltage U_0 is detected and sent to the primary side control parts via radio frequency (RF) [33]. However, in the field of the PV plants, the frequency and the magnitude of the bus voltage achieved by PLL [34] are needed for regulating the output power. It is difficult to add the output voltage regulation parts in the control diagram to replace the load voltage U_0 as shown in the Figure 8.



Figure 8. The control block diagram.

With the i_{PkX} , i_{PkY} and U_o , the proportion integration (PI) controller can yield the conduction angle θ_{Lk} and phase $\theta_{\Delta k}$, which is used to generate the pulse width for the *k*th inverter to reduce the circulating currents and keep the output voltage constant. K_{Xk} is the X component of the branch current sharing PI controller. K_{Uk} is the voltage feedback PI controller. K_{Yk} is the Y component of the branch current minimizing PI controller. All of the controllers presented in the paper are designed as digital PI controllers with incremental PI algorithm which can well follow the reference signal. The equation of the incremental PI algorithm is:

$$\Delta u_{k} = K_{P}[e_{k} - e_{k-1} + \frac{T}{T_{I}}e_{k} + \frac{T_{D}}{T}(e_{k} - 2e_{k-1} + e_{k-2})]$$

= $K_{P}(1 + \frac{T}{T_{I}} + \frac{T_{D}}{T})e_{k} - K_{P}(1 + \frac{2T_{D}}{T})e_{k-1} + K_{P}\frac{T_{D}}{T}e_{k-2}$
= $\alpha e_{k} + \beta e_{k-1} + \gamma e_{k-2}$ (19)

where $\alpha = K_P(1 + \frac{T}{T_I} + \frac{T_D}{T})$, $\beta = -K_P(1 + \frac{2T_D}{T})$, $\gamma = K_P \frac{T_D}{T}$, *T* is the sampling period, and e_k is the error between the *k*th sampling value and the (k - 1)th sampling value. For the industrial application, the values of the α , β , γ for the PI controllers have been achieved by observing the experimental phenomena and debugging experience. Finally, we can get a relatively optimal values of the α , β , γ for the PI controllers when there is a fast variation. The performance of the PI controllers are verified in the following section. Furthermore, we will take faster controllers into consideration, e.g., robust controller, sliding mode controller and so on to follow the reference, when there is a faster variation.

Finally, the parallel-connected inverter IPT system will work under the condition that, the magnitudes of the branch currents are controlled to be identical, the current phase differences between the parallel units are zero, and the load voltage U_0 is equal to the reference voltage U_0 ref.

5. Experimental Results

In order to verify the proposed current phasor and voltage constant control approach, an experimental IPT prototype is set up with two identical units connected in parallel without loss of generality. The maximum output power of this prototype is 1 kW. By regulating the conduction and phase angles of the parallel inverter output voltages, the circulating currents can be reduced, and the output voltage can be controlled constantly.

The exterior appearance of the experimental setup is portrayed in Figure 9 and the circuit parameters of the prototype are listed in Table 2. The two inverters are separately powered by two isolated DC supplies. The TMS320F28335 digital signal processing (DSP) (Texas Instruments, Dallas, TX, USA) is employed as the controller of the IPT system, and generates gate pulse signals for the inverter switching devices. The experimental waveforms are measured and displayed by Agilent MSO-X 4034A scope (Agilent, Palo Alto, CA, USA).



Figure 9. The exterior appearance of the proposed IPT prototype.

From Section 3, it is clear that both the tolerance of the connection inductors and the difference of the output inverter fundamental voltages can cause the circulating currents. Considering the worst condition, we set the connection inductance $L_{e1} \neq L_{e2}$, and the output inverter fundamental voltages $\dot{U}_1(1) \neq \dot{U}_2(1)$, for validating the proposed current phasor control approach.

The connection inductance $L_{e1} = 1.2 L_e$, $L_{e2} = 0.8 L_e$, $L_e = 50 \mu$ H, the input DC voltages $E_1 = 1.15 E_2 = 115$ V and the reference load output voltage $U_{o_ref} = 100$ V. The steady-state current waveforms without the current phasor control but with the constant voltage control are shown in Figure 10. By fixing the phase angles $\theta_{\Delta 1} = \theta_{\Delta 2} = 0$ and regulating the conduction angles ($\theta_{L1} = \theta_{L2}$), the output load voltage is controlled to be 100 V as same as the reference voltage U_{o_ref} . However, there is a large difference between the branch currents i_{P1} and i_{P2} , which is shown in the bottom waveform of Figure 10 the magnitude of the twice circulating current is 5 A. With the output voltage and current (U_0 and I_0), the DC input voltages (E_1 and E_2), and the DC input currents (I_1 and I_2), the efficiency of the experiment can be calculated by equation $\eta = U_0 I_0 / (E_1 I_1 + E_2 I_2) = \frac{1008}{115.3 \times 4.69 + 100.2 \times 5.58} \approx 91.65\%$. The output power is 1 kW and the efficiency is 91.65\%. Fortunately, no DC or harmonic circulating current exists, owing to the employment of the series-parallel resonant tank.

Table 2. Design specifications and circuit parameters of inductive power transfer (IPT) prototype.

Parameters	Value
Inverter frequency f/kHz	20
Inductance of inverter 1 in series $L_{a1}/\mu H$	445.0
Capacitance of inverter 1 in series C_{a1}/nF	143.3
Inductance of inverter 1 in parallel $L_{b1}/\mu H$	42.7
Capacitance of inverter 1 in parallel C_{b1}/nF	1476.0
The connection inductance of inverter $1 L_{e1}/\mu H$	60.9
Inductance of inverter 2 in series $L_{a2}/\mu H$	432.8
Capacitance of inverter 2 in series C_{a2}/nF	147.0
Inductance of inverter 2 in parallel $L_{b2}/\mu H$	43.6
Capacitance of inverter 2 in parallel C_{b2}/nF	1472.0
The connection inductance of inverter $2 L_{e2}/\mu H$	39.2
Inductance of the primary coil $L_{\rm P}/\mu{ m H}$	195.0
Capacitance of primary circuit C_P/nF	323.7
Mutual inductance $M/\mu H$	60.0
The air gap of the primary and secondary coils d/cm	12
Inductance of the secondary coil $L_{\rm S}/\mu {\rm H}$	507.34
Capacitance of secondary circuit C _S /nF	124.8
Equivalent resistance of the load $R_{\rm L}/\Omega$	10
MOSFET: IRF640N	
RF: nRF24L01	



Figure 10. The waveforms of U_0 , i_{P1} , i_{P2} , i_P and $2\Delta i$ without the current phasor control.

With the current phasor and constant voltage control approach applied into the IPT prototype, the circulating current between the branch currents i_{P1} and i_{P2} can be reduced effectively, and the output load voltage is controlled to be 100 V. The steady-state current waveforms are shown in Figure 11. The magnitude of the twice circulating current is less than 0.5 A, which is near one-tenth of that without the current phasor control. The efficiency of the experiment can be calculated by the equation $\eta = U_0 I_0 / (E_1 I_1 + E_2 I_2) = \frac{1011}{115.3 \times 4.75 + 100.2 \times 5.48} \approx 92.18\%$. At the same output power (about 1 kW), the efficiency is 92.18% and is higher than that without the current phasor control (91.65%). In order to justify the statement, an efficiency comparison for the different operating point is provided in Figure 12. At the same time, no DC or harmonic circulating current exists. The experimental results verify the performance of the proposed current phasor and constant voltage control approach, which is suitable for the parallel-connected inverter IPT system.



Figure 11. The waveforms of U_0 , i_{P1} , i_{P2} , i_P and $2\Delta i$ with the current phasor control.



Figure 12. An efficiency comparison for different operating point (at $U_0 = 50-100$ V).

The dynamic performance during the output voltage transient is shown in Figure 13. When the reference voltage U_{o_ref} is stepped up from 80 to 100 V, U_o rises up quickly. The response time is about 24 ms, and there is no overshoot of the output voltage. When the reference voltage U_{o_ref} is stepped down from 100 to 80 V, U_o drops immediately. The response time is about 18 ms, and there is no overshoot of the output voltage too. The waveform of the output voltage is shown at the top of

Figure 13. Meanwhile, the branch currents (i_{P1} and i_{P2}) and the primary coil i_P current are given in Figure 13.



Figure 13. Close loop system response to step change in reference output load voltage from 80 to 100 V and then back to 80 V.

The dynamic performance during the load transient is shown in Figure 14. When the load R_L is stepped down from 15 to 10 Ω , it takes a little response time (about 25 ms) to return to 100 V, and the overshoot of the output voltage U_0 is small. When the load R_L is stepped up from 10 to 15 Ω , it takes a bit of response time (about 20 ms) to return to 100 V, and the overshoot of the output voltage U_0 is small. When the load R_L is stepped up from 10 to 15 Ω , it takes a bit of response time (about 20 ms) to return to 100 V, and the overshoot of the output voltage U_0 is small too. The waveform of the output voltage is shown at the top of Figure 14. Meanwhile, the branch currents (i_{P1} and i_{P2}) and the primary coil i_P current are given in Figure 14.



Figure 14. Close loop system response to step change of load resistance from 15 Ω to 10 Ω and then back to 15 Ω .

According to the experimental results mentioned above, it can be concluded that the proposed current phasor and constant voltage control approach has a good dynamic response performance with asymmetrical connection inductances and different DC input voltages.

6. Conclusions

A novel multiple inverters based IPT system has been described in this paper to upgrade the power capability of the IPT system by using low-power semiconductors. Series-parallel resonant

tank is used to suppress the DC and harmonic components of the circulating current caused by a slight unbalance of the control signal, the inner resistances of the inverters and other uncertainties. The current decomposition based phasor control method has been proposed to eliminate the fundamental circulating current. With the current decomposing method, the high frequency AC signals can be transformed to DC signals for the phasor controllers, which decreases the computational burden and complexity of the control algorithm. It provides convenience for power extension through the coordination between multiple resonant inverter units and the current decomposing circuits which reduces the manufacturing cost. Finally, a 1-kW parallel two-inverter IPT prototype has been conducted to verify the performance of the proposed control method. The experimental results demonstrate that the proposed current phasor and voltage constant control approach can reduce the fundamental circulating currents effectively and own a good dynamic performance.

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Abbreviations

Parameters ar	nd Constants
E_k	DC input voltage of each MOSFET inverter
I_k	DC input current of each MOSFET inverter
L _{ak}	Resonant inductance of each unit in series
C_{ak}	Resonant capacitance of each unit in series
L_{bk}	Resonant inductance of each unit in parallel
$C_{\mathbf{b}k}$	Resonant capacitance of each unit in parallel
L _{ek}	The connection inductance of each unit in parallel
n	The number of parallel units
u_k	The output voltage of each inverter
i_k	The output current of each inverter
$u_k(1)$	The output fundamental voltage of each parallel unit
$i_{\mathrm{P}k}$	The branch current of each parallel unit
C_{P}	The compensation capacitance of the primary circuit
i _P	The current in the primary coil
$L_{\rm P}$	The inductance of the primary coil
М	The mutual inductance between the primary and the secondary coils
LS	The inductance of the secondary coil
$C_{\rm S}$	The compensation capacitance of the secondary coil
i _S	The current in the secondary coil
C_{F}	The capacitance of the load-side DC filter
$R_{\rm L}$	The equivalent load resistance
Uo	The output voltage across the load
Io	The output current through the load

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