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Authors:

Matteo Meneghini, Oliver Hilt, Joachim Wuerfl, Gaudenzio Meneghesso

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Technology and Reliability of Normally-Off GaN HEMTs with p-Type Gate

Matteo Meneghini [1,*], Oliver Hilt [2], Joachim Wuerfl [2] and Gaudenzio Meneghesso [1]

1 Department of Information Engineering, University of Padova, via Gradenigo 6/B, 35131 Padova, Italy; gaudenzio.meneghesso@unipd.it

2 Ferdinand-Braun-Institut, Leibniz-Institut für Höchstfrequenztechnik, 12489 Berlin, Germany; Oliver.Hilt@FBH-Berlin.de (O.H.); hans-joachim.wuerfl@fbh-berlin.de (J.W.)

* Correspondence: matteo.meneghini@unipd.it; Tel.: +39-049-827-7664

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Abstract: GaN-based transistors with p-GaN gate are commonly accepted as promising devices for application in power converters, thanks to the positive and stable threshold voltage, the low on-resistance and the high breakdown field. This paper reviews the most recent results on the technology and reliability of these devices by presenting original data. The first part of the paper describes the technological issues related to the development of a p-GaN gate, and the most promising solutions for minimizing the gate leakage current. In the second part of the paper, we describe the most relevant mechanisms that limit the dynamic performance and the reliability of GaN-based normally-off transistors. More specifically, we discuss the following aspects: (i) the trapping effects specific for the p-GaN gate; (ii) the time-dependent breakdown of the p-GaN gate during positive gate stress and the related physics of failure; (iii) the stability of the electrical parameters during operation at high drain voltages. The results presented within this paper provide information on the current status of the performance and reliability of GaN-based E-mode transistors, and on the related technological issues.

Keywords: gallium nitride; transistor; p-GaN; normally-off; reliability; degradation

1. Introduction

GaN-based high electron mobility transistors (HEMTs) are excellent devices for application in power electronics. GaN is a wide bandgap semiconductor, with an energy gap of 3.4 eV, and for this reason GaN HEMTs can be operated at high temperature (>300 °C) with an excellent control of channel current. In addition, the breakdown field of GaN is 3.3 MV/cm, i.e., significantly higher than that of silicon (0.3 MV/cm). This means that a 1 µm-thick GaN layer can theoretically withstand 330 V, whereas a Si layer with the same thickness shows breakdown around 30 V. Thanks to the high breakdown field of GaN, lateral transistors with breakdown voltages higher than 1900 V have already been demonstrated [1]. In lateral GaN HEMTs, a two-dimensional electron gas (2DEG) is formed at the interface between GaN and AlGaN; the high mobility of the 2DEG (in excess of 2000 cm^2/Vs [2]) results in current densities around 1 A/mm, and in a very low on resistance (25 mΩ for a 650 V/60 A device [3]). This implies a significant reduction in the switching losses, with positive impact on the efficiency of GaN-based power converters. Finally, the low Ron × Qg product (on-resistance × gate charge) smaller than 1 nC·Ω permits to significantly reduce the switching losses of power converters. As a consequence, kW-range power converters with efficiency higher than 99% have already been demonstrated, based on GaN HEMTs [4].

A relevant aspect that is currently under study is the reliability of GaN-based transistors. In fact, during operation in high-voltage power converters, the HEMTs may be subject to extreme field and

current levels that may favor device degradation. In real-life applications, several potentially harmful conditions may be reached. As an example, in Figure 1 we report the simplified representation of a boost power converter based on a normally-off HEMT, along with the schematic V_{DS} and I_D waveforms during a switching event (for a detailed description see also [5]).

It is clear that:

1. When the transistor is in the off-state (condition (1) in Figure 1), a high drain-source voltage is applied to the HEMT. The high resulting field (Figure 2) may favor charge trapping mechanisms, including the filling/depletion of defects located in the C-doped buffer [6], the injection of electrons from the substrate [7], and surface trapping processes [8]. These mechanisms are typically fully recoverable. In addition, the exposure to high off-state bias may trigger time-dependent degradation processes that lead to the catastrophic failure of the transistors [9]
2. In principle, when the HEMT is used as a switch, current and voltage should never be high simultaneously. However, in a hard switching event (labeled as (2) in Figure 1), during the turn-on of the transistor the drain current can start to increase before the drain-source voltage of the HEMT drops. During the turn-on transient, the drain current can exceed the inductor current I_L, due to the discharge of the drain capacitance through the channel (as explained in [5]), and then become (approximately) equal to the inductor current I_L. This may favor the degradation processes triggered by hot electrons [10], and lead to an increased power dissipation (and self-heating)
3. When the HEMT is in the on-state (condition labeled as (3) in Figure 1), the gate-source junction is positively biased, at voltages in the range 5–7 V. Under these conditions, the gate junction—typically based on an MIS-stack or on a p-GaN layer—may show a time-dependent degradation [11] that leads to a strong increase in gate leakage
4. The non-ideality of the switching events (i.e., the fact that current and voltage may be high simultaneously) may increase the peak and average power dissipation, and thus the self-heating. Operation at higher temperatures may further accelerate the trapping and degradation processes described above, thus limiting device lifetime.

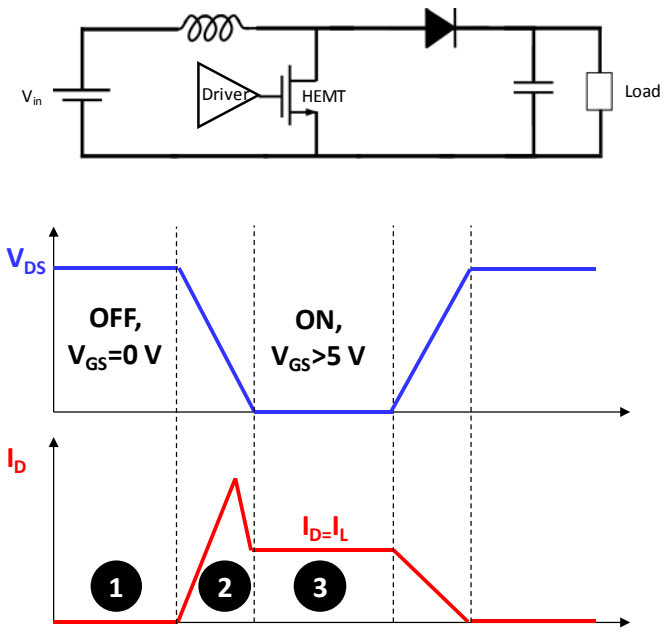

Figure 1. Schematic representation of a boost power converter and of the switching transitions during operation.

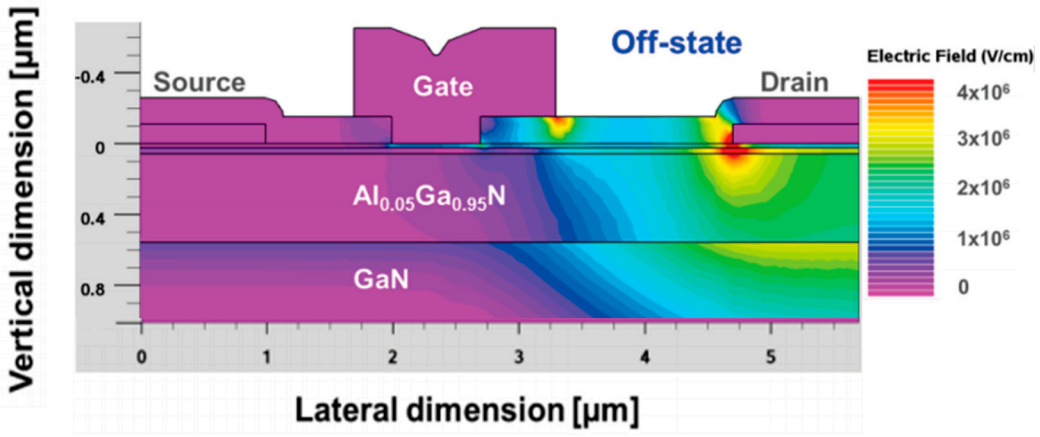

Figure 2. Simulated electric field in a GaN high electron mobility transistor (HEMT) in off-state, with a drain bias of 300 V.

For safety reasons, GaN HEMT used in power converters must be normally-off devices. In this way, if the gate driver fails and its output goes to zero, the HEMT switches to the off-state. If a simple AlGaN/GaN heterojunction is used to fabricate a HEMT, the device shows a normally-on behavior. In fact, due to the spontaneous and piezoelectric polarization of nitrides, a 2DEG is formed at the AlGaN/GaN heterointerface, even when the gate bias is equal to zero volt.

Several solutions have been proposed throughout the years to achieve normally-off operation:

(i) The implantation of fluorine ions under the gate [12]. The negative charge of the F-ions favors the depletion of the channel, and results in a positive threshold voltage V_{th}. Recent papers [13,14] showed that F-ions may show instability under high electrical stress, thus leading to changes in the threshold voltage. Chen et al. [15] indicate that on recent devices an excellent stability of fluorine atoms can be obtained through F-plasma ion implantation.

(ii) The use of a MIS-type gate stack, with full recess of the AlGaN [16]. This solution guarantees an effective minimization of the gate leakage, and threshold voltages higher than one volt. The main drawbacks of this approach are the threshold voltage instability (positive (PBTI) [17], or negative (NBTI) [18]) due to the interface/border traps in the insulator, and the time-dependent dielectric breakdown (TDDB) of the thin insulator [11].

(iii) The integration, in a single package, of a cascoded pair constituted by a (normally-on) high voltage GaN-transistor and a low voltage silicon MOSFET [19]. The latter controls the on/off state of the pair, while the GaN HEMT (that has a high robustness to high fields) holds the voltage in the off-state. The advantages of this solution are the very good stability of the threshold voltage, the possibility of using standard Si drivers, and the use of a normally-on HEMT, whose fabrication process and reliability are well assessed. On the other hand, cascode complexity is the main drawback of the cascoded solution.

(iv) The use of a p-GaN or p-AlGaN layer on top of the AlGaN/GaN heterojunction. The p-type layer lifts the band diagram of the heterostructure, and this results in a complete depletion of the 2DEG with V_{GS} = 0 V. Specific issues of HEMTs with p-GaN gate are the time-dependent degradation of the gate-stack, and trapping effects related to the Mg-acceptor.

The last approach (p-GaN HEMT) is finding wide consensus within the scientific and industrial community. For this reason, it is important to investigate the main issues related to the stability of these devices. The aim of this paper is to present an overview of the main trapping and degradation mechanisms that take place in GaN-HEMTs with p-GaN gate. After a detailed description of the technology of HEMTs with p-GaN gate, we discuss the following aspects: (i) the pulsed performance of state-of-the-art devices, and the trapping processes related to the p-GaN gate stack;

(ii) the degradation of the p-GaN gate stack at positive gate bias; and (iii) the degradation in off-state, at high drain bias.

2. Normally-Off Transistors with p-GaN Gate: Technology and Performance

In p-GaN gate HFETs, the Schottky-type metal gate of AlGaN/GaN HEMTs is replaced by a p-type doped GaN stripe (Figure 3a). Magnesium is typically used as p-type dopant. The resulting GaN-channel–AlGaN-barrier–p-GaN-gate semiconductor stack of the gate module can be considered as a pin-diode structure with a depletion zone. With proper p-type doping, the depletion zone extends over the thickness of the GaN channel layer for zero-volt gate bias and thus interrupts the 2DEG at the gate position. The GaN HFET is converted to normally-off. In view of the energy diagram, the conduction band of the channel region is shifted above the Fermi level (Figure 3b). With positive gate bias, the 2DEG transistor channel is re-established, yielding the transistor to on-state conditions.

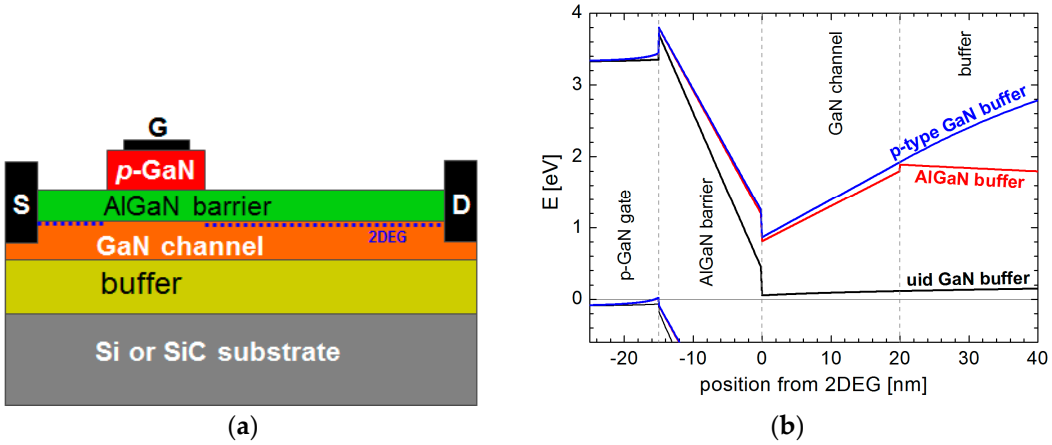

Figure 3. Normally-off GaN transistors utilizing charge management in gate region: (**a**) GaN normally-off transistors using p-type doped GaN underneath the gate metal; and (**b**) Energy band diagram of a p-GaN type normally-off transistor comparing AlGaN buffer and p-type (compensation-doped) GaN buffer versus an unintentionally doped (uid) GaN buffer.

For power applications, threshold voltage ranges above +1 V are desirable to ensure safe operation. The threshold voltage of p-GaN gate transistors is essentially adjusted by the p-GaN doping concentration and by the AlGaN barrier thickness. There is a trade-off for the 2DEG-channel electron concentration, n_e, since both V_{th} and the on-state resistance vary with n_e.

A properly designed back-barrier beneath the GaN channel layer (as is often used for preventing electron punch-through effects) helps to enhance the threshold voltage. Band diagram simulations with a p-type compensation-doped GaN buffer or an AlGaN buffer (Figure 3b) show that the conduction band energy of the AlGaN/GaN heterojunction of these structures is further shifted above the Fermi level with respect to a structure with a non-doped GaN buffer [20].

The p-GaN gate HFET was proposed by Hu et al. [21] already in 2000. Panasonic pioneered the development towards power-electronic normally-off 600 V switches [22,23]. The principal idea has also been taken up by other institutions leading to very successful GaN normally-off devices [24,25]. In a concept variation, the extrinsic p-type semiconductor material NiO_x has been taken instead of a III-N semiconductor [26]. P-type Gates for GaN HFETs can also get combined with an AlGaN-barrier gate recess to further enhance the threshold voltage without sacrificing the 2DEG electron concentration in the access region [26]. State-of-the-art p-GaN gate transistors with 600 V breakdown strength feature one-volt threshold voltage, low off-state leakage currents of 10 nA/mm for zero-volt gate bias and 0.4 A/mm drain current for on-state conditions at typically five-volt gate bias (Figure 4a,b). The on-state

resistance is 13 Ω·mm and 60 mΩ/600 V transistors with 100 A pulse capability can thus be realized with 200 mm gate periphery (Figure 4c) [24].

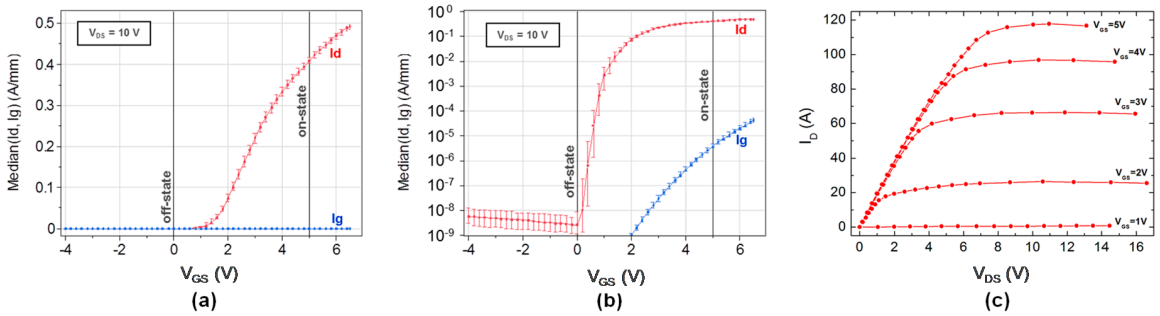

Figure 4. Current-Voltage (IV) characteristics of p-GaN gate HFETs: Transfer characteristics (drain current in red and gate current in blue) for 600 V p-GaN gate HFETs in (**a**) linear and (**b**) logarithmic scale. Wafer statistics from 36 devices are shown. Device gate width is 3.2 mm; (**c**) Output characteristics of a 60 mΩ/600 V p-GaN gate HFET with 214 mm gate width.

Figure 3a sketches the basic structure of a p-GaN gated device. The standard technological approach toward its realization is based on full-wafer MOCVD-growth of the Mg-doped p-GaN layer, which can be performed either in the same growth run as for the HFET GaN and AlGaN layers beneath or in a second MOCVD run in a separate machine to avoid Mg cross-contamination during growth of the HFET layers. Gate structuring is realized by selective dry-etching of the p-GaN epitaxial layer in an early phase of the complete device process [20,22]. Selective overgrowth of the p-GaN region has also been reported [2,8]. The process sequence has to be selected properly as it depends on the annealing hierarchies of the different metallizations used for contacting the p-GaN gate and the source/drain ohmic contacts. A Ni/Au-based p-type ohmic contact metallization which is alloyed at 530 °C under O_2-containing atmosphere was chosen for the devices presented in Figure 4. The contact resistance is in the order of 0.1–1 Ω·cm^2.

The p-doped GaN layer on top of the AlGaN barrier and the GaN channel form a *pin*-diode; this diode gradually starts turning on upon increasing positive gate bias. This manifests itself in an on-state gate current of about 10 μA/mm (Figure 4b) which might be challenging for gate driving. A replacement of the p-type ohmic contact on top of p-GaN gate layer by a p-type Schottky contact using tungsten [25] or TiN [27] as gate metal can significantly reduce the on-state gate current of the transistor. The introduced Schottky-diode is in reverse polarity with respect to the semiconductor-junction *pin*-diode. Using WSiN as Schottky-type gate contact showed a barrier height of 0.7 eV and the transistor gate swing can be extended to six to eight volts due to reduced on-state gate current (Figure 5). Using a Schottky-type instead of an ohmic gate contact can significantly simplify proper gate control in power-electronic switching environments.

A detailed investigation of the impact of gate metal on the performance of p-GaN/AlGaN/GaN transistors was presented in [28]. The authors of this study demonstrated that the work function of the gate metal has a critical impact on the electrical parameters of the devices, such as OFF-state leakage, forward operating current and threshold voltage. Several gate metals (Ni/Au, Ti/Au and Mo/Ti/Au) were compared, to discuss the importance of a trade-off between V_{TH} and output drain current.

Recent papers [29] studied the impact of the thermal budget on the metal gate on the device characteristics; more specifically, it was demonstrated that a high temperature gate annealing (800 °C) on devices with Al/Ti gate may lead to changes in the Schottky barrier height and, consequently, of the gate leakage.

Hao et al. [30] proposed a different method to fabricate normally-off p-GaN/AlGaN/HEMTs. Instead of using etching technology, they proposed to adopt hydrogen plasma to compensate holes in the p-GaN above the two-dimensional electron gas. In this way, they were able to form a high

resistivity area to reduce leakage current and to increase the control capability of the gate. Based on this approach, Hao et al. were able to obtain a threshold voltage of 1.75 V with a subthreshold slope of 90 mV/dec.

These results suggest that hydrogen may have an impact on the electrical characteristics of the devices, by compensating the shallow Mg acceptors. In addition, hydrogen atoms can show a relatively fast diffusion in GaN, as reported in previous studies [31,32], thus favoring changes in the properties of the metal/p-GaN interface [33]. For these reasons, it is important to evaluate the possible impact of hydrogen on the electrical characteristics of the devices.

Panasonic suggested that hole injection from the p-GaN gate into the GaN channel can have a positive impact on the p-GaN gate module [22]. As the hole mobility is much less than the electron mobility the holes are slowly drifting towards the source. Some holes are recombining with channel electrons, however a steady-state hole density builds up underneath the gate and in the source-side of the source gate access region. In this case charge neutrality requests for an increased electron density in the adjacent channel region, which then results in a higher drain current of the device. Hole injection from the gate is associated with a hole current flowing form the metallic gate contact. Driving the devices into the hole injection regime thus increases that forward gate current considerably.

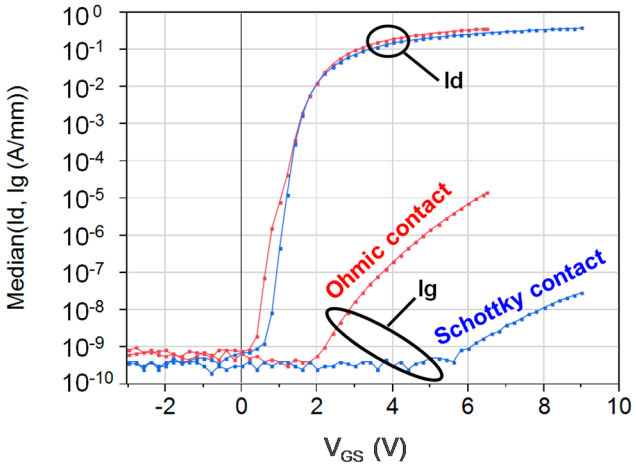

Figure 5. Transfer characteristics (drain and gate currents) for pGaN-gate transistors with Ni/Au-based ohmic gate contacts (red) and WSiN-based Schottky-type contacts (blue). Wafer medians from 36 devices each are shown. V_{DS} = 10 V.

The p-GaN technology already provided some impressive device results and could demonstrate safe and practically dispersion-free device operation up to 650 V. Similar to MIS-type and Schottky-type GaN HFETs, p-GaN HFETs of the 600–650 V class have demonstrated very low capacitances, gate charge and area-specific on-state resistances and outperform Si-based superjunction MOSFETs [24,34]. GaN power switching transistors showing significantly reduced dynamic on-state resistance normally rely on compensated (in many cases C-doped) buffer structures often in combination with ternary AlGaN layers [34–36]. The dynamic R_{ON} data for 400–600 V switching of p-GaN gate HFETs (Figure 6) are competitive to values achieved with normally-on HFETs using MIS or Schottky-type gate modules [22,24]. The dynamic R_{ON} in HV GaN-HFETs seems to be still dominated by buffer related trapping effects. The combination of GaN channel thickness and buffer layer material properties and dimensions have to be optimized accordingly.

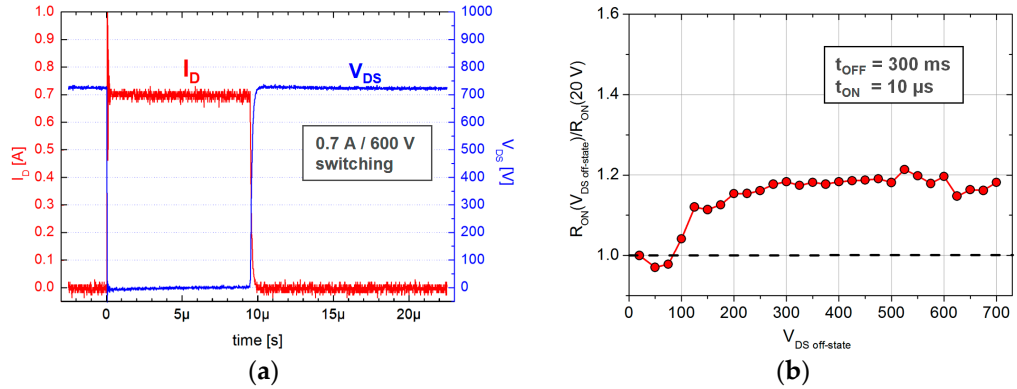

Figure 6. Dynamic performance of a p-GaN gate HFET with 9.2 mm gate: (**a**) 0.7 A/700 V switching transient of a p-GaN gate HFET switching a 1 kΩ resistive load; (**b**) Dynamic on-state resistance increase as a function of off-state stress voltage as determined from the on-state voltage drop during the 10 µs switching event. Off-state bias was applied for 300 ms before switching on.

3. Recoverable and Permanent Degradation of Normally-Off Transistors with p-GaN Gate

This section presents an overview on the recoverable and permanent degradation processes that affect the performance of GaN-based HEMTs with p-GaN gate. In the first part of the section, we describe the pulsed characteristics of GaN-HEMTs with p-GaN gate, and the charge trapping mechanisms induced by positive gate bias. The second part describes the time-dependent degradation of the p-GaN gate induced by the exposure to positive gate bias. Finally, in the third part we describe the failure processes induced by high drain voltage in the off-state.

3.1. Charge Trapping Processes Related to the p-GaN Gate

GaN-HEMTs with p-GaN are turned on with a positive gate-bias, typically higher than four volts. It is therefore important to evaluate and describe the trapping processes induced by the exposure to a positive gate bias, with a low drain voltage (this condition is representative for operation in linear region, phase 3 in Figure 1). In this condition, the drain voltage is fairly low (less than one to two volts): as a consequence, trapping is not supposed to take place in the gate-drain access region, where the lateral field is low. On the other hand, with a positive gate bias, trapping may occur in the region under the gate, thus affecting the threshold voltage of the devices.

Figure 7a reports the pulsed I_D-V_{DS} curves measured starting from several quiescent bias points on a GaN HEMT with p-GaN gate. The quiescent bias points have increasing gate voltage (from zero volts to six volts), and zero drain voltage. During the measurements, the devices are in the on-state for 1 µs, and in the quiescent bias for 99 µs. As can be noticed (Figure 7a), the exposure to a positive gate bias does not induce any variation of the on-resistance. On the other hand, the drain current in the saturation region shows a measurable increase, representative of a negative current collapse. This is due to a negative (leftwards) shift of the threshold voltage (NBTI), see Figure 7b. This behavior is different from what observed in GaN-based MIS-HEMT that, when submitted to positive bias, show a positive-threshold instability (PBTI) [37], due to the trapping of electrons in the insulator/AlGaN stack.

We can tentatively explain the observed NBTI of HEMTs with p-GaN gate as follows: when a positive voltage is applied to the gate, holes are injected from the metal to the p-GaN layer. The injected holes may accumulate at the p-GaN/AlGaN interface (see the schematic band diagrams in Figure 8), or at trap states located in the AlGaN/GaN heterostructure. This leads to a temporary increase in 2DEG density, i.e., to the negative shift in threshold voltage.

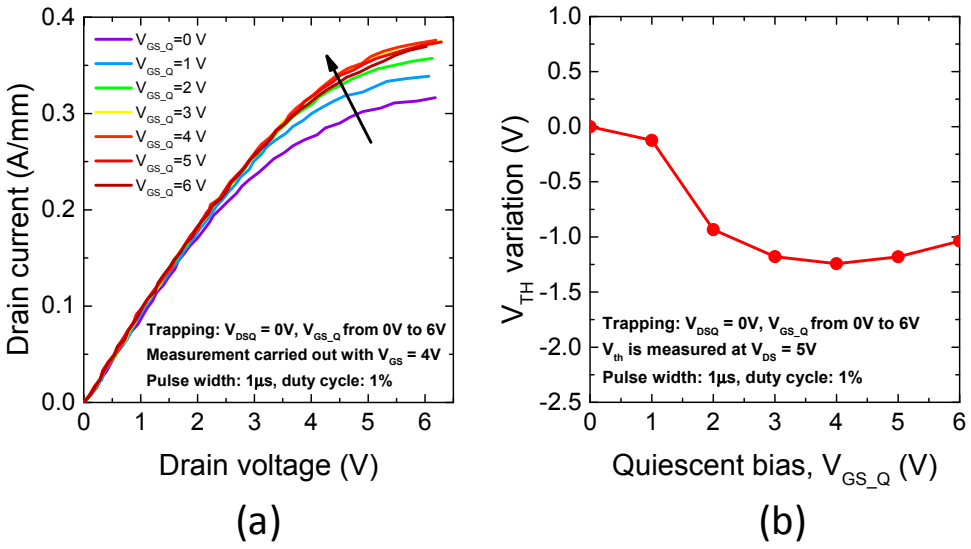

Figure 7. (**a**) Pulsed I_D-V_{DS} curves measured starting from several quiescent bias points on a GaN HEMT with p-GaN gate; (**b**) Variation of threshold voltage as a function of the quiescent bias point V_{GS_Q} applied to the gate (Courtesy of Isabella Rossetto, University of Padova).

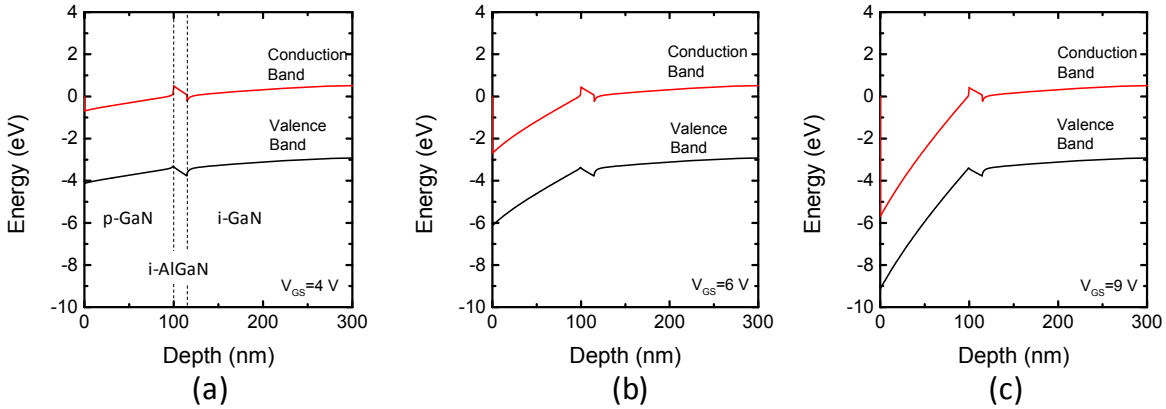

Figure 8. Band diagram of a HEMT with p-GaN gate, as simulated under the gate. The three frames refer to different gate voltages: (**a**) V_{GS} = 4 V; (**b**) V_{GS} = 6 V; (**c**) V_{GS} = 9 V. Courtesy of Eldad Bahat-Treidel, FBH (Berlin, Germany).

As in the case of normally-off transistors, the exposure to high drain bias in the off-state can trigger further trapping processes, due to the filling of surface states [8], to defects located in the (C-doped) buffer [6], or to the injection of electrons from the substrate [38]. These trapping processes are not specific for p-GaN gate devices, and their discussion is beyond the scope of this paper. It is worth noticing that through proper optimization of the growth parameters, and through the use of specific device structures, it is possible to completely suppress current collapse in GaN HEMTs with p-GaN gate. Kaneko et al. [39] recently proposed to use hole injection from the drain to compensate the trapped electrons, thus eliminating the current collapse.

3.2. Degradation Processes Induced by Positive Gate Bias

GaN-based transistors with p-GaN gate have typically a threshold voltage higher than one volt; in order to minimize the on-resistance, the devices are turned on with a gate voltage V_{GS} in the range four to seven volts, depending on the driver and circuit application. When the gate-source voltage exceeds the threshold voltage, the band diagram of the transistor changes significantly, and most of

the voltage exceeding threshold drops on the p-GaN layer. This results in the increase in the field (and of the band bending) on the p-GaN layer: this is explained in Figure 8, which shows the band diagram calculated for three different gate voltages, V_{GS} = 4 V, V_{GS} = 6 V, V_{GS} = 9 V. On the other hand, the electric field in the AlGaN layer does not change significantly when the gate bias increases above four volts.

The high electric field in the p-GaN layer may favor the time-dependent degradation process of the gate junction. This can be easily understood by submitting GaN-HEMTs with p-GaN gate to constant voltage stress, with positive gate bias and grounded source. Figure 9 reports the results obtained by stressing identical transistors with a gate-source bias of 8.5 V (with V_{DS} = 0 V). The differences in gate current and time-to-failure are due to sample-to-sample variability. After an initial phase where gate current is stable, a step-wise variation is observed, leading to a significant increase in gate current. Time-to-failure (TTF) is defined as the time necessary for reaching a gate leakage of 10 mA (measured at 8.5 V). Electroluminescence measurements (Figure 10) indicate that each of the steps in gate current corresponds to the appearance of a "hot-spot", corresponding to the creation of a leakage path.

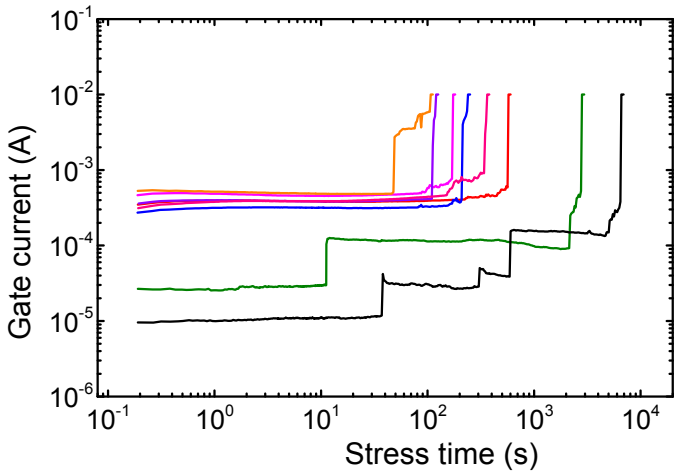

Figure 9. Current variation measured during a constant voltage experiment on identical transistors with p-GaN gate. Stress conditions: V_G = 8.5 V, V_S = 0 V, drain floating.

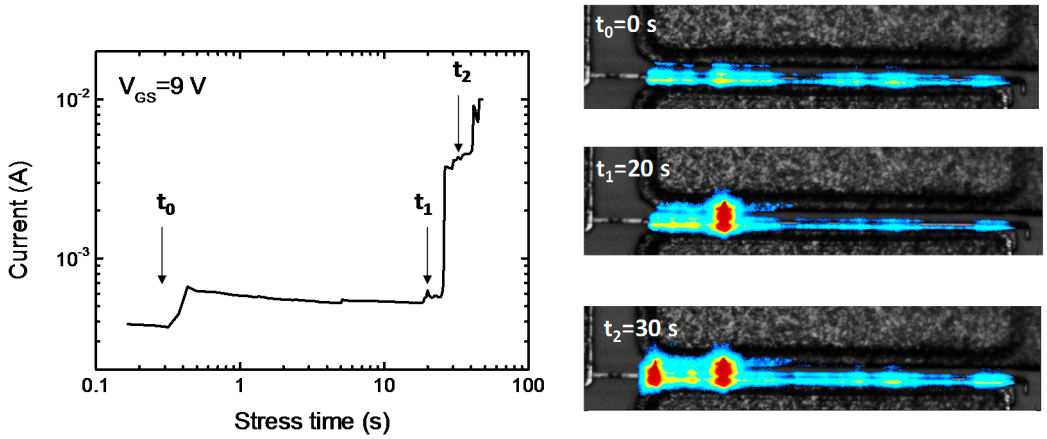

Figure 10. (**Left**) Current variation measured during a constant voltage experiment (V_{GS} = 9 V); (**Right**) False color electroluminescence (EL) pattern reporting the distribution of light emitted by the gate junction during stress, at different time intervals.

The generation of hot spots has been reported also for reverse-biased Schottky junctions on AlGaN/GaN [40]. In that case, the time-dependent breakdown has been ascribed to a defect

generation/percolation process due to the high field reached within the AlGaN layer. In the case of HEMTs with p-GaN gate, the situation is different: the stress bias is positive, and most of the potential falls on the p-GaN layer. The situation can be complicated by the fact that in several cases the metal/p-GaN contact is a Schottky junction that is reversely biased when the gate voltage is positive [27]. This may lead to the partial depletion of the p-GaN layer in proximity of the surface. A first possible mechanism that can explain the time-dependent failure of the devices is the following: at high positive bias, the high electric field in the p-GaN favors the propagation of defects, due to generation/percolation process [41]. The depleted region next to the p-GaN surface may act as a "leaky" insulator, and show a time-dependent breakdown similar to what happens in dielectrics. TTF was found to be Weibull distributed, and to have an exponential dependence on stress voltage. These evidence support the hypothesis that degradation is due to a percolation process. Two-dimensional simulations [42] indicated that the field in the p-GaN peaks at the edges of the gate. Degradation is therefore supposed to be stronger in proximity of the gate edges, rather than under the gate. Recent papers suggested that a second process can contribute to the breakdown of the gate junction, namely avalanche multiplication. Wu et al. [27] proposed that at high positive gate bias, electrons can be injected from the channel to the p-GaN region, where a high field is present. The electrons are therefore accelerated by the high field (see Figure 11), and avalanche processes may lead to device breakdown. A third possible model was proposed by Tapajna et al. [43], who suggested that degradation is initiated by the generation of donor-like traps in the p-GaN, close to the AlGaN interface. This locally lowers the electric field in the AlGaN, and leads to the generation of localized leakage paths. This would eventually lead to the soft- and hard-breakdown of the gate stack. Degradation of the SiN passivation at the gate edges may also take place during stress [42].

Light emission is supposed to take place in the p-GaN layer, via three possible processes: (i) as shown in Figure 11, the electrons injected from the channel towards the p-GaN region are accelerated by the high field, thus gaining a high energy, and emitting light due to multiple-step transitions (Bremsstrahlung) [44]. The electrons may also recombine with the holes present in the p-GaN layer, either via (ii) band-to-band process [45]; or (iii) through defect states. Recent papers [44] indicated a strong yellow luminescence (2.25 eV), which is consistent with defect-assisted recombination in the p-GaN layer.

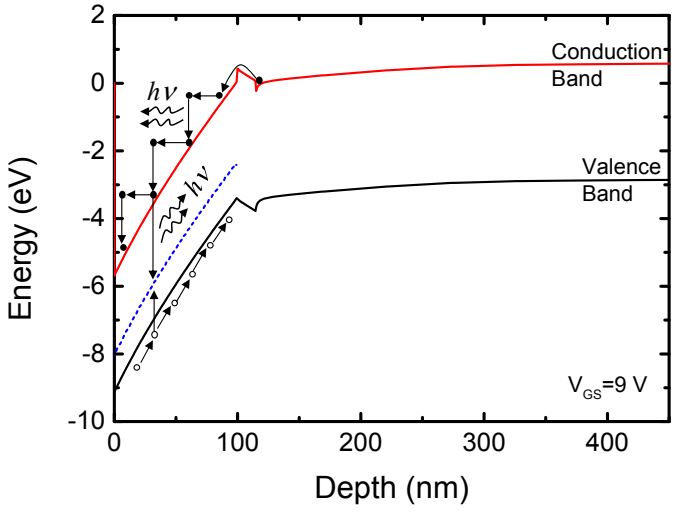

Figure 11. Schematic band diagram of an HEMT with p-GaN gate with V_{GS} = 9 V showing the various processes responsible for EL.

3.3. Degradation Processes Induced by High Drain Bias in the Off-State

Other relevant degradation processes may occur when the devices are stressed in the off-state, with a high drain bias. The several processes that contribute to drain current conduction in the sub-threshold regime (with high drain bias) are briefly summarized in the following: (i) a non-optimal process may enhance the leakage conduction through surface states and/or defects within the passivation layer; (ii) the reverse leakage of the p-GaN/AlGaN junction is generally relatively low, however in stressed devices the leakage through the AlGaN may become stronger, and contribute to the overall drain current; (iii) if the buffer is not optimized, a significant drain-source leakage may be present, due to the injection of electrons (coming from the source) deep into the buffer below the depleted region of the gate; this process is also referred to as punch-through [46]. Finally, for extremely high drain voltages vertical (from drain to substrate) leakage may also be present [1].

Figure 12 reports the results of a breakdown test carried out on a transistor with p-GaN gate; with the transistor in the off-state (V_{GS} = −8 V) the drain bias is increased until failure. As can be noticed, when the drain voltage ranges between 0 V and 400 V, drain current is dominated by gate leakage, flowing either through surface paths or as a reverse current of the p-GaN/AlGaN junction. When the drain bias exceeds 400 V, the drain current starts being dominated by drain-source leakage, i.e., by the injection of electrons from the source to the deep buffer (under the depleted region induced by the negative gate bias). It is worth noticing that the drain current remains well below 10 μA/mm up to a drain voltage of 800 V, indicating that the devices have very good blocking properties.

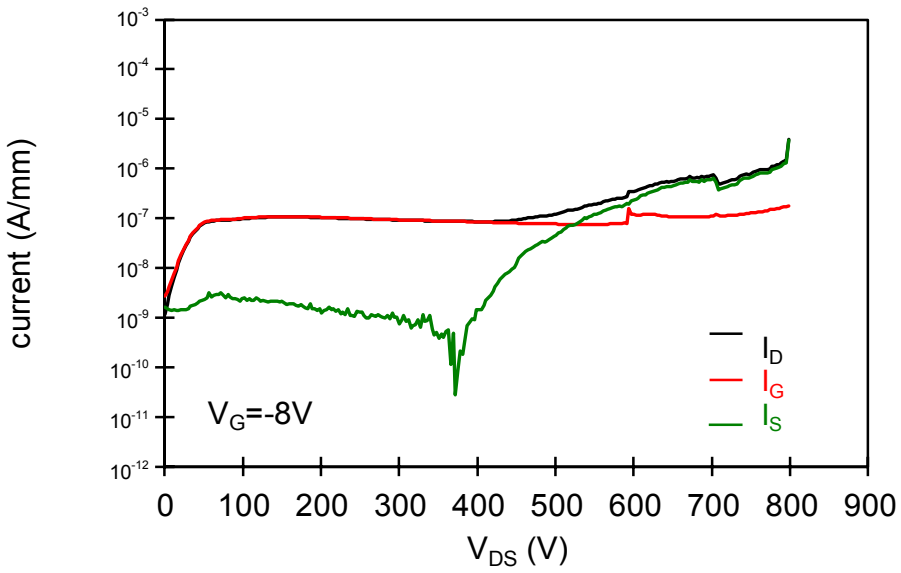

Figure 12. Breakdown test carried out on a transistor with p-GaN gate. With a negative gate bias (V_{GS} = −8 V), the drain bias is swept to 800 V, and the source, drain and gate currents ae measured.

For drain voltages close to 800 V, the electric field may significantly increase, both at the gate head and in proximity of the drain pad (see Figure 2). This may lead to the catastrophic failure of the device, and to the shortening of the transistor.

The degradation dynamics can be better understood by carrying out step-stress tests. Figure 13 reports the results of a representative experiment: gate voltage is fixed to V_{GS} = −4 V in order to guarantee off-state operation, and drain bias is increased by 50 V every 120 s, until failure is reached. The gate, source and drain current are measured during each of the stages of the test. When a moderate drain bias is applied (in the range 0–400 V), drain current is equal to gate current. At the beginning of each step, gate current decreases gradually: this decrease is fully recoverable (see two subsequent steps) and may be ascribed to charge trapping effects. In the same V_{DS} range, source-drain leakage is very low, since the drain bias is not sufficiently high to induce a measurable punch-through. For drain

voltages higher than 400 V (as seen in the breakdown curves) source current becomes dominant, and this behavior is maintained until failure. It is worth noticing that before failure (V_{DS} > 800 V) current becomes noisy, indicating a gradual generation of defects within the device structure that eventually leads to the failure (V_{DS} = 900 V for the device in Figure 13).

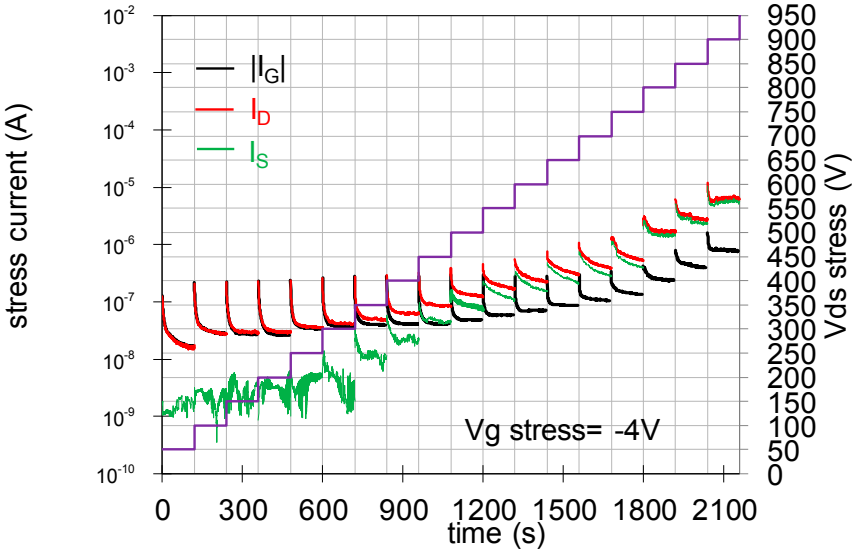

Figure 13. Results of a step-stress experiment carried out on a transistor with L_{GD} = 15 μm. During stress, V_{GS} = −4 V and the drain voltage is increased by 50 V every 120 s.

4. Conclusions

In summary, with this paper we have described the main technological issues related to the development of normally-off transistors with p-GaN gate. In addition, we have described the trapping and degradation processes of these devices. The original results described within this paper provide general guidelines for the development of normally-off GaN-based HEMTs, and information on the main parasitic/degradation processes.

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