NMOS-Based Integrated Modular Bypass for Use in Solar Systems (NIMBUS): Intelligent Bypass for Reducing Partial Shading Power Loss in Solar Panel Applications

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NMOS-Based Integrated Modular Bypass for Use in Solar Systems (NIMBUS): Intelligent Bypass for Reducing Partial Shading Power Loss in Solar Panel Applications

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Abstract: NMOS-based Integrated Modular Bypass for Use in Solar systems (NIMBUS) is designed as a replacement for the traditional bypass diode, used in common solar panels. Because of the series connection between the individual solar cells, the power output of a photovoltaic (PV) panel will drop disproportionally under partial shading. Currently, this is solved by dividing the PV panel into substrings, each with a diode bypass placed in parallel. This allows an alternative current path. However, the diodes still have a significant voltage drop (about 350 mV), and due to the fairly large currents in a panel, the diodes are dissipating power that we would rather see at the output of the panel. The NIMBUS chip, being a low-voltage-drop switch, aims to replace these diodes and, thus, reduce that power loss. NIMBUS is a smart bypass: a completely stand-alone system that detects the failing of one or more cells and activates when necessary. It is designed for a 100-mV voltage drop under a 5-A load current. When two or more NIMBUS chips are placed in parallel, an internal synchronization circuit ensures proper operation to provide for larger load currents. This paper will elaborate on the operation, design and implementation of the NIMBUS chip, as well as on the first measurements.

Keywords: photovoltaic power; power loss; partial shading; diode bypass; smart bypass

1. Introduction

Typically, a single Si solar cell can generate a voltage of about 0.5–0.6 V with a photocurrent depending on the illuminated surface area of the cell (usually about 30–35 mA/cm^2). To increase the output voltage to a more workable level and to limit the current in the panel connections, all cells in a solar panel are placed in series. A traditional photovoltaic (PV) panel consists of 60 cells, generating about 30 V and 5–10 A. While the series connection is very useful in practice, it comes with a big disadvantage: the entire output current is determined by the cell with the lowest photocurrent. Differences in this photocurrent can arise due to the statistical distributions in the characteristics of the PV cells, but a more significant discrepancy occurs due to partial shading of the panel. Under partial shading, not only the power of the shaded cell is lost, but the output power of the fully-illuminated cells is dramatically reduced, as well [1]. In extremis, the power of the entire panel can drop to zero if just one cell is completely shaded, until the failing cell goes in reverse breakdown. On top of this, the power generated by the irradiated cells that is not delivered to the load is dissipated in the panel itself, creating hot spots, which is known to cause permanent damage [2,3].

There are several ways to tackle this issue. By optimizing the parasitic shunt resistance of the solar cell, the partial shading power loss can be reduced [4]. Normally, we want to maximize this

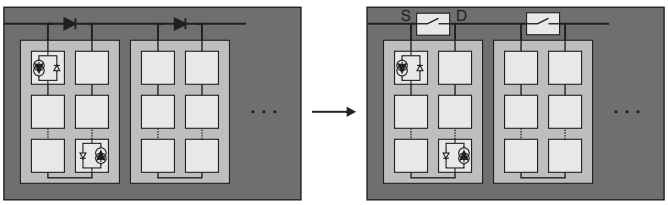
shunt resistance, since it leads to power loss in a fully-irradiated solar panel. However, when there is a current mismatch between the cells, one can calculate an optimized shunt resistance that will maximize the output power. This solution is not very practical, since the optimized value for the shunt resistance depends on the exact shading to illumination ratio.

Another solution is to include parallel connections between the cells. This way, the output current will not be blocked when just one cell is shaded. Research has found that a Totally Cross Tied (TCT) connection scheme, where all cells are connected in a mesh network, gives the best results [5,6]. However creating these interconnections on a common solar panel is not so straightforward, and the resulting higher current flowing through these interconnections will also create additional power loss.

There are more complex solutions, where the cells of the solar panel are divided into groups (substrings), where each substring is provided with a DC/DC converter. Current mismatch between the substrings is no longer an issue, but it is a very expensive solution. To reduce the cost, some converters only try to eliminate the current mismatch and operate on power differences [7]. These converters can be smaller and less expensive. Reconfigurable panels, where one deals with the difference in photocurrent by rearranging individual cells or substrings ([8] gives an extensive overview of the current techniques), also provide a flexible solution, but at the cost of an increased complexity.

However, the most common solution is to provide each substring (typically the solar panel is divided into three substrings of 20 cells) with a junction diode in anti-parallel (see Figure 1a). When the photocurrent of one (or more) cells in such a substring is reduced, the excess current (the surplus current generated by the other substrings) flows through this bypass diode. The cells in the other substrings are not affected and can still generate full power, but the substring with the shaded cell(s) is bypassed and does not contribute to the output power generation. Obviously, there are still shortcomings. The most clear shortcoming is that an entire substring is bypassed (it may still hold some non-shaded cells and/or the shaded cells can still produce some, albeit less, power) when one of its cells is shaded. This is where the Maximum Power Point (MPP) tracker comes into play. Without any bypass diodes, this MPP is fairly easy to find, but with every bypass that is added, another local MPP is introduced (one where that bypass is active and one where it is not) [9]. The job of the MPP tracker is to find the global MPP, which can be challenging. However, both simulations [10] and real life field test results [11] have shown that even when just one cell is failing (causing an entire substring to be bypassed), the global MPP with an active bypass can be higher than without the bypass present (obviously depending on the irradiation difference between the cells).

Another unavoidable shortcoming is that the bypass diodes themselves are dissipating power, reducing the power available at the output. Ideally, a bypass is a switch with zero on-resistance. It detects the failure of a cell inside its substring and activates itself (see Figure 1). Such a "smart bypass" is one of the building blocks for smart PV modules [12]. In [13], a proof-of-concept of such a smart bypass is presented. This paper elaborates on a new and improved version of this smart bypass, the NMOS-based Integrated Modular Bypass for Use in Solar systems (NIMBUS) chip. Section 2 describes the functionality of the chip. Section 3 provides some power simulations. In Section 4, we take a look at the physical implementation of the chip and the resulting measurements.



(**a**) (**b**)

Figure 1. In a solar panel, the traditional bypass diode (**a**) is replaced with a smart bypass with (**b**) a minimal on-resistance.

2. Design of the NIMBUS

2.1. General Operation

NIMBUS is an acronym for "NMOS-based Integrated Modular Bypass for Use in Solar Systems". Its block diagram is depicted in Figure 2. At its center, there is a large reverse blocking MOSFET (T_1) that will serve as the main current guiding switch. Its floating bulk ensures blocking in both directions, as long as V_{gate} has the proper value. It is important to note that the NIMBUS is a completely stand-alone system. Just like using a bypass diode, there are only two connections to be made with the solar panel. The source (S) and drain (D) connections of the NIMBUS replace the anode and cathode connections of the bypass diode, respectively (see Figure 1). The drain voltage (V_D) will also serve as the reference voltage for the entire chip.

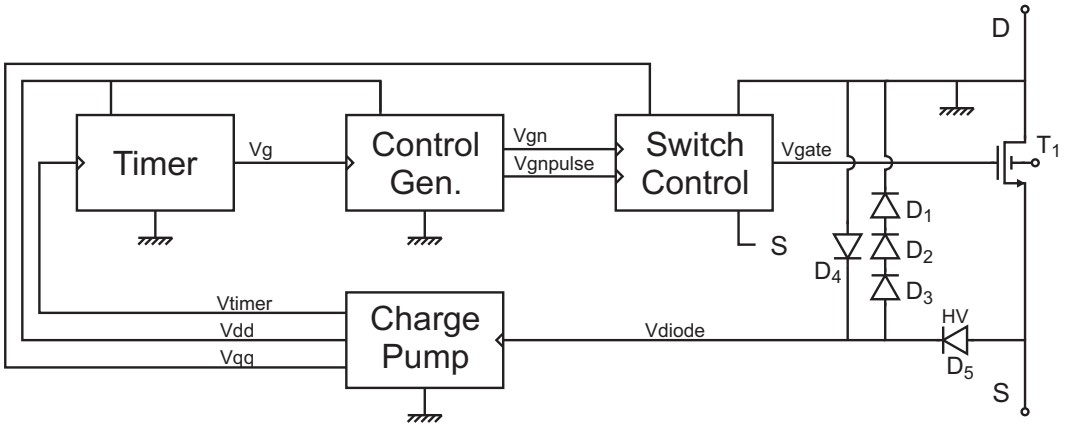


Figure 2. The block diagram of the NMOS-based Integrated Modular Bypass for Use in Solar systems (NIMBUS) chip.

When there is no shade and all cells are illuminated, every substring is generating power. In this case, V_D will be higher than V_S (or, with $V_D = 0$ V, $V_S < 0$). Switch control (see below) adjusts V_{gate} to keep T_1 in the off-state. At this point, the other blocks in the system are inactive. When one or more of the cells in the substring are generating less current for some reason, the excess current from the other substrings will flow through the anti-parallel diodes D_5 and D_{1-3}. When this happens, a polarity reversal occurs: V_S becomes higher than V_D (basically, the substring starts dissipating power). Again, switch control keeps T_1 in the off-state. However, when the charge pump sees a positive input voltage, it is activated and starts to generate the internal supply voltages (V_{DD}, V_{QQ} and V_{timer}) to 3.3 V, which are stored on internal capacitors (C_{DD}, C_{QQ} and C_{timer}, respectively). When the generation is completed, the timer block gives the signal that the switch can be activated. The exact control signals that drive switch control are generated in the control generator block.

When switch control activates T_1, all current flows through the large switch, and V_S drops to a low voltage (e.g., 50–100 mV, ideally 0 V). At this point, the charge pump stops pumping, and the charged storage capacitors provide the necessary power. However, with the substring being shorted, it is very difficult to notice when the cells that were once in the shade are fully illuminated again. Therefore, the timer block will also act as a periodic sampler. After a predetermined amount of time (e.g., 1 s; it seems that relevant irradiance fluctuations happen in the order of seconds [14]) after the switch is activated, the timer block will signal switch control to deactivate T_1. When the cells are still in the shade, V_S will jump to a positive voltage, the charge pump will be reactivated, the capacitors will be recharged and the timer block will reactivate T_1. If however all cells are fully irradiated, there will be no excess current; thus, V_S will be negative, and the entire system shuts down. The efficiency of the system is then determined by the on-resistance of the switch and the ratio between the sample period (time between two samples) and the sampling time (duration of the sampling itself, *i.e.*, time between

polarity reversal and switch activation). The latter is usually negligible, as the sample period is of the order of seconds, while the sampling time is about 200 µs.

The switch control circuit is shown in Figure 3. As said, its function is to keep the switch in the off-state, irrespective of the polarity of the switch, and to turn the switch on and off when needed. Switch control is comprised of three distinct circuits: Circuit A, which keeps the switch in the off-state, Circuit B to turn the switch on or off and Gate Protection Circuit (GPC), which protects the gate of T_1 from possible overvoltage.

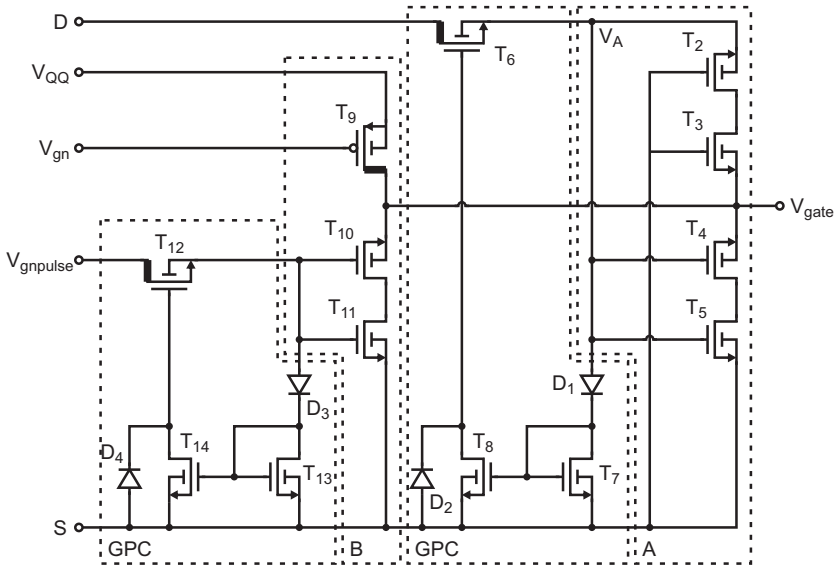


Figure 3. Schematic of the switch control block. Circuit A keeps the switch in the off state. Circuit B changes the state of the switch. GPC (Gate Protection Circuit) protects the gate of the switch from overvoltage.

For a more complete elaboration of the switch control, we refer to [13].

2.2. Shortcomings of the First Prototype

To provide a proof-of-concept of such a smart bypass, a prototype was created in the I3T50 technology of OnSemi, a 50-V extension to the 0.35 µm CMOS process. It was designed for a 150-mV voltage drop under the maximum load current of 0.5 A (0.3 Ω). The sample period was about 10 ms, with a sampling time of 250 µs. Therein lie the first and most important shortcomings. These values, while sufficient for a less expensive proof-of-concept, are not practically useful in a real solar system. The on-resistance is to be decreased significantly while the maximum load current needs a drastic increase.

The relatively short sample period not only causes a significant power consumption of the smart bypass, but also leads to a more fundamental problem. In the prototype, the time is measured by discharging a large capacitor (C_{timer}) through a large resistor (200 MΩ). When this voltage drops below a certain value, the timer block deactivates T_1. The used resistor in the I3T50 technology does not only take up a lot of die area, but being a poly-Si resistor, also has a negative temperature coefficient: the value decreases with increasing temperature. This means that when the chip heats up due to a relatively short sample period, the resistor value will decrease, which even further decreases the sample period. Above a certain current level, this results in enough positive feedback to completely destroy the chip. The timer block needs a full revision.

Another, smaller, issue is the fact that the generated voltage of the charge pump is not completely stable and dependent on the temperature and its input voltage (V_{diode}). A simple feedback loop can solve this problem.

2.3. Upgrades and Improvements

2.3.1. Switch T_1

In the prototype, switch T_1 was a high-voltage NDMOS (Double-Diffused n-type MOSFET) device. The NDMOS in the I3T50 technology is able to block a voltage up to 40 V between drain and source. A high-voltage device (>3.3 V) is necessary, since the generated voltage of a single 20-cell substring (which is the drain-source voltage of the main MOSFET) can go up to 12 V. A regular NMOS would break down. To get an on-resistance of 0.3 Ω, a channel width of 96 mm was needed. The capacitor C_{QQ}, which holds the charge to activate T_1, has a value of 1 nF. Together, they occupy 1.2 mm^2 of the die area.

To create a more practically useful device, we aimed at creating a switch with an on-resistance of 20 mΩ for a load current of maximum 5 A (100 mV voltage drop under full load). Using the same NDMOS device, this would mean an immense increase in size for both the NDMOS and the storage capacitor C_{QQ}, which would make it difficult to make the device cost effective. We opted to replace the high-voltage NDMOS device with a regular low-voltage NMOS. The on-resistance ($\Omega \cdot$ mm^2) of this device in the I3T50 technology is an order of magnitude lower than its high-voltage brother. This way, a 20 mΩ NMOS can be created with an area of 0.3 mm^2. The channel width of such a device is an impressive 140 mm.

Of course, as mentioned above, this causes a problem when used on a regular 20-cell substring. For this bypass to be used, we needed to change the traditional solar panel setup (three substrings of 20 cells) to a setup with smaller substrings, being 10 substrings of six cells. A substring of six cells generates a maximum of 3.6 V, just within the operating range of an NMOS. The panel setup with the location of the bypasses can be seen in Figure 4. Smaller substrings with more bypasses also give an advantage with regards to power efficiency (see Section 3). This conclusion was also found after a year-long measurement in the field [15] (Chapter 5).

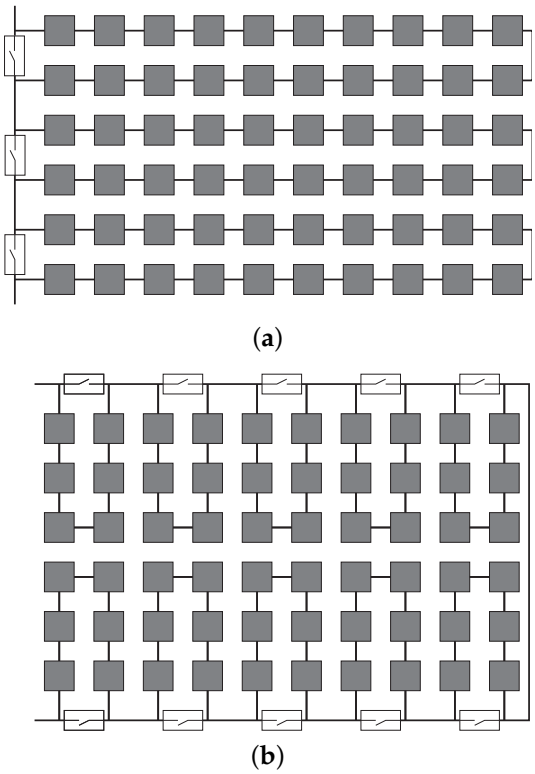


Figure 4. (**a**) The old panel setup , three substrings of 20 cells *vs.* (**b**) the new panel setup , 10 substrings of six cells with the location of the bypasses.

2.3.2. Charge Pump

The schematic of the improved charge pump is depicted in Figure 5. The charge pump (I_1) itself is a simple two-stage Dickson charge pump, with V_{diode} as the input voltage (see also Figure 2). The output voltage is compared to a bandgap reference voltage (I_2, based on [16]). A high V_{back} signal disables the charge pump. When there is polarity reversal in the substring, V_{diode} will jump to 1.8 V–2.8 V. This voltage powers the bandgap reference and comparator and the charge pump starts to charge the capacitors holding V_{DD} (powering the digital blocks), V_{timer} (for measuring time) and V_{QQ} (holding the charge for the large gate capacitance). When the desired voltage is reached, the charge pump is deactivated. T_3 is also deactivated to avoid charge flowing away through the voltage divider.

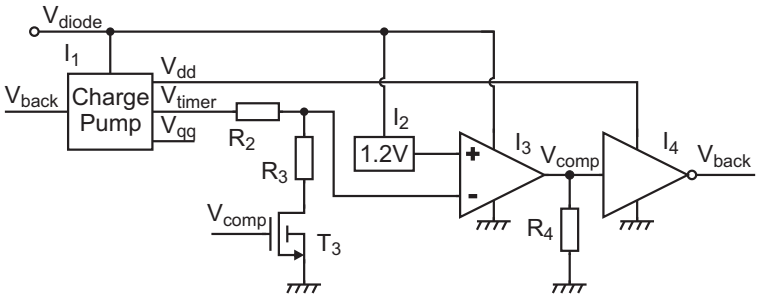


Figure 5. Schematic of the improved charge pump with a feedback loop.

2.3.3. Timer

The renewed timer block can be seen in Figure 6.

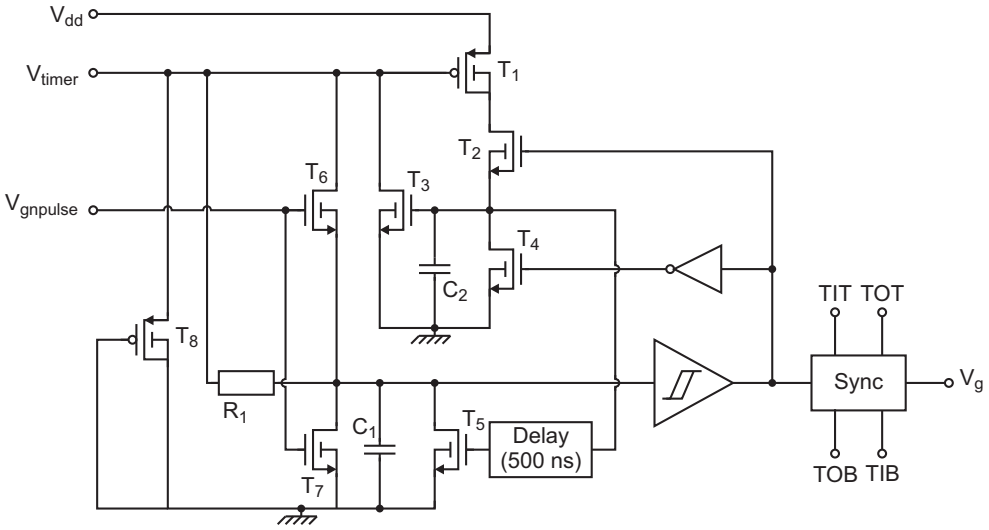


Figure 6. Schematic of the timer block.

The measurement of the sampling time happens in the same way as in the prototype: V_{timer} is fed to the Schmitt trigger trough a small delay (R_1, C_1). The measurement of the sample period is still done by discharging the C_{timer} capacitor. To get a sample period of 1 s, either the capacitor needs to be extremely large, or the pulled current extremely low. With C_{timer} being 1.3 nF, the pulled current should be no more than 500 pA–1 nA. A couple of options were investigated to achieve such low current levels: we could either use self-biasing subthreshold current sources, as shown in Figure 7 (based on the circuits from [17,18]), or use a simple MOSFET with a very large channel length. We will have a look at their performances.

Five different circuits were examined. The first three were the subthreshold current source of Figure 7a, with R_1 being 20 MΩ and 40 MΩ or replaced with an NMOS with a very large channel length ($L = 2520$ µm). A fourth circuit was that of Figure 7b. The final 'circuit' was simply a PMOS with a very large channel length ($L = 19,920$ µm). These have been implemented in the same I3T50 technology (Table 1 gives an overview for easy reference).

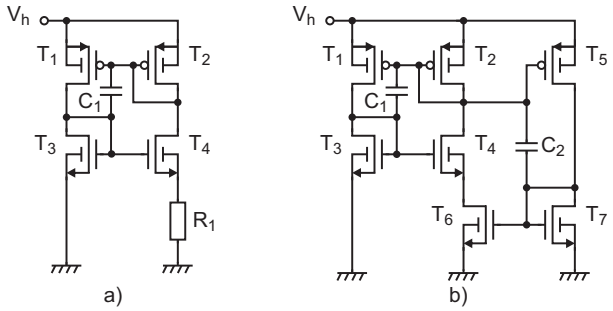


Figure 7. Examined subthreshold current sources: (**a**) with resistor [18] and (**b**) without resistor [17].

Table 1. Overview of the tested circuits.

#	Circuit 1	Circuit 2	Circuit 3	Circuit 4	Circuit 5
	Circuit of Figure 7a, R_1 is an NMOS with L = 2.5 mm	A single PMOS with L = 20.0 mm and a grounded gate	Circuit of Figure 7a, R_1 = 20 MΩ	Circuit of Figure 7a, R_1 = 40 MΩ	Circuit of Figure 7b
I_{total}	2.5 nA	1.5 nA	2 nA	1 nA	2 nA
Die area	15,273 µm^2	34,560 µm^2	180,800 µm^2	350,140 µm^2	39,816 µm^2

Since the timer block is powered by a charged capacitor, it is crucial that the powered blocks use as little power as possible. When the input voltage of the Schmitt trigger drops below the threshold voltage of a PMOS (present in the input stage of the Schmitt trigger) this storage capacitor is continuously drained, decreasing the supply voltage. To work around this, C_{timer} is quickly discharged once its voltage drops below the PMOS threshold voltage (see also [13]). The measurement results are collected in Figure 8. It shows the voltage of the storage capacitor, V_{timer}, as a function of time. All circuits seem to be suitable, but when complexity and die size are taken into account, a simple large-channel PMOS seems to be the best candidate. This function is realized by transistor T_8 in Figure 6.

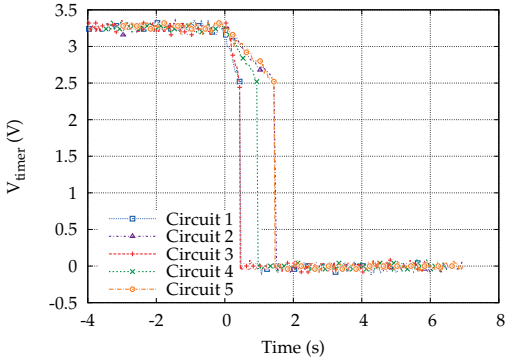


Figure 8. Measurement results of the different current sources. The capacitor voltage is drawn as a function of time.

2.3.4. Synchronization Circuit

The NIMBUS chip is designed for a maximum load current of 5 A. Many solar systems, however, can generate currents up to 10 A. To also be compliant with those current levels, we included the option of placing two (or more) NIMBUS chips in parallel. Two parallel switches need to be perfectly synchronized. If one switch were to be activated before the other, all current would flow through this one switch and destroy it. The synchronization circuit is actually considered to be part of the timer block, as it will increase the sampling time until all parallel switches are ready (Figure 6). Figure 9 shows the simple synchronization circuit (Figure 9a) and how two parallel NIMBUS chips are connected (Figure 9b): a large connection coming from the solar panel is connected to both source connections of the bypasses and exits from the drain connections. For every two bypasses that need to be synchronized, two connections have to be made.

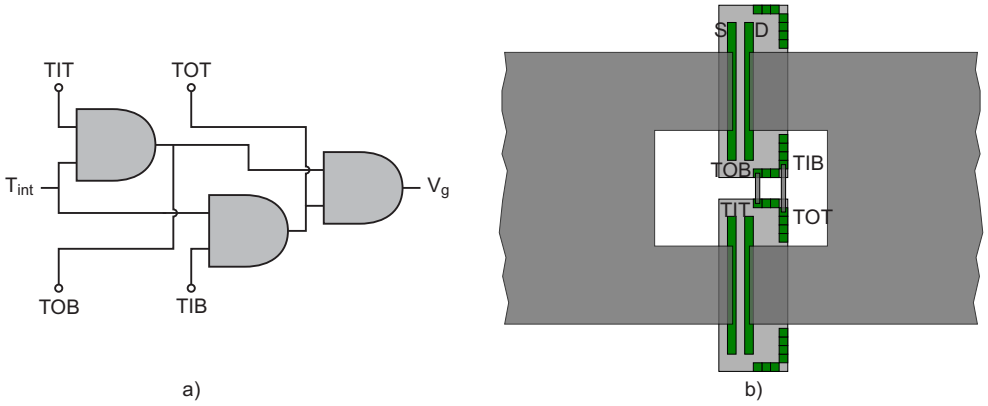


Figure 9. Synchronization circuit: (**a**) schematic and (**b**) chip interconnection.

The synchronization circuit has two external inputs: TIT (Timer In Top) and TIB (Timer In Bottom), and two external outputs: TOT (Timer Out Top) and TOB (Timer Out Bottom). T_{int} is the internal timer signal, which would control the timing if the synchronization circuit were not present (the high signal activates the switch). Parallel NIMBUS chips are connected in such a way that the TOB and TIB pins of the bypass on top are connected to the TIT and TOT pins of the bypass at the bottom, respectively. The input pins that are not connected to anything are default high. The output pins TOT and TOB will be pulled high when both T_{int} and their opposite input pin are high. In the case of a single bypass, this means that T_{int} will directly control V_g ($T_{int} = V_g$). If there are two chips in parallel, the TIT input of the top chip will be (default) high; the TOB output will become high when the T_{int} signal is high, basically notifying the bottom chip that it is ready to activate the switch. The top chip will not activate the switch, though, as long as this TIB signal is not high. The TIB signal of the top chip (connected to the TOT signal of the bottom chip) will become high when the T_{int} signal of the bottom chip (with a default high TIB input) becomes high. This line of reasoning can be extended to more bypasses in parallel (theoretically without limit). Basically, it comes down to all bypasses keeping their V_g signal low until *all* T_{int} signals are high. In reality, there is a small delay between the rise of the T_{int} signal of a certain bypass and the subsequent rise of the V_g signals (and the activation) of the other bypasses. Simulation shows that this delay between two adjacent bypasses is about 1.5 ns. If more bypasses are connected, the total delay will increase, but the later a bypass is activated, the smaller its added value will be: the total on resistance will not change much when the, e.g., tenth bypass is activated. A more crucial factor might be whether the first activated bypass, which carries the full current alone, can handle that current for 1.5 ns. This introduces a practical limit of about 3–4 parallel bypasses (when the maximum load current of 5 A for each bypass is assumed).

3. Power Simulations

In the following section, we will take a closer look at some power simulations. The simulations show a comparison between two module setups: the old setup (three substrings of 20 cells) *versus* the new setup (10 substrings of six cells); and a comparison between different bypass elements: the traditional diode, the NIMBUS chip and an ideal bypass.

3.1. Used Models

The model of a PV cell that was used in these simulations is the simple one-diode model [19] (see Figure 10), with I described as:

$$I = I_{ph} - I_s \left[\exp\left(\frac{V + R_s I}{nkT/q} \right) - 1 \right] - \frac{V + R_s I}{R_p} \quad (1)$$

I_{ph} and I_s are the photovoltaic and saturation current, respectively, q the electron charge, k the Boltzmann constant, T the temperature of the pn junction and n the diode ideality constant. The shunt and parallel resistance have the chosen values of R_s (=1 $\Omega \cdot cm^2$) and R_p (=1 $k\Omega \cdot cm^2$), with a cell size of 225 cm^2. The current density was set to 35 mA/cm^2.

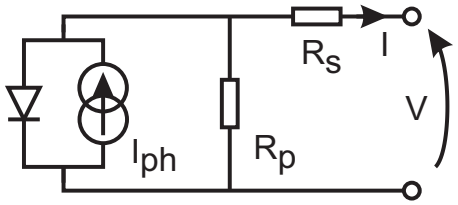


Figure 10. One-diode equivalent circuit of a PV cell.

This results in the cell characteristic shown in Figure 11. The photocurrent (I_{ph}) is 7.88 A when the cell is completely illuminated. The maximum power point (MPP) is located at a voltage of 0.537 V, with a current of 7.38 A, generating a cell power of 3.96 W. A complete solar panel consisting of 60 cells generates under ideal conditions 237.70 W ($I_{MPP} = 7.38$ A, $V_{MPP} = 32.2$ V).

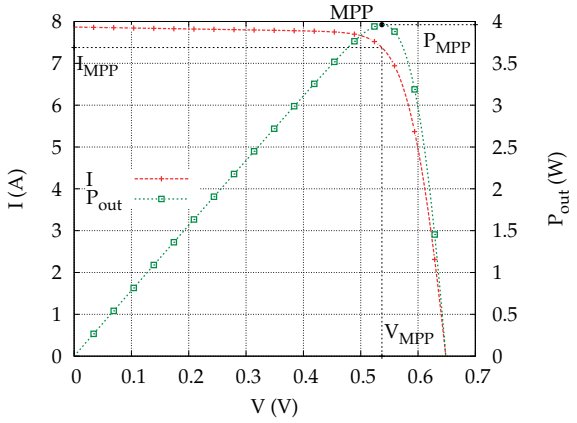


Figure 11. Single cell characteristics.

3.2. Simulations

Since the goal is to see how the panels perform under partial shading, we will examine two shading scenarios: a horizontal shade (parallel to the rows in the panel in Figure 4) and a vertical shade (parallel to the columns in the panel). In each case, the shadow will gradually 'creep' up the panel. A value on

the x axis between zero and one indicates the shading intensity of the first row or column (e.g., a value of 0.5 means the first row (column) has a 50% shade; the other rows (columns) are not shaded). A value 2.7 means that the first and second row (column) are completely shaded; the third row (column) is 70% shaded. The output power at the MPP is than compared to the maximum available power in the panel: the output power if every cell in the panel works at its own MPP. The results are collected in Figures 12 and 13.

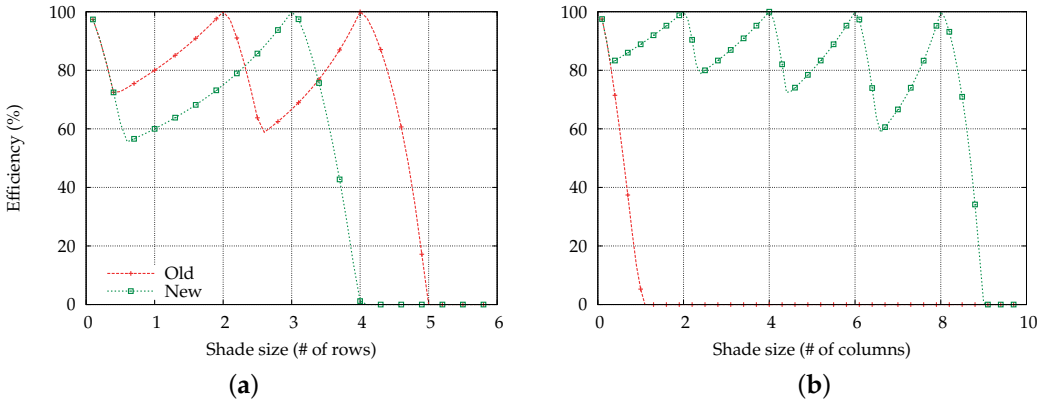


Figure 12. Efficiency comparison between the old and new panel setup under different shading scenarios: (**a**) horizontal shade and (**b**) vertical shade. Values in between the natural numbers on the x axis denote the shading intensity of the next row or column.

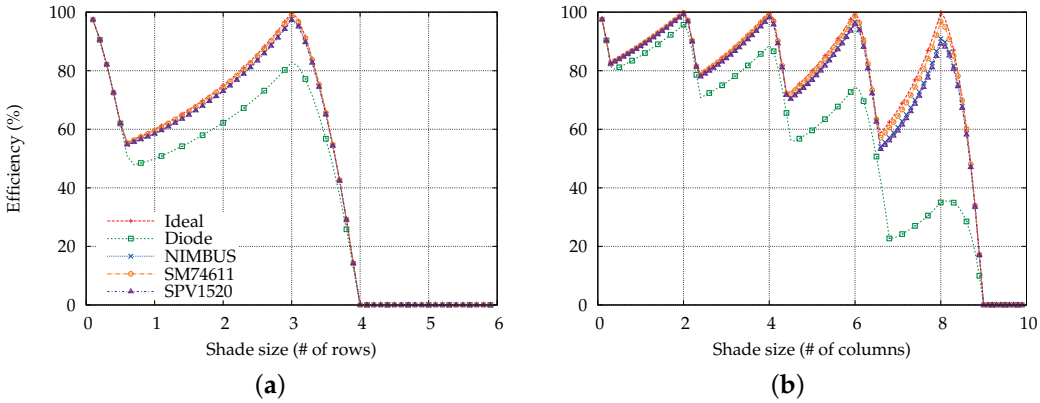


Figure 13. Efficiency comparison between the different bypass elements (ideal bypass, diode bypass, NIMBUS (10 mΩ), SM74611 (Texas Instruments, 3.5 mΩ [20]), SPV1520 (STmicroelectronics, 12 mΩ [21])) under different shading scenarios: (**a**) horizontal and (**b**) vertical. Values in between the natural numbers on the x axis denote the shading intensity of the next row or column.

Figure 12 shows the comparison between the old and new panel setup. In both cases, the bypass element is an "ideal bypass": a switch with an on-resistance of 0 Ω, so no power is lost when the bypass is active. The left side of the figure shows the situation under gradual horizontal shading, the right side under vertical shading. The curves can be explained as follows (e.g., under horizontal shading). When there is no shade ($x = 0$), the efficiency is obviously 100%. All of the power that is available in the panel is seen at the output. When there is some shade on the first row ($0 < x < 0.5$–0.7) the efficiency starts to drop. The shaded cells limit the output current of the other non-shaded cells, lowering the overall output power. At this point, however, the bypass over the substring with the shaded cells is not yet activated, as bypassing the entire string would result in an even lower output power. At $x = 0.5$–0.7, the shaded cells limit the output current so much that it becomes beneficial to activate the bypass. The bypassed substring is completely cut off from the system. The efficiency rises

again because the difference between the power of the panel without that substring and the power of the panel with that substring (that produces less and less power) becomes smaller. When the entire substring is shaded ($x = 2$ in the case of the old setup), there is no difference: an entirely shaded substring produces no power, so it does not matter whether it is bypassed or not. The efficiency is again 100%.

In the case of horizontal shading, the difference between the old and new setup is not that clear. Both have substrings that can be bypassed based on the size and intensity of the shade. Since in this direction, the old panel setup divides the panel into three parts (the three substrings themselves) and the new panel setup divides the panel into just two parts (top five and bottom five substrings), we can assume that the old panel setup will perform slightly better (more divisions generally means a larger 'flexibility' towards different shades). This also comes forward when looking at the average efficiency, taken over the entire x axis. With the old panel setup, this average is about 65.12%, while with the new setup, this is only 47.48%.

The advantage of the new panel setup becomes more clear when looking at the efficiency under vertical shading. Since the old panel setup has only substrings oriented in the horizontal direction, shade on all of the cells in a single column will immediately cause the output power to drop down, without a possibility to bypass the shaded cells. The new panel setup does have this possibility, thus performing much better. The average efficiency of the old panel is only 5.32%, while the new panel can get an average efficiency of 75.14%. It is clear that the new panel setup, due to the smaller, more numerous substrings, is on average better at dealing with different shading scenarios. When the horizontal and vertical shade scenarios are given equal weights, the old panel setup has an average efficiency of 35.22%, while the new panel setup increases this to 61.31%.

In Figure 13 we compared the efficiencies of different bypass elements, using the new panel setup, again looking at both horizontal and vertical shading. The bypass elements compared here are the traditional bypass diode, the ideal bypass, the NIMBUS chip (R_{on} = 10 mΩ, 7.38 A requires two devices in parallel) and two state-of-the-art devices: SM74611 (Texas Instruments, 3.5 mΩ [20]) and SPV1520 (STmicroelectronics, 12 mΩ [21]), which are also discussed in Section 5.1. The benefit of using an active bypass becomes clear. Due to the rather large voltage drop over the bypass diode, a significant portion of the available power is lost. The more substrings are bypassed, the more relevant this loss is. At $x = 8$, the current flows through eight bypasses. With the ideal bypass, the efficiency is 100%, but with the diode bypass, this efficiency is just 35%. The differences between the several active bypasses are less pronounced. In terms of power, SM74611 performs the best, cranking this efficiency up to 96.76%. NIMBUS is next with 90.92%, closely followed by SPV1520 with 89.14%. Table 2 gives an overview of the results of these simulations.

Table 2. Overview of the simulation results (IB: Ideal Bypass; DB: Diode Bypass, NB: NIMBUS; TI: SM74611 [20]; ST: SPV1520 [21]).

	Horizontal Shade				
	Old		New		
η_{avg}	65.12%		47.48%		
	IB	DB	NB	TI	ST
η_{avg}	47.48%	40.92%	46.68%	47.20%	46.52%
lowest local max.	100%	82.91%	97.72%	99.20%	97.26%
	Vertical Shade				
	Old		New		
η_{avg}	5.32%		75.14%		
	IB	DB	NB	TI	ST
η_{avg}	75.14%	57.39%	72.90%	74.35%	72.46%
lowest local max.	100%	35.51%	90.92%	96.76%	89.14%

4. Implementation and Measurements

NIMBUS is implemented in the I3T50 technology from OnSemi. While there are technically no high-voltage components present in the design, we still needed the functionality of the isolated pockets of that technology. A photo of the layout can be seen in Figure 14. The total chip is 7.6 mm long and occupies an area of 10.5 mm^2. The small, long slit in the middle is the NMOS switch with a channel width of 14 cm. The large drain and source contacts are placed as close to the switch as possible. On top are the storage capacitors (C_{timer} = 1.3 nF, C_{DD} = 1 nF, C_{QQ} = 0.3 nF − total area = 2.2 mm^2) and on the bottom the large current diodes. In the top left corner resides the other logic (timer, charge pump, switch control). At the sides, the connections of the synchronization circuit are visible (see also Figure 9), together with some outputs for testing.

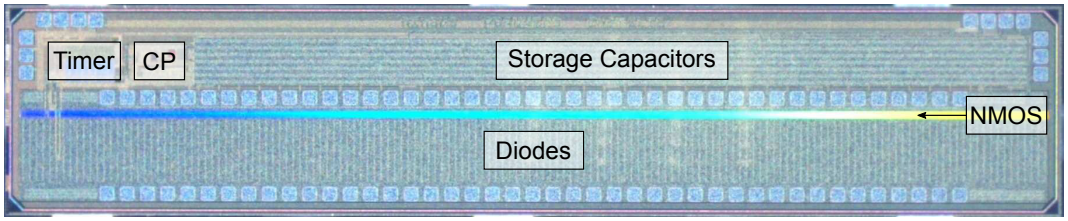


Figure 14. Photo of the NIMBUS chip in the I3T50 technology from OnSemi.

The NIMBUS chips were tested on a PCB where a couple of substrings were emulated using the simple one-diode model of Figure 10, so we could easily control the photocurrents using current sources. With a switch, the current of one of the substrings could be interrupted, simulating a sudden shade, in order to force the current from the other substring through the bypass. Figure 15 shows the measured source voltage (V_S) and the timer voltage (V_{timer}), when the switch was thrown at $t = 0$ s (with I_{ph} = 0.5 A). For $t < 0$, V_S is negative; this is when the substring is generating power. At this time, the V_{timer} capacitor is not yet charged. After the switch is thrown, V_S jumps to about 2.5–3 V, where it stays for a short time (about 200 s) while the charge pump is generating the internal voltages: V_{timer} is charged to 3.3 V. The bypass is activated, and the source voltage now drops to a low voltage and stays there for about one second, while V_{timer} is slowly discharging. When it falls below the PMOS threshold voltage, the timer block deactivates the switch, V_S jumps back to 3 V and the cycle continues.

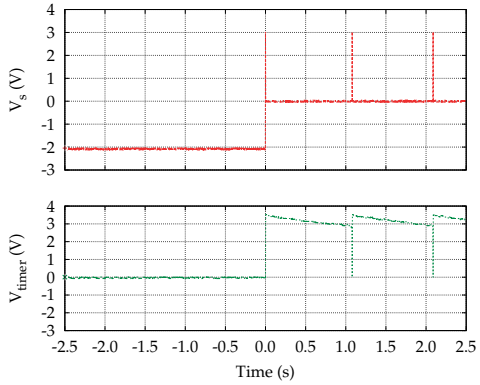


Figure 15. The measured source voltage (V_S) and timer voltage (V_{timer}). The bypass is activated at t = 0 s. The load current is 0.5 A.

The measured on-resistance over the operating current range of the NIMBUS chip is depicted in Figure 16. Both the resistance of a single chip and that of two parallel chips can be seen. The on-resistance in both cases is slightly higher than expected, which is probably due to the heating of the chip under higher load currents. Although the measurements seem to indicate that

the synchronization circuit is fully functional, this was not the case for all chips. Due to the exact implementation of this circuit needed for the "default high" position of the input pins, an unforeseen random variable was introduced, causing some of the synchronization circuits to fail under higher load currents. We assume the increased thermal noise might play a factor.

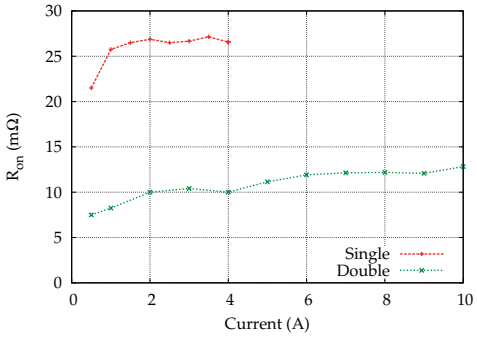


Figure 16. The measured on-resistance over the operating current range of the NIMBUS, for both a single chip and two parallel chips.

5. Discussion

5.1. Comparison with the State-of-the-Art

There are other active bypasses that are very similar to the NIMBUS chip. We can provide some advantages depending on the exact application. The devices we will discuss here are the SM74611 by Texas Instruments [20] and the SPV1520 provided by ST Microelectronics [21,22]. In the datasheets of those devices, we find that the on-resistances of SM74611 and SPV1520 are 3.5 mΩ and 12 mΩ, respectively, with an operating current of about 15 A. A single NIMBUS chip seems to fall somewhat short with its on-resistance of 20 mΩ and maximum current of 5 A. However, thanks to the synchronization circuit, this maximum current can be increased while the on-resistance is decreased. To provide a current of 10 A, two NIMBUS chips can be placed in parallel, and the total on-resistance will be just 10 mΩ, slightly better than the SPV1520. The added synchronization circuit gives extra flexibility that can be used to fit the requirements more closely. Section 3 dug a little deeper into the effects of the differences in on-resistance and how it reflects on the output power of the panel. It appears that even though an on-resistance of 3.5 mΩ *versus* one of 10 mΩ seems like a big difference, the resulting difference in output power is very similar. The use of this synchronization circuit can bring up some valid questions. Is this really needed and why would not the other devices benefit from being placed in parallel? When those (or other, similar devices) are placed in parallel without synchronization, chances are that one of the two (or more) devices will be active first. One of two things can happen: (i) the total current is too high for a single device and the device will break or (ii) the single device can handle the current but in doing so reduces the voltage drop over the other devices so they will not be able to charge up and turn on. On the other hand, it is clear that in order to reduce the on-resistance, more chips are needed, which will increase the cost. A rough estimate was made concerning the cost of the NIMBUS chip when produced at large volumes, and it seems that the cost of two chips in parallel would amount to similar prices as the commercial devices (around $2). For currents up to 5 A, this cost is reduced to a little less than half.

The biggest advantage of the NIMBUS chip is that it is a single chip (up to 5 A) in a common technology (see Section 4). Both SM74611 and SPV1520 are so-called systems-in-package, fitting different components within a single package. While this is irrelevant when looking at a standard application within a solar panel, a single chip will be a lot easier to manage if we want to integrate the active bypass within the panel itself [12] creating a true 'smart solar panel'. The reason why NIMBUS could be kept in a single chip is two-fold. On the one hand, care was taken to avoid large

passives. The low-power design kept the necessary voltage-supply capacitors small enough to be integrated. Large resistors were avoided and, for example, replaced with a subthreshold current source (timer circuit). On the other hand, by creating a floating-bulk NMOS as the main switch, the NMOS's internal parasitic diode is disabled, and current can be blocked under both polarizations of the bypass. Because of this, the current can flow through diodes D_1 to D_3 (Figure 2) when the voltage needs to be pumped up. When this is not the case (as in the SM74611 and SPV1520), the current flows through the internal diode, creating a voltage drop of about 700 mV. To convert this voltage, low-threshold transistors are necessary. In the NIMBUS design, low-threshold transistors are not needed.

5.2. Conclusion and Future

The NIMBUS chip has proven to be a reasonably successful implementation of a "smart bypass", a replacement for the traditional bypass diode to minimize the power loss in a solar panel under partial shading. Although, for a possible next version, we would have to take a closer look at the synchronization circuit in order to make it more robust. Other devices are available that provide the same functionality, but we feel that NIMBUS can provide some benefits in specific cases (e.g., panel integration). Power simulations showed that the performance of NIMBUS is comparable to that of the state-of-the-art. While the first, indoor, controlled tests looked promising, we still need to perform many tests to prove its functionality in the field. NIMBUS will be mounted on a small PCB and plugged into a standard junction box (Figure 17), so that it can be connected to a real solar panel. Those tests can reveal not only whether the chips remain functional in a real outdoor environment, but also what the effective power gain can be under standard lighting conditions with the occasional shadow.

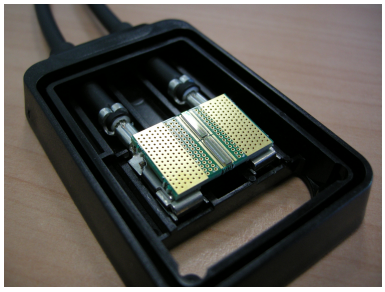


Figure 17. Two parallel NIMBUS chips to be inserted in a standard junction box.

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