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Long Bo, Lijung Huang, Yufei Dai, Youliang Lu, Kil To Chong

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Long Bo [1,2], Lijun Huang [1], Yufei Dai [1], Youliang Lu [3] and Kil To Chong [4,*]

1 School of Mechanical and Electrical Engineering, Institute for Electric Vehicle Driving System and Safety Technology, University of Electronic Science and Technology of China, Chengdu 611731, China; longbo_1978@uestc.edu.cn or longbo1978@hotmail.com (L.B.); jun_uestc@std.uestc.edu.cn (L.H.); dai_yufei@std.uestc.edu.cn (Y.D.)

2 State Key Laboratory of Power Transmission Equipment & System Security and New Technology, Chongqing University, Chongqing 400044, China

3 School of Automation Engineering, University of Electronic Science and Technology of China, Chengdu 611731, China; luyl@uestc.edu.cn

4 Department of Electronics & Information Engineering, Chonbuk National University, Jeonju 567, Korea

* Correspondence: kitchong@jbnu.ac.kr; Tel.: +82-63-270-2478; Fax: +82-63-270-2394

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Abstract: Transformerless grid-connected inverters, due to their advantages of high efficiency, small volume and light weight, have been the subject of more research and interest in recent years. Due to the asymmetrical driving signal in pulse width modulation (PWM) caused by time-delay, zero-drift of the current sensors and imparities of the power transistors, output of the grid current contains dc component. As a result, power quality of the grid is degraded. In this paper, a dc (direct current) component suppression scheme with adaptive back-propagation (BP) neural network proportional-integral-differential (PID) control is proposed for dc component minimization. Moreover, sliding-window-double-iteration-method (SWDIM) is utilized for fast dc component extraction. Compared with the conventional method, the proposed scheme shows better performance, and the dc component can be attenuated to be within 0.5% of the rated current.

Keywords: dc component; power quality; adaptive back-propagation; neural network; grid-connected inverter

1. Introduction

Grid-connected inverter systems are the key facilities for wind turbine generation (WTG), photovoltaic, and fuel cell power generation systems. An ideal output of the grid-connected inverter should only contain ac (alternating current) component. In practice, due to various reasons that lead to the presence of dc components in the system [1–7] such as (1) asymmetries in the switching behavior of power semiconductor devices, (2) existing dc components in the grid, (3) PWM duty-ratio imparities of the gate drivers, (4) turn-ON/-OFF delays on the devices, (5) asymmetries of the power transistors (such as on-state resistance, voltage drop, leakage current, etc.), and (6) dc components from voltage and current sensors, etc., there are some small amounts of dc components in the grid-side current. Since the inherent equivalent resistance of a voltage-source grid-connected inverter is very small, this will cause the saturation of distribution transformers in the grid and result in poor power quality, higher loss, line-frequency power ripple, dc-link voltage ripple and overheating issues in the power system [8,9]. Moreover, power quality of the grid is degraded, as a result, other equipment sharing the same grid may not work properly, and therefore, dc component injection to the grid should be strictly inhibited.

Aiming at resolving the serious power quality problems caused by dc components, many studies have been done to analyze and compare the limits of the dc component injection in the network to evaluate the correct quality criteria [10,11]. However, until now most work has focused on carrying out direct measurements of dc components from PV or wind power generation grid-connected inverters in the ac-side and the problems that can be led by the injection of dc component [12].

Nowadays, some power sectors and non-government organizations (such as IEEE) have set up dc component limitation standards (e.g., IEEE Std.929-2000) to ensure the safety of ac networks. According to the latest survey results, the most restricted standard allowing dc component injection to the grid is 5-mA, other standards rule higher limits as a limitation of 20-mA by distributed generators of less than 16 A-rms per-phase or 1000 mA [13].

To eliminate dc components in grid-connected inverters, ways of finding some solutions on the design of grid-connected inverter have drawn great interest in recent years [14–16]. The latest statistical studies show that the solutions to reduce dc component can be classified into four categories and be summarized in the following viewpoints:

(1) *DC component suppression inverters*. This approach does not change the power circuit topology, and an additional sampling circuit is adopted. In this research area, Sharma first introduced a dc component voltage detection method [17]. A small 1:1 voltage transformer and an RC circuit were used to detect the dc component voltage at the inverter output in the full-bridge grid-connected inverter. The dc component in the grid current was eliminated by feeding back the dc component voltage to the PI controller, yet, this method needs an additional voltage transformer, which will make the hardware system more complex. Alfock and Bowtell continued studying this method by establishing and verifying a mathematical model [18]. He and Xu used a voltage sensor at the inverter output consisting of a differential amplifier and a low-pass filter. DC component detected at the output of the low-pass filter is fed back to the controller. However, experimental results under grid-connected mode were not given. The voltage-detection control method uses sensors to detect the dc component across the ripple filter [19], this method ensures that a very low dc component voltage across the filter, which is sensitive to noise, is measured. Buticchi proposed another dc component detection method [20], however, this method needs a nonlinear inductor. Hence, a customized inductor should be designed according to specific systems.

(2) *Detection and compensation methods*. Guo et al. developed a method to block dc components by using a virtual capacitor [21,22]; however, the dynamic response of the closed-loop control system was affected by the virtual capacitors. The method of applying inverter topology with dc component suppression ability uses inherent structure of the inverter topology, which can prevent dc components from injecting into the grid, e.g., the half-bridge inverter. However, few practical topologies exist. The method of current-detection control uses current sensors to detect the dc component injection, but its effectiveness is limited by the accuracy of sensor due to the inherent significant zero-drift characteristic of Hall-effect current sensors. To solve the zero-drift problems, an auto-calibrating inverter has been proposed by Armstrong [23]. However, this method requires determining the switch state of the H-bridge to measure the inherent zero-drift of the system.

(3) *Use of ac capacitors at the output current path to block the dc components* [24,25]. This will add additional cost and power losses. Moreover, the capacitance must be large enough to get better dc component suppression performance.

(4) *Using an isolation transformer*. This is the simplest way which allows the galvanic isolation and voltage level regulation, yet, the additional fundamental transformer could produce an increase on the inverter's final cost, moreover, its efficiency is reduced, and it is bulky and heavy [26].

From the survey results, much work on dc component suppression has been done. Compared with the scheme using an isolation transformer, ac capacitors or virtual capacitors, the dc component detection and suppression schemes using current sensors are the simplest, most direct and efficient ways, and the main contributions of this paper are summarized as follows:

(1) The influences that will lead to dc components in the grid-connected system are analyzed, including turn-ON/-OFF time-delay, imparities of power transistors, unbalanced grid voltage, scaling errors of sensors.

(2) Different from conventional dc component suppression methods, in this paper, to effectively and timely minimize the dc components in the grid, an adaptive back-propagation BP-PID controller is presented, in which, coefficients of PID controller are adaptively regulated on-line by the output of the BP controller. The proposed scheme combines the merits of two controllers, which show better performance in robustness, self-learning capability, and fast time response.

(3) Sliding-Window-Double-Iteration-Method (SWDIM) [27–29], which has the advantages of easiness, fast implementation and better disturbance rejection capability, is implemented to extract the dc components from the grid-current.

This paper is arranged in four sections. In Section 2, the topology of a three-phase LCL type grid-connected inverter is demonstrated, and how the imparities of power bridge, time-delay on gate driving signals, zero-drift of the sensors and unbalanced grid voltage affect the dc components of the output-current are analyzed. Section 3 gives the proposed dc component minimization control strategy using an adaptive BP-PID controller. The speed learning coefficients of BP-PID controller are automatically regulated. Section 4 demonstrates the simulation and experimental results for the proposed scheme, and suggestions for future research work are also given.

2. Impacts of Time-Delay, Scaling Errors of Sensors, Unbalanced Voltage on Grid Current Performance

2.1. DC Component Injection Analysis

Figure 1 shows the schematic diagram of three-phase grid-connected inverter using P/Q control. With the help of grid voltage e_{ga}, e_{gb} and e_{gc}, the reference grid current (i_{aref}, i_{bref} and i_{cref}) is calculated, e_{ga}, e_{gb} and e_{gc} are the phase-voltage of the grid, respectively. L_a, L_b and L_c are the inverter-side inductance, respectively. L_{ga}, L_{gb} and L_{gc} are the grid-side inductance, respectively. i_{ga}, i_{gb} and i_{gc} are the phase-current of the grid, respectively. v_a, v_b and v_c are the inverter-side output voltage, respectively.

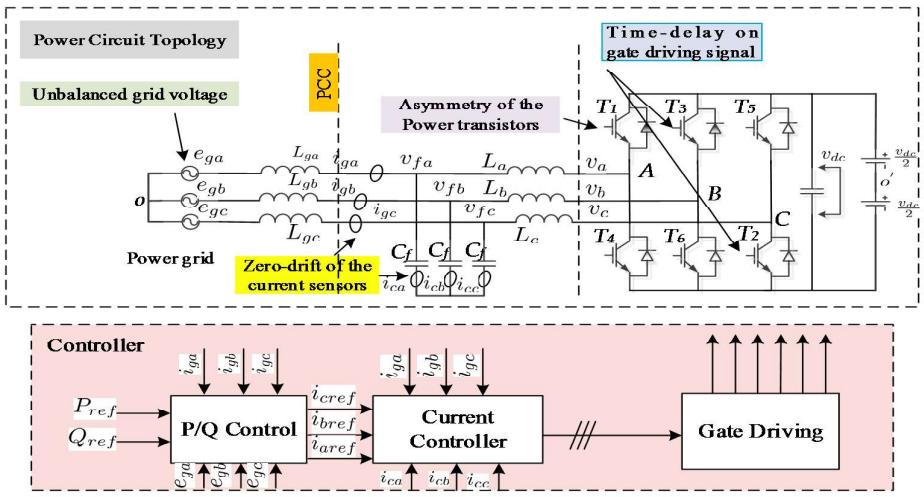


Figure 1. The influences that might cause dc-component at the PCC point of grid-connected converters.

Figure 1 shows the factors that will influence the dc component at the output voltage of grid-connected inverter. The power devices are decentralized, such as non-ideal characteristics of power switching devices (different device turn-ON/-OFF voltage drop), the gate-driving signals are not

symmetrical (time-delay exists), and the zero-drift error (or scaling errors) in current detection circuit varies. The ac-voltage of the grid (e_{ga}, e_{gb} and e_{gc}) are not symmetrical, also due to the noise, the current reference sometimes may contain dc component, this can also cause additional dc component at the output of point of common coupling (PCC).

2.2. DC Component Injection Due to Gate-Driving Delays

In this section, how the dc components are being influenced by device turn-ON/-OFF delays, is analyzed. Taking bipolar PWM modulation as an example, assuming that the average voltage between point O and O' (as shown in Figure 1) in the switching period is $\overline{u}_{OO'}$, the average voltage between point A and O in the switching period is $\overline{u}_{AO}$, and the dc-link-voltage is u_d, the on-time for power transistor VT_1 and VT_4 are t_{on1}, t_{on4}, respectively, T_s is the PWM period.

To simplify the analysis, take phase-A as an example. When power transistor VT_1 switches on, the inverter output voltage $\overline{u}_{AO'} = \frac{u_d}{2}$; when power transistor VT_4 switches off, the inverter output voltage $\overline{u}_{AO'} = -\frac{u_d}{2}$. Therefore, the waveform of $\overline{u}_{AO'}$ is a rectangular wave with an amplitude of $\frac{u_d}{2}$. The inverter voltage output for phase B and C are similar to those of phase A, except that each phase differs of 120°. Line-to-line voltage for u_{AB}, u_{BC} and u_{CA} can be calculated by the following equation.

$$\begin{cases} u_{AB} = u_{AO'} - u_{BO'} \\ u_{BC} = u_{BO'} - u_{CO'} \\ u_{CA} = u_{CO'} - u_{AO'} \end{cases} \tag{1}$$

The inverter output voltage of per-phase is calculated as

$$\begin{cases} u_{AO} = u_{AO'} - u_{OO'} \\ u_{BO} = u_{BO'} - u_{OO'} \\ u_{CO} = u_{CO'} - u_{OO'} \end{cases} \tag{2}$$

Combing (1) with (2), rearrange them to get the following equation.

$$u_{OO'} = \frac{1}{3}(u_{AO'} + u_{BO'} + u_{CO'}) - \frac{1}{3}(u_{AO} + u_{BO} + u_{CO}) \tag{3}$$

Assuming the loads for the grid are symmetrical, and the grid voltage is balanced, which means $u_{AO} + u_{BO} + u_{CO} = 0$, so that the voltage of $u_{OO'}$ in Figure 1 would be

$$u_{OO'} = \frac{1}{3}(u_{AO'} + u_{BO'} + u_{CO'}) \tag{4}$$

In the positive half-cycle of the grid, the average voltage $\overline{u}_{AO'}$ would be

$$\overline{u}_{AO'} = \frac{u_d}{2} \cdot \frac{t_{on1}}{T_s} - \frac{u_d}{2} \cdot \frac{T_s - t_{on4}}{T_s} = i_{ga1} + L \cdot \frac{di_{ga1}}{dt} + u_{ga} + u_{OO'} \tag{5}$$

Solving this first-order differential equation to get the grid-connected current as

$$\begin{aligned} \bar{i}_{ga1} &= \int_0^{\frac{T_s}{2}} \frac{u_d}{2LT_s} \cdot (t_{on1} - T_s + t_{on4})dt - \frac{1}{L}\int_0^{\frac{T_s}{2}} u_{ga}dt - \frac{1}{L}\int_0^{\frac{T_s}{2}} u_{OO'}dt \\ &= \frac{u_d}{4L} \cdot (t_{on1} - T_s + t_{on4}) - \frac{1}{L}\int_0^{\frac{T_s}{2}} u_{ga}dt - \frac{1}{L} \cdot \frac{1}{6}u_d \cdot \frac{1}{6}T_s \\ &= \frac{u_d}{4L} \cdot (t_{on1} - T_s + t_{on4}) - \frac{1}{L}\int_0^{\frac{T_s}{2}} u_{ga}dt - \frac{1}{36L}u_d T_s \end{aligned} \tag{6}$$

Similarly, in the negative half-cycle of the ac grid, the average voltage $\overline{u}_{AO'}$ is

$$\overline{u}_{AO'} = \frac{-u_d}{2} \cdot \frac{t_{on4}}{T_s} + \frac{u_d}{2} \cdot \frac{T_s - t_{on1}}{T_s} = i_{ga2} + L \cdot \frac{di_{ga2}}{dt} + u_{ga} + u_{OO'} \tag{7}$$

Solving the first-order differential Equation (7) to get the grid-connected current

$$\begin{aligned}\bar{i}_{ga2} &= \int_0^{\frac{T_s}{2}} \frac{u_d}{2LT_s}\cdot(-t_{on4}+T_s-t_{on1})dt - \frac{1}{L}\int_0^{\frac{T_s}{2}} u_{ga}dt - \frac{1}{L}\int_0^{\frac{T_s}{2}} u_{OO'}dt \\ &= \frac{u_d}{4L}\cdot(-t_{on1}+T_s-t_{on4}) - \frac{1}{L}\int_0^{\frac{T_s}{2}} u_{ga}dt + \frac{1}{L}\cdot\frac{1}{6}u_d\cdot\frac{1}{6}T_s \\ &= \frac{u_d}{4L}\cdot(-t_{on1}+T_s-t_{on4}) - \frac{1}{L}\int_0^{\frac{T_s}{2}} u_{ga}dt + \frac{1}{36L}u_dT_s\end{aligned} \tag{8}$$

Combining (6) with (8), the grid-current i_{ga} under normal state would be

$$i_{ga} = \bar{i}_{ga1} + \bar{i}_{ga2} = -\frac{1}{L}\int_0^{T_s} u_{ga}dt - \frac{1}{L}\int_0^{T_s} u_{OO'}dt = -\frac{1}{L}u_{ga}T_s \tag{9}$$

Assuming that in the positive and negative half-cycle of the ac-grid, there are time-delays Δt_1 and Δt_4 in the driving signal, the average voltage in (5) can be written as (10), and the average voltage in (7) can be written as (11).

$$\overline{u}_{AO'} = \frac{u_d}{2}\cdot\frac{t_{on1}+\Delta t_1}{T_s} - \frac{u_d}{2}\cdot\frac{T_s-t_{on4}-\Delta t_1}{T_s} = i_{ga1} + L\cdot\frac{di_{ga1}}{dt} + u_{ga} + u_{OO'} \tag{10}$$

$$\overline{u}_{AO'} = \frac{-u_d}{2}\cdot\frac{t_{on4}+\Delta t_4}{T_s} + \frac{u_d}{2}\cdot\frac{T_s-t_{on1}-\Delta t_4}{T_s} = i_{ga2} + L\cdot\frac{di_{ga2}}{dt} + u_{ga} + u_{OO'} \tag{11}$$

Hence, in the positive half-cycle of the ac-grid, the grid-side current i_{ga1} is

$$\begin{aligned}\bar{i}_{ga1} &= \int_0^{\frac{T_s}{2}} \frac{u_d}{2LT_s}\cdot(t_{on1}+2\Delta t_1-T_s+t_{on4})dt - \frac{1}{L}\int_0^{\frac{T_s}{2}} u_{ga}dt - \frac{1}{L}\int_0^{\frac{T_s}{2}} u_{OO'}dt \\ &= \frac{u_d}{4L}\cdot(t_{on1}-T_s+t_{on4}+2\Delta t_1) - \frac{1}{L}\int_0^{\frac{T_s}{2}} u_{ga}dt - \frac{1}{36L}u_dT_s\end{aligned} \tag{12}$$

In the negative half-cycle of the ac-grid, the grid-side current i_{ga2} is

$$\begin{aligned}\bar{i}_{ga2} &= \int_0^{\frac{T_s}{2}} \frac{u_d}{2LT_s}\cdot(-t_{on4}-2\Delta t_1+T_s-t_{on1})dt - \frac{1}{L}\int_0^{\frac{T_s}{2}} u_{ga}dt - \frac{1}{L}\int_0^{\frac{T_s}{2}} u_{OO'}dt \\ &= \frac{u_d}{4L}\cdot(-t_{on1}+T_s-t_{on4}-2\Delta t_4) - \frac{1}{L}\int_0^{\frac{T_s}{2}} u_{ga}dt + \frac{1}{36L}u_dT_s\end{aligned} \tag{13}$$

Combing (12) with (13), the grid-current i_{ga} considering the time-delay Δt_1 and Δt_4 would be

$$i_{ga} = \bar{i}_{ga1} + \bar{i}_{ga2} = \frac{u_d}{2L}(\Delta t_1 - \Delta t_4) - \frac{1}{L}u_{ga}T_s \tag{14}$$

Equation (14) demonstrates that if there are any asymmetries on the device turn-ON/-OFF delays, the grid-connected current i_{ga} will change. If the time-delay of power transistor VT_1 and VT_4 are the same, $\Delta t_1 = \Delta t_4$, there will be no dc component in the output current.

2.3. DC Component Analysis Due to Zero-Drift and Scaling Error of Current and Voltage Sensors

In grid-connected converters, the current or voltage sampling for grid-side current is necessary, yet, zero-drift current and scaling errors exist in current and voltage sensors. Figure 2 illustrates the control diagram of LCL-type grid-connected system, the grid and capacitor current are usually adopted as the current feedbacks. According to the closed-loop control diagram, a system block diagram of the grid-connected current in the stationary frame can be established. The result shows that if there are any dc components in the sensors, after been amplified by the current controller, the inverter-side output voltage will contain dc components.

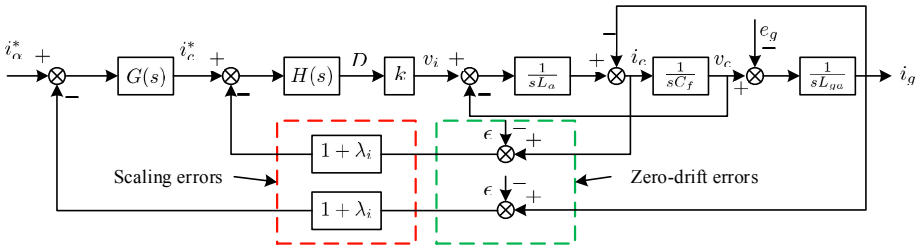


Figure 2. Closed-loop control diagram of LCL-type grid-connected inverter considering zero-drift and scaling error.

Therefore, how to eliminate the influences caused by zero-drift or scaling errors in current sensors are the key issues. Assuming all the sensors have the same scaling error coefficient λ_i and zero-drift offset ϵ, the grid-current i_{ga} would be:

$$i_{ga}(s) = \frac{kG(s)H(s)i_a^* + e_{ga}(s)s^2C_fL_a + 2\epsilon kG(s)H(s)}{s^3C_fL_aL_{ga} + s(L_a + L_{ga}) + kH(s)(1+\lambda_i)(G(s) + L_{ga}C_fs^2)} \tag{15}$$

To simplify (16) for analysis, the influence of the controllers is ignored by considering $G(s) = H(s) = 1$. In the stationary coordinate, the reference current for phase-A can be written as $i_a^*(s) = \frac{I_m w_0}{s^2+w_0^2}$ in frequency domain. In the formula mentioned, I_m is the amplitude of the three-phase reference current and w_0 is the line angular frequency. When $s = 0$, the grid current at zero frequency $i_{ga}(0)$ represents the dc component:

$$i_{ga}(0) = \frac{i_a^*}{1+\lambda_i} + 2\epsilon = \frac{I_m}{w_0(1+\lambda_i)} + 2\epsilon \tag{16}$$

According to (17), dc component in phase-B and phase-C are similar with phase-A. Since all sensors have the same zero-drift current Δi, a differential elimination method is put forward to eliminate the zero-drift current, the output current is defined by:

$$\begin{cases} i_{ga} = i_{ga0} + \Delta i \\ i_{gb} = i_{gb0} + \Delta i \\ i_{gc} = i_{gc0} + \Delta i \\ i_{ga0} + i_{gb0} + i_{gc0} = 0 \end{cases} \tag{17}$$

Since, the grid-connected inverter is star-connected, from (18), the feedback grid current i_{ga0}, i_{gb0} and i_{gc0} without zero-drift can be derived as:

$$\begin{cases} i_{ga0} = \frac{1}{3}(2i_{ga} - i_{gb} - i_{gc}) \\ i_{gb0} = \frac{1}{3}(-i_{ga} + 2i_{gb} - i_{gc}) \\ i_{gc0} = \frac{1}{3}(-i_{ga} - i_{gb} + 2i_{gc}) \end{cases} \tag{18}$$

From (19), the dc component caused by zero-drift in current sensors can be effectively eliminated using this differential method.

2.4. DC Component Analysis Due to the Asymmetries of Power Transistors

In an LCL-type grid-connected system, the power transistors do not always have the same characteristics, such as state-on resistance, hence the voltage drop is different, this section will analyze how dc components are affected due to the asymmetries of power transistors.

Assuming the voltage-drop of power device VT_1 and VT_4 are Δu_{t1} and Δu_{t4} respectively, t_{on1} and t_{on4} are the device on-time for VT_1 and VT_4, respectively. In the positive half-cycle of the grid, the average voltage $\overline{u}_{AO'}$ would be:

$$\overline{u}_{AO'} = \frac{u_d - \Delta u_1}{2} \cdot \frac{t_{on1}}{T_s} - \frac{u_d - \Delta u_4}{2} \cdot \frac{T_s - t_{on4}}{T_s} = i_{ga1} + L \cdot \frac{di_{ga1}}{dt} + u_{ga} + u_{OO'} \tag{19}$$

Similarly, in the negative half-cycle of the ac-grid, the average voltage output $\overline{u}_{AO'}$ would be:

$$\overline{u}_{AO'} = -\frac{u_d - \Delta u_4}{2} \cdot \frac{t_{on4}}{T_s} + \frac{u_d - \Delta u_1}{2} \cdot \frac{T_s - t_{on1}}{T_s} = i_{ga2} + L \cdot \frac{di_{ga2}}{dt} + u_{ga} + u_{OO'} \tag{20}$$

Hence, combining (20) and (21), the relation between grid-side current i_g and device on-time of $t_{on1}(VT_1)$ and $t_{on4}(VT_4)$ would be:

$$\begin{aligned} i_{ga} &= \tfrac{1}{L}\textstyle\int_0^{T_s} (\overline{u}_{AO'} - u_{ga} - u_{OO'})dt = \tfrac{1}{L}\int_0^{\frac{T_s}{2}} (\overline{u}_{AO'} - u_g u_{OO'})dt + \tfrac{1}{L}\int_{\frac{T_s}{2}}^{T_s} (\overline{u}_{AO'} - u_g u_{OO'})dt \\ &= \tfrac{1}{4}[\Delta u_1(2t_{on1} - T_s) + \Delta u_4(2t_{on4} - T_s)] - \tfrac{1}{L} u_{ga} T_s \end{aligned} \tag{21}$$

Formula (22) indicates that if the power transistors do not always have the same characteristics, the grid-connected current will contain dc components, which is decided by the voltage-drop of power transistors.

2.5. DC Component Analysis Due to Unbalanced Grid Voltage

In utility, the operation of the PWM inverter may suffer from a short circuit fault, especially an asymmetrical short-circuit fault, which will make the phase voltage of the grid unbalanced and may further cause dc component in the grid-connected current. Unbalanced grid voltage consists of under-voltage and over-voltage imbalance. Assuming that the voltage fluctuations for three-phase coefficients are symbolize as λ_a, λ_b and λ_c respectively, the grid voltage will be:

$$\begin{cases} u_{ga} = u_{ga0}(1 + \lambda_a) \\ u_{gb} = u_{gb0}(1 + \lambda_b) \\ u_{gc} = u_{gc0}(1 + \lambda_c) \end{cases} \tag{22}$$

In (23), assuming the grid voltage for u_{ga0},u_{gb0} and u_{gc0} are symmetrical and balanced, which means $u_{ga0} + u_{gb0} + u_{gc0} = 0$. Also, assuming the loads are symmetrical, as a result, the sum of load voltage $u_{LRa} + u_{LRb} + u_{LRc} = 0$, then the voltage $u_{OO'}$ will be written as:

$$u_{OO'} = \frac{1}{3}(u_{AO'} + u_{BO'} + u_{CO'}) - \frac{1}{3}(u_{ga} + u_{gb} + u_{gc}) \tag{23}$$

Considering (6), (8), (23) and (24), the grid-current i_{ga} considering unbalanced grid voltage is:

$$i_{ga} = \bar{i}_{ga1} + \bar{i}_{ga2} = -\tfrac{1}{L}\textstyle\int_0^{T_s} u_{ga}dt - \tfrac{1}{L}\int_0^{T_s} u_{OO'}dt = -\tfrac{T_s}{L}u_{ga0} + \tfrac{T_s}{3L}(-2u_{ga0}\lambda_a + u_{gb0}\lambda_b + u_{gc0}\lambda_c) \tag{24}$$

The result shows that if there is any unbalanced grid voltage, the grid-connected current will contain dc components, which are decided by the fluctuation coefficients (λ_a, λ_b and λ_c) of the voltage sensors.

2.6. DC Component Extraction Algorithm Using SWDIM

To realize dc component suppression, it is necessary to extract the dc component from the grid current. In this paper, a novel method to acquire dc components named SWDIM is proposed. Fundamental frequency component and harmonic component detection are presented.

Assuming the grid-connected current i_g can be written as:

$$i_g(t) = i_{dc} + i_{ac} = i_{dc} + \sum_{i=1\cdot\cdot L} i_n \cdot sin(2\pi n f_1 t + \varphi_n) \tag{25}$$

In (26), i_{dc} is the dc component of the grid current, i_{ac} is the ac component of the grid current. i_n,nf_1, φ_n are the amplitude, frequency and phase-angle of the ac signal, respectively, the integration result for i_g is written in (27) as:

$$i_a = \frac{1}{T}\int_{t_0}^{t_0+T} i_g dt = i_{dc} + \frac{1}{T}\sum_{n=1\cdot\cdot L} \frac{i_n}{n\pi f_1} sin(n\pi f_1 T) sin(2\pi n f_1 t + \phi_n + n\pi f_1 T) \tag{26}$$

Obviously, considering $T = 1/f_1$, the second component of (27) is 0, the dc component is determined by:

$$i_a = \frac{1}{T}\int_{t_0}^{t_0+T} i_g dt = \frac{1}{T}\int_{t_0}^{t_0+T} (i_{dc}(t) + i_n sin(2\pi n f_1 t + \phi_n))dt = i_{dc} \tag{27}$$

From the above analysis in (28), a conclusion can be made that even if there is a large current when $T = 1/f_1$, high accuracy dc component estimation can still be achieved. In a utility, the ac frequency usually varies within a certain area, which degrades the performance of the proposed method. Considering $T = 1/f_0$ and $f_0 \neq f_1$, the integration result for grid current $i_g(t)$ is given by:

$$\begin{array}{l} i_a = \frac{1}{T}\int_{t_0}^{t_0+T} i_g dt = \frac{1}{T}\int_{t_0}^{t_0+T} (i_{dc}(t) + i_n sin(2\pi n f_1 t + \phi_n))dt \\ = i_{dc} + \sum\limits_{n=1\cdot\cdot L} \frac{f_0 I_n}{n\pi f_1} sin(\frac{n\pi f_1}{f_0}) sin(2\pi n f_1 t_0 + \phi_n + \frac{n\pi f_1}{f_0}) \end{array} \tag{28}$$

From (29), the estimation error for dc component contains ac components, the amplitude is $\frac{f_0 I_n}{n\pi f_1} sin((n\pi f_1)/f_0)$. It has to be noted that, if the difference between f_0 and f_1 is small, the value of $sin(n\pi f_1/f_0)$ would also be very small. To overcome the limitations caused by frequency drift, double integration for the grid current can be accomplished. The result is shown in (30):

$$\begin{array}{l} i_a = \frac{1}{T^2}\int_{t_0}^{t_0+T} (\int_{t_0}^{t_0+T} i_g dt)dt = \frac{1}{T^2}\int_{t_0}^{t_0+T} (\int_{t_0}^{t_0+T} (i_{dc} + i_n sin(2\pi n f_1 t + \phi_n))dt)dt \\ = i_{dc} + \sum\limits_{n=1,2,\cdot\cdot L} (\frac{f_0 I_n}{n\pi f_1} sin(\frac{n\pi f_1}{f_0}))^2 i_n sin(2\pi n f_1 t_0 + \phi_n + \frac{n\pi f_1}{f_0}) \end{array} \tag{29}$$

From (30), it can be clearly seen that the dc component estimation still exists, however, the estimation error is much smaller than that in (30). This is explained in (31) as:

$$[\frac{f_0}{n\pi f_1} sin(\frac{n\pi f_1}{f_0})]^2 \approx [\frac{1}{n\pi} sin(\frac{n\pi f_1}{f_0})]^2 \tag{30}$$

The frequency error between fundamental frequency f_0 and drift-frequency f_1 is much smaller than the estimation error shown in (32):

$$\frac{f_0 I_n}{n\pi f_1} sin(\frac{n\pi f_1}{f_0}) \approx \frac{1}{n\pi} sin(\frac{n\pi f_1}{f_0}) \tag{31}$$

It can be proved that through many times of integration, the steady-state error can be greatly minimized. However, the more integration times implemented, the slower the time response for dc component suppression will be. In utility, considering the time response requirements, double integrations can satisfy our requirements.

3. Proposed DC Component Suppression Scheme with Adaptive BP-PID Controller

Some conventional dc component suppression scheme studies adopt a PID controller. Its coefficients are usually fixed, which is not suitable for dynamic reference, and sometimes unsuitable parameter specification will cause the instability of the system. To minimize the dc components, as well as low harmonic distortions in grid current, adaptive back-propagation (BP) neural network, which has the advantages of strong adaptation, self-learning capability and on-line parameter regulation capability, has been put forward, the proposed scheme combines the merits of the two controllers, which could achieve better performance to minimize the dc component.

3.1. DC Component Suppression Scheme with Adaptive BP-PID Control

To effectively realize dc component suppression and based on the analysis in Section 2 of how the dc component is generated, an intelligent control algorithm that utilizes an adaptive BP-PID control algorithm is illustrated in Figure 3, where the reference current is composed by two parts, one for the quasi-proportional resonance (QPR) current controller for closed-loop current tracking and the other part is composed by the output of the dc component suppression controller. The coefficients of PID controller in dc-suppression are regulated in a timely way by the output of an adaptive BP neural network.

PSIM 9.1 and VS2010 are utilized to accomplish the co-Simulink work. The control algorithm is written in C-language. The power circuit topology is set up in PSIM.

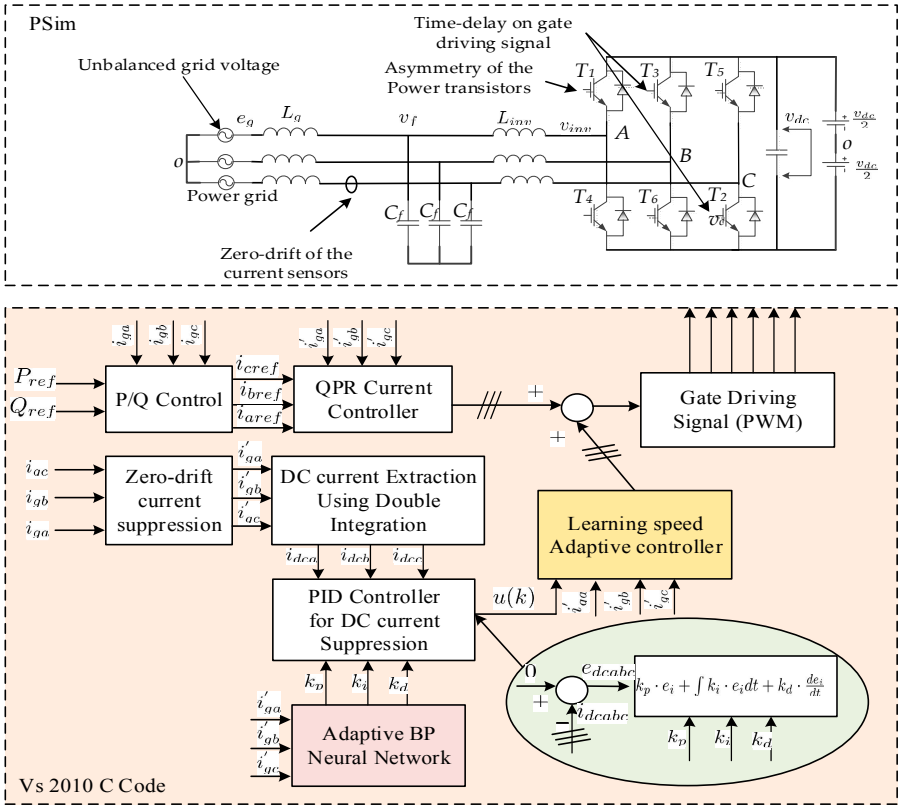


Figure 3. Block diagram of the proposed adaptive BP-PID controller for dc component suppression.

As shown in Figure 3, the implementation of the proposed suppression control scheme contains three steps:

(1) DC component extraction method using double integrations. This block is used for fast dc component extraction.
(2) Adaptive BP neural network, which is used to optimize the coefficients (k_p, k_i and k_d) of PID controller, so that the dc components can always be minimized.
(3) BP-PID controller for dc component suppression with coefficients of PID controller that are automatically updated through the output of the adaptive BP neural network.

The implementation flowchart of BP-PID controller used in the simulation is illustrated in Figure 4. Firstly, to eliminate dc components caused by zero-drift of the sensors, usually, the current sensors of the inverter, by its nature, have zero drift or scaling errors when they receive a symmetrical sine wave. The output signal has a dc component. If the dc component is positive, after being corrected by a current loop controller, the correction loop causes the output of inverter producing a corresponding negative dc component, and vice versa. Using this theory, the output control method for dc components can be eliminated.

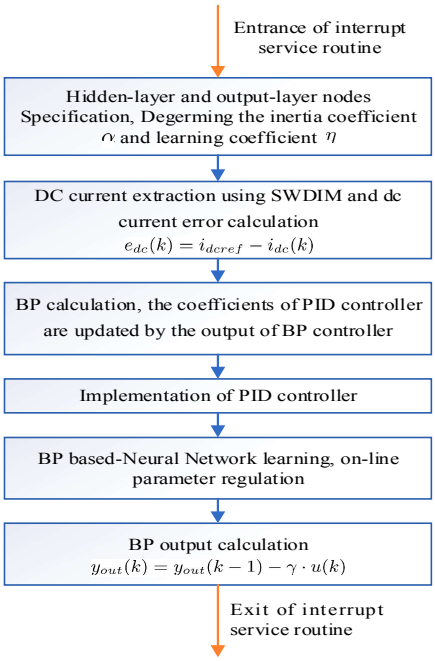


Figure 4. Implementation flowchart diagram of adaptive BP-PID controller.

3.2. *Adaptive Speed Learning BP-PID Controller Design*

In Figure 5, γ is defined as the learning speed of $u(k)$. The core objective of the adaptive BP-PID controller for dc component suppression is to find the most appropriate coefficient γ to minimize the dc component.

Assuming that there is a limitation for the difference e_{dc} between reference dc component i_{dcref} and feedback dc component i_{dcfd}, when the absolute value of dc component $|de_{dc}(k)| \leq err_{max}$ varies within a very small range, the control output $u(k)$ should maintain its previous value. When the absolute values of the dc component are greater than the differential error, which means that the error is relatively bigger, it is needed to consider the regulation steps of the control output variable. Figure 5 illustrates the implementation flowchart based on the above analysis.

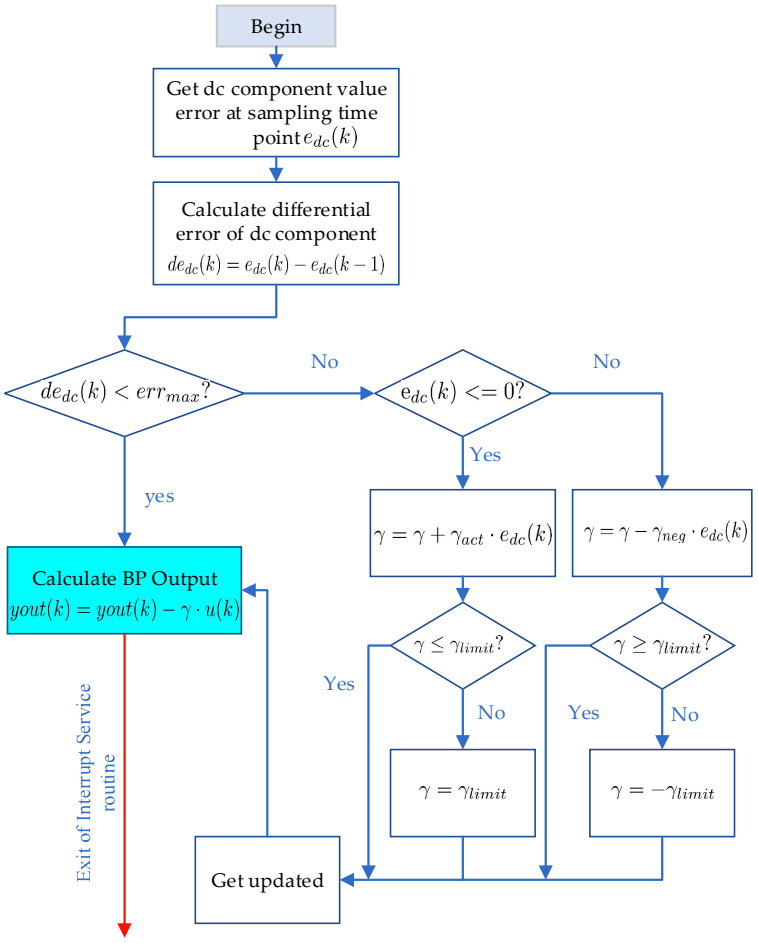


Figure 5. Implementation flowchart of adaptive speed learning coefficient regulation method for BP neural network.

4. Simulation Results

To validate the correctness of the proposed system, simulation verifications were performed. The simulation verification contains two steps: (1) design of an LCL filter, (2) implementation of the proposed dc component suppression scheme.

4.1. Parameter Design of an LCL Filter

4.1.1. Inverter-Side Inductance Calculation of LCL-Filter

According to the theoretical analysis [27], the expressions for maximum inverter-side inductance is:

$$L_{1max} = \frac{\lambda v_{L1} V_g}{\omega_0 I_1} \tag{32}$$

where in (33), V_g is the grid voltage, $I_1 = \frac{P_e}{3V_g}$ is the rated current of the inverter, ω_0 is the angular frequency of the grid, λ_{vL1} is the ratio between the RMS value of inverter-side inductance and filter capacitance C_f, which is usually selected as 0.05. In the proposed scheme, set $V_g = 220$ V, $I_1 = \frac{P_e}{3V_g} = 3.03$ A, $\omega_0 = 100\pi$ and $\lambda_{vL1} = 0.05$, L_{1max} can be calculated as 11.6 mH.

Similarly, the expression for minimum inverter-side inductance is:

$$L_{1min} = \frac{V_{in} T_{sw}}{8 \lambda_{cL1} I_1} \tag{33}$$

where in (34), V_{in} is the dc-link voltage of the inverter, T_{sw} is the switching frequency of the transistors, $I_1 = \frac{P_e}{3V_g}$ is the RMS value of fundamental current, λ_{cL1} is the ripple coefficient of inverter-side inductance output current, which is usually chosen as 0.2~0.3. Set $V_{in} = 700$ V, $T_{sw} = 50k$, $I_1 = \frac{P_e}{3V_g} = 3.03$ A and $\lambda_{cL1} = 0.3$, L_{1min} can be calculated as 1.9 mH. As a result, considering the volume and efficiency of the inverter, the inverter-side inductance of the LCL filter is chosen as $L_1 = 2$ mH.

4.1.2. Capacitance Calculation of LCL-Filter

The capacitance of C_f in LCL-filter will influence the reactive power. Large capacitance will increase the reactive power and the inverter-side current, moreover, switching power loss of power transistors will increase, corresponding. The expression for inverter-side capacitor is [28]:

$$C_{max} = \lambda_C \frac{P_e}{\omega_0 V_g^2} \tag{34}$$

where in (35), C_{max} is the maximum allowable capacitance, λ_C is the ratio between the reactive power introduce by capacitance and the rated power output of grid-connected inverter, which is usually chosen as $\lambda_C = 5\%$. As a result, the maximum allowable capacitance in three-phase grid connected system is calculated as 2.19 μF. As a result, the filter capacitance C_f is chosen as 2.2 μF in experiment.

4.1.3. Grid-Side Inductance Calculation of LCL-Filter

When the inverter-side and filter capacitance are specified, the grid-side inductance is usually chosen according to the standards in IEEE Std.929-2000 and IEEE Std-2003. The expression for minimum grid-side inductance is shown as [29]:

$$L_2 = \frac{1}{2\pi f_{sw} \left| \frac{i_g}{v_i} \right|^2 \left| 1 - \frac{f_{sw}}{f_r} \right|^2} \tag{35}$$

where in (36), f_{sw} is the switching frequency of power transistor, f_r is the frequency of carrier signal, $\frac{i_g}{v_i}$ is the ratio between grid current and inverter-side voltage. Similar with the former calculation method, the grid-side inductance is calculated by (36) as $L_2 = 1.08$ mH, as a result, an approximate grid inductance with $L_2 = 1$ mH is utilized in the experiment.

4.2. Implementation of the Proposed DC Suppression Scheme

The control algorithm is written in C code in VS2010, the simulation setup is shown in Figure 3. Table 1 shows the parameter specifications.

Table 1. Parameter specifications in the simulation.

Component	Parameter	Value
Grid	Grid voltage (line to line)	380 V_{rms}
	Grid frequency f	50 H_z
	DC-link voltage V_{dc}	600 V
	Switching frequency f_{sw}	50 kH_z
	Grid-side inductance L_g	1 mH
	Inverter-side inductance L_{inv}	2 mH
	Capacitance of LCL filter C_f	2.2 μF

To demonstrate how dc-component are minimized, dc-components of 1.5-A in phase-A, −0.5-A in phase-B and −1-A in phase-C are given as the initial existing dc-component, respectively. The SPWM modulation technique is implemented in a current closed-loop. DC component suppression comparisons results between PID and adaptive BP-PID controller are illustrated. The comparisons are performed by the following steps:

(1) Before 0.04 s, the inverter operates in grid-connected mode without suppression. The current closed-loop with conventional PID controller is implemented. The dc components of phase-A, Phase-B, and Phase-C using SWDIM are shown, respectively.
(2) When the simulation time t (0.1 s $<$ t $<$ 0.2 s), dc component suppression using the conventional PID controller is implemented.
(3) When (t $>$ 0.2 s), dc component suppression control using the proposed BP-PID controller is implemented.

To demonstrate that the proposed scheme has better performance in dc component suppression than a conventional PID controller, Figures 6–8 show the grid current, grid voltage and dc component waveforms of the inverter with/without dc suppression loops under different active power reference conditions.

(1) Given the reference active power $P = 1.2$ kW, when t = 0.1 s, dc component suppression using a conventional PID controller is implemented. The average dc component is approximately 988 mA, −296 mA, and −693 mA, respectively. When t = 0.2 s, the dc suppression loop using an adaptive BP-PID controller is implemented. After about 1.5-line cycles, the dc suppression effects become stable, and the average dc components are approximately −109, 31, and 78 mA, respectively. Compared with a conventional PID controller, the adaptive BP-PID controller reduces the dc component value by 73.17%, 65.37% and 77.07%, respectively.
(2) Given the reference active power $P = 3.6$ kW, when t = 0.1 s, dc component suppression using a conventional PID controller is implemented. The average three-phase dc component is approximately 1050, −258, and −793 mA, respectively. When t = 0.2 s, the dc suppression loop of the adaptive BP-PID controller is implemented. After about 1.5-line cycles, the dc suppression effects become stable, and the average three-phase dc components are approximately 37, 5, and −42 mA, respectively. Compared with conventional PID controller, the adaptive BP-PID controller reduces the three-phase dc component values by 67.56%, 52.52% and 75.08%, respectively.
(3) Given the reference active power $P = 6.0$ kW, when t = 0.1 s, dc component suppression using a conventional PID controller is implemented. The average dc components are approximately 1037, −258 and −780 mA, respectively. When t = 0.2 s, the dc suppression loop of the adaptive BP-PID controller is implemented. After about 1.5-line cycles, the dc suppression effects become stable, and the average three-phase dc components are approximately 66, 8 and −74 mA, respectively. Compared with the conventional PID controller, the adaptive BP-PID controller reduces the dc component values by 64.75%, 53.29% and 70.48%, respectively.

From Figures 6–8, when given different active power, the adaptive BP-PID controller algorithm can eliminate the dc component in a short time, and the steady state value is close to 0, which proves that the adaptive BP-PID controller used is superior to the traditional PID controller in dc component suppression.

Taking Figure 7 as an example for analysis: when the active power reference $P = 3.6$ kW, it can be seen from Figure 7a,b that the grid-connected current obviously contains a dc-offset compared with the standard sinusoidal wave without dc-suppression control. The waveform of phase A is shifted upward and the phase B and phase C waveforms are shifted downward, indicating that the grid-connected current contains dc components.

The three-phase dc components are about 1.5, −0.5, and −1 A, respectively, which proves that the sliding window integration method can accurately extract the dc signals. When t = 0.1 s, the dc

suppression loop with traditional PID controller is implemented. The grid-connected current still have large offsets, and the dc component exhibits periodic fluctuations. Although the dc component of the grid-connected current is suppressed, the suppression effect is not ideal. The dc suppression loop with adaptive BP-PID controller is put into operation at 0.2 s. The grid-connected current of the system enters a steady state after a short time, and the grid current does not contain any dc-offset. At this time, the dc component is close to 0, indicating that the dc component in the grid-connected current is minimized. From Figure 7c, taking phase-A as an example, the grid-connected current and voltage of the inverter are in phase when the system adopts a dc suppression loop with a conventional PID controller or an adaptive BP-PID controller. The grid current can still be well tracked.

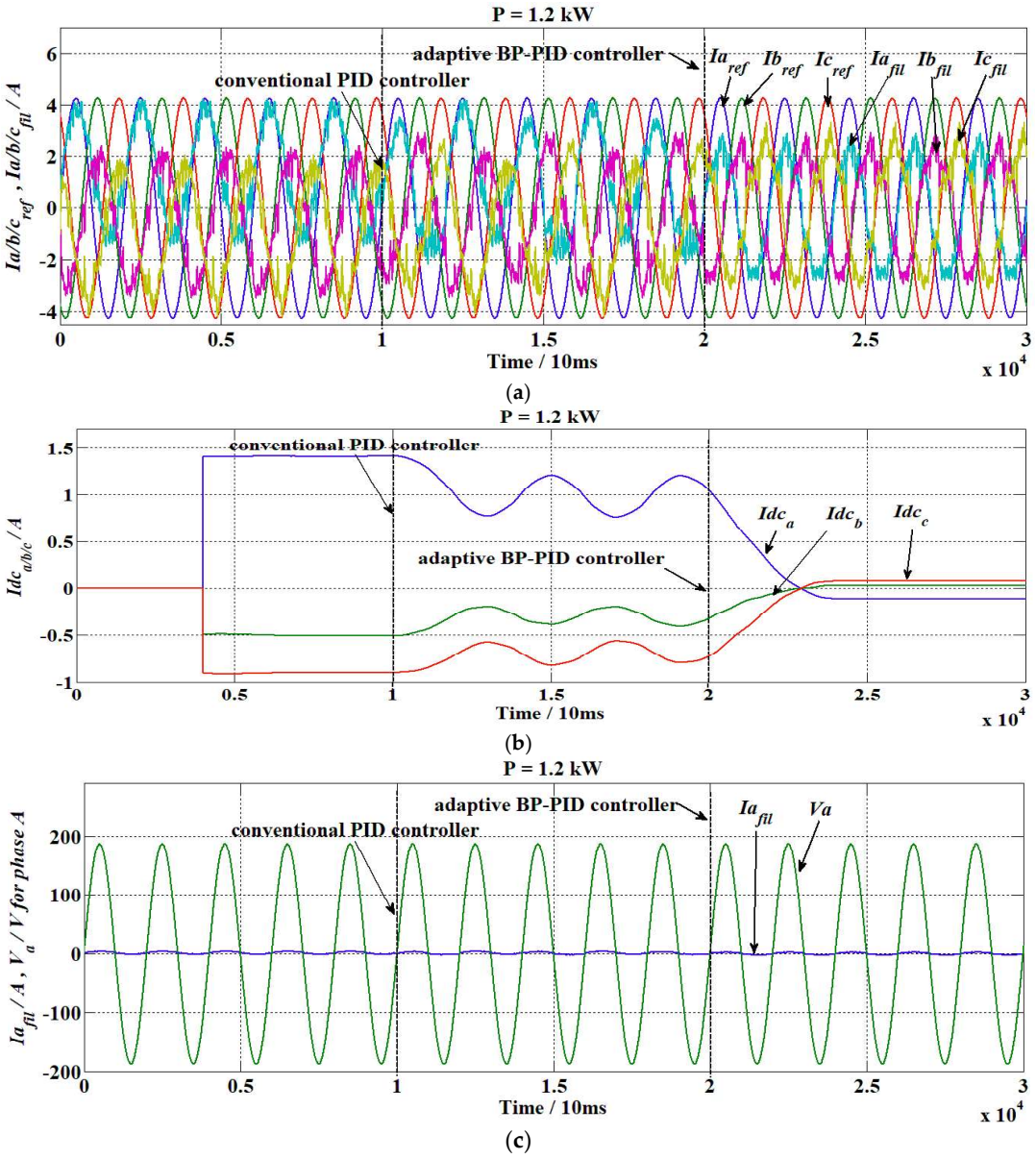


Figure 6. Waveforms of dc component, grid voltage and current using PID controller and adaptive BP-PID controller for dc-component suppression in three-phase system, respectively (P = 1.2 kW, Q = 0), respectively. (**a**) reference and feedback currents. (**b**) dc component extraction using SWDIM. (**c**) current and voltage output of phase-A.

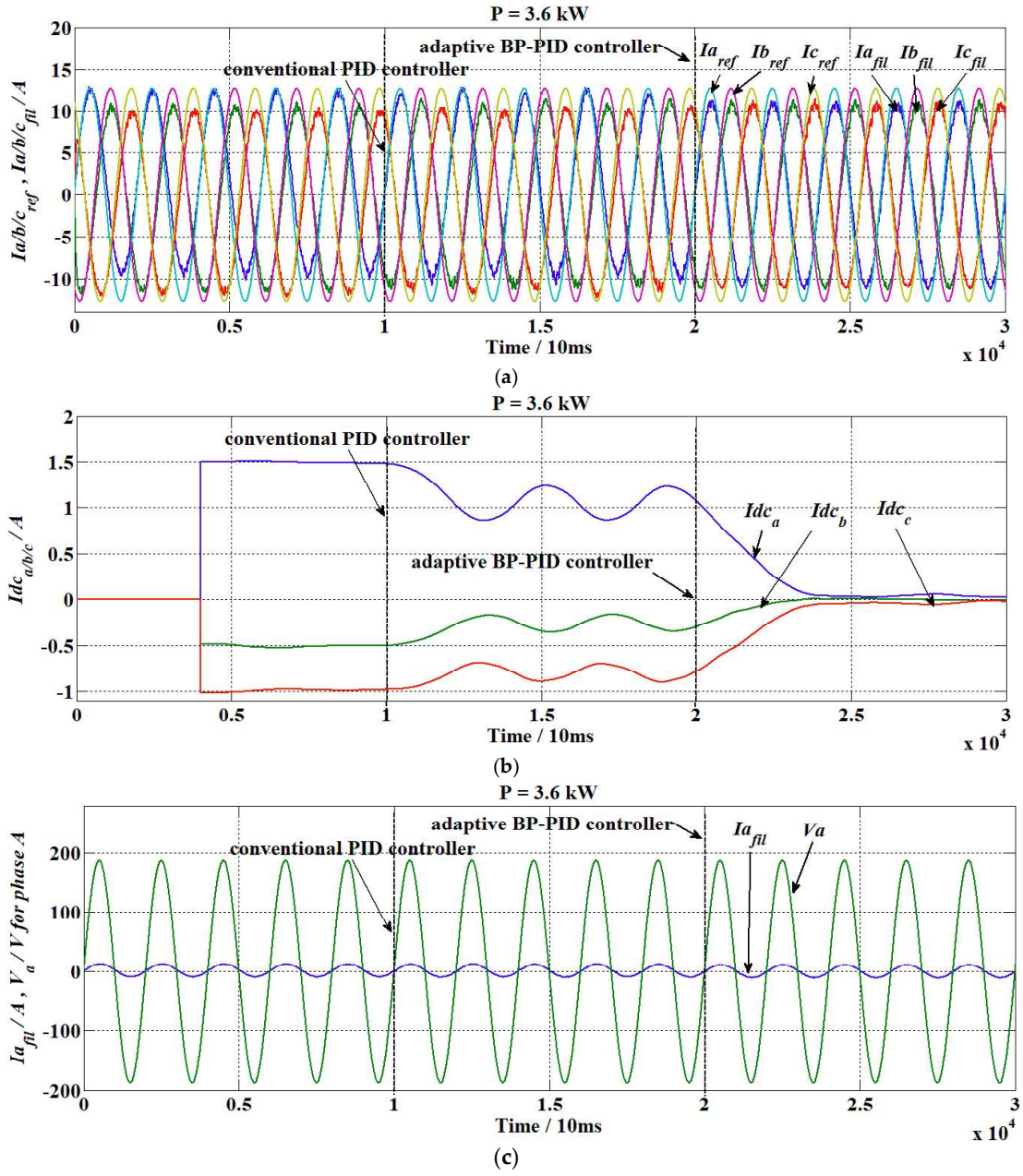


Figure 7. Waveforms of dc component, grid voltage and current using PID controller and adaptive BP-PID controller for dc-component suppression in three-phase system with (P = 3.6 kW, Q = 0), respectively. (**a**) reference and feedback currents. (**b**) dc component of three-phase currents. (**c**) current and voltage output of phase-A.

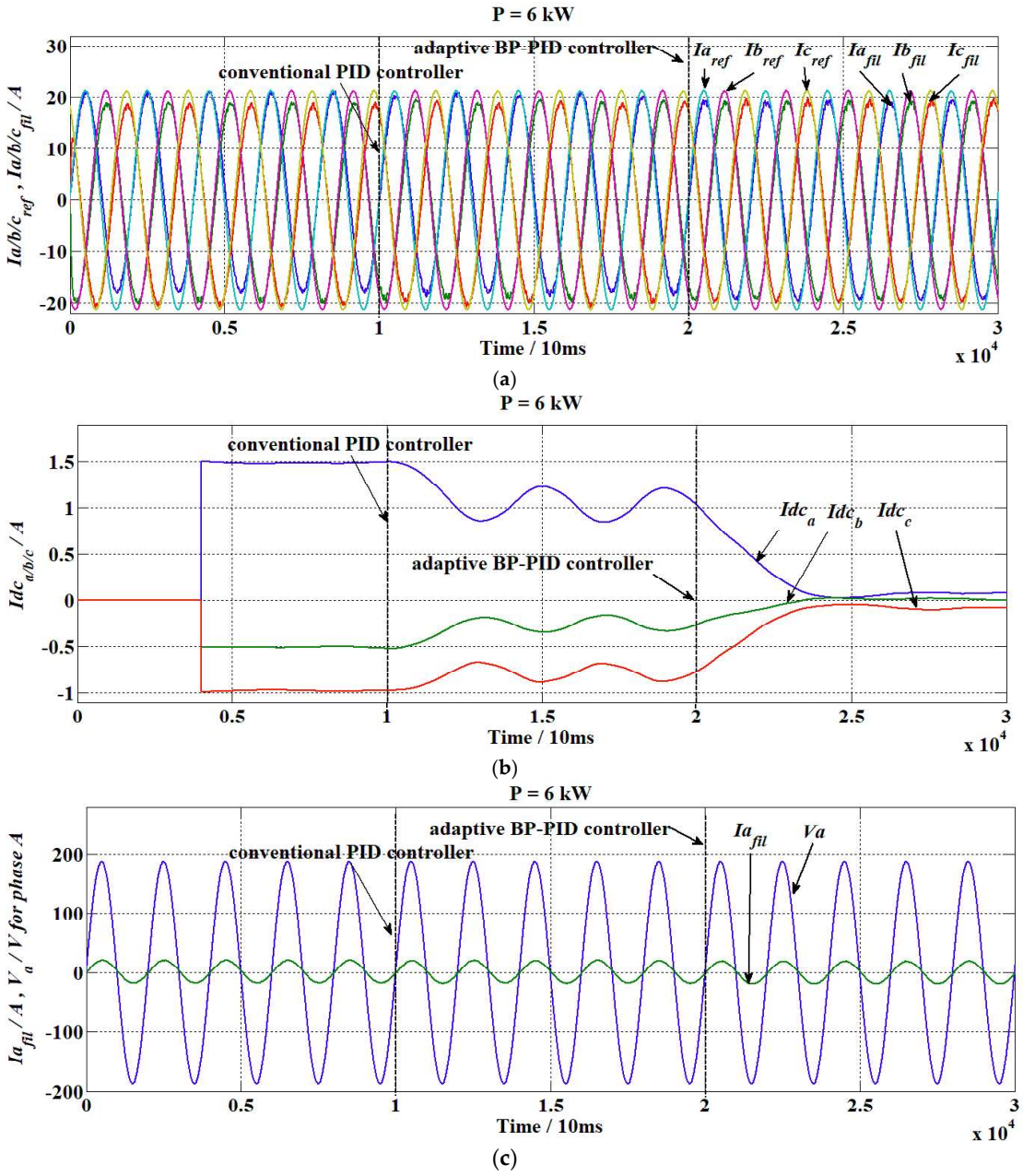


Figure 8. Waveforms of dc component, grid voltage and grid current using PID controller and adaptive BP-PID controller for dc-component suppression in three-phase system with (P = 6.0 kW, Q = 0), respectively. (**a**) reference and feedback currents. (**b**) dc component of three-phase currents. (**c**) current and voltage output of phase-A.

5. Experimental Results

5.1. Hardware Setup

To validate the proposed dc component minimization strategy, a 2-kVA three-phase transformer-less grid-connected inverter system hardware platform is set up. Figure 9a shows the system configuration block diagram and Figure 9b shows the hardware setup of the proposed control scheme. The red line represents the positive pole of the dc bus voltage, and conversely, the black

line represents the negative pole in Figure 9a. Similarly, the yellow,green and blue lines represent A-phase, B-phase and C-phase, respectively. The power transistors IRFP460C 500 V/20 A, which are especially tailored to minimize on-state resistance, provide superior switching performance, withstand high-energy pulse in the avalanche and commutation mode are applied in the system. Since the aim of this article is to verify the correctness of the proposed controller, to guarantee the safety of the hardware configuration, experiments have been made with a relatively small current.

The parameter specifications implemented in the experiment are illustrated in Table 2 in the appendix. The switching frequency of the inverter is 15 kHz. The proposed control scheme is implemented with a 32-bit float-point TMS320F28335 DSP in the experiment, which is mainly used for fast and complicated mathematic calculations and control algorithm implementation. The execution time for the proposed algorithm is about 200 µs in total. A small Hall current sensor is set between the inverter output and the grid to measure the dc component injection to the grid. The voltage across the shunt resistor is filtered by a low-pass filter with a cut-off of 2 Hz to suppress fundamental frequency, a four-channel TDS2010B oscilloscope (Tektronix, Beaverton, OR, USA) is implemented for measuring the dc component voltage.

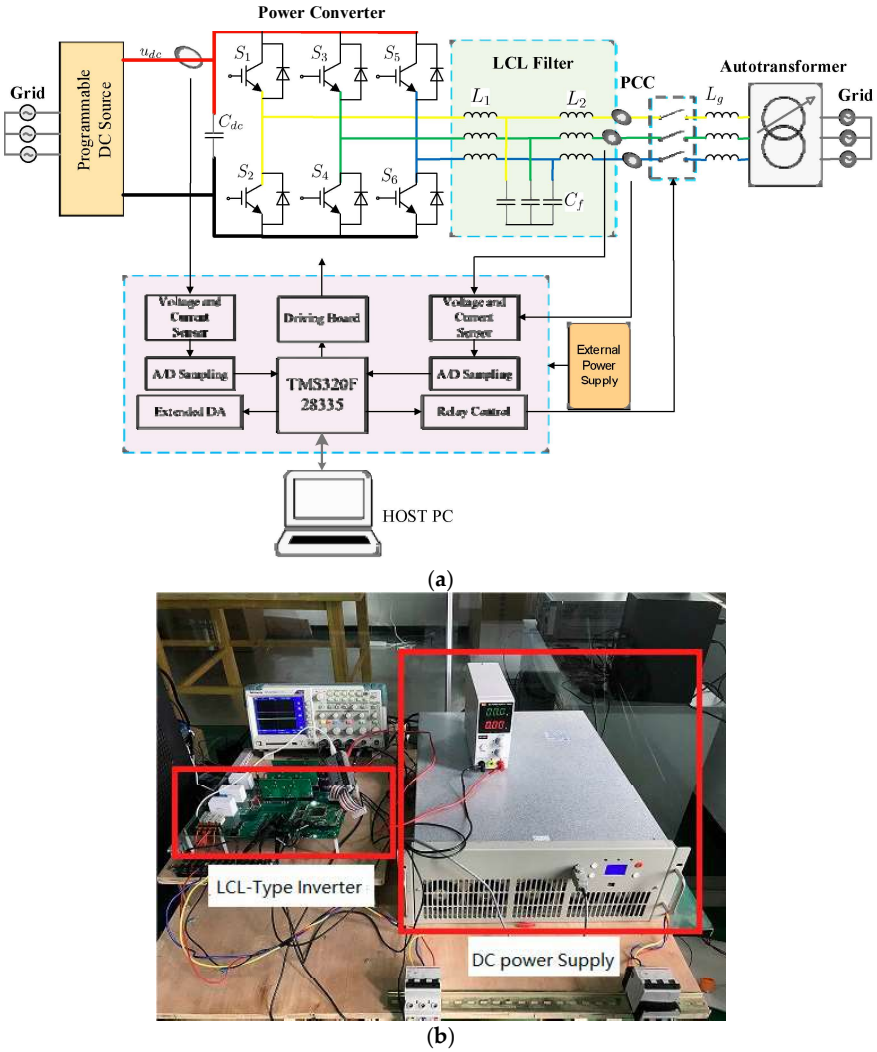


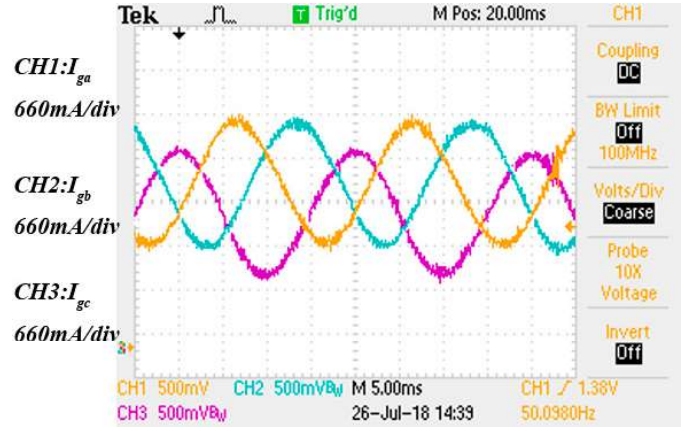
Figure 9. Experiment platform of the three-phase grid-connected inverter. (**a**) system configuration block diagram. (**b**) photograph of the three-phase inverter prototype.

Table 2. Parameter specifications in experiment.

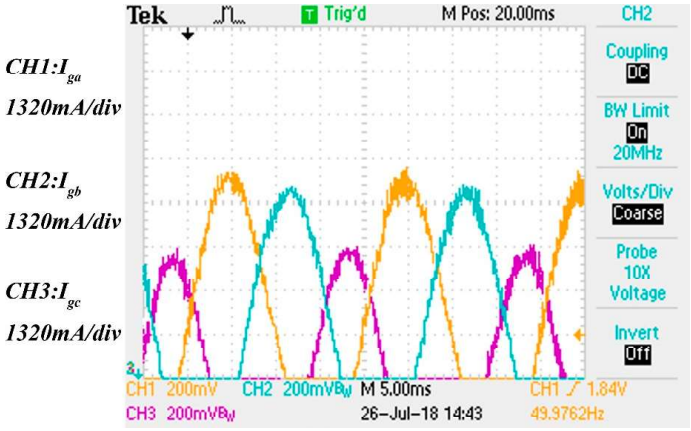
Symbol	Parameter	Values
P_e	Rated power	2 kW
e_g	Line-to-Line voltage (After the autotransformer)	16 V_{ac}
f_g	Grid frequency	50 H_z
C_{dc}	DC-link capacitance	3 mF
L_{inv}	Inverter-side inductance	2 mH
L_g	Grid-side inductance	1 mH
C_f	Filter capacitance	2.2 μF
f_s	Switching frequency	50 kH_z
V_{dc}	DC-link voltage	60 V_{ac}

5.2. Experimental Results

To clearly see the effectiveness of the control strategy on dc component suppression scheme, a dc component bias is superposed artificially on the reference current, via the closed-loop control, leading to a dc component in the grid-side inductance. Then the proposed control scheme is added and checked to verify the effectiveness of dc component minimization. The experimental results are shown in Figures 10 and 11, respectively.



(**a**)



(**b**)

Figure 10. Waveforms of grid current with dc components at different current reference without suppression control. (**a**) $i_{dref} = 1$ A. (**b**) Zoom-in detail of Figure 10a.

Figure 10 demonstrates the waveform of inverter-side current, in which a dc component bias of (0.2, 0.15 and −0.35 A) for i_{aref}, i_{bref} and i_{cref} is superposed on the reference current, respectively, the grid current reference is 1-A. Also, as shown in Figure 10, without minimization control strategy, there are obviously dc components in the three-phase currents. The reference current of the d-axis in rotating coordinates is given by $i_{dref} = 1$ A, the peak values of the three-phase grid current reference are $i_{ga} = 1.19$ A, $i_{gb} = 1.14$ A and $i_{gc} = 0.67$ A, respectively, which demonstrates the existence of a dc component.

Figure 11 shows the grid current with dc component minimization control using the adaptive BP-PID method. When the reference current of the d-axis is given by $i_{dref} = 1$ A, as shown in Figure 11a, the peak values of the three-phase grid currents are $i_{ga} = 0.999$ A, $i_{gb} = 1.029$ A and $i_{gc} = 1.022$ A, respectively. As shown in Figure 11b, with the proposed controller, the grid current becomes more symmetrical, the current differences are 1, 30 and 22 mA, respectively, the dc component can be successfully minimized.

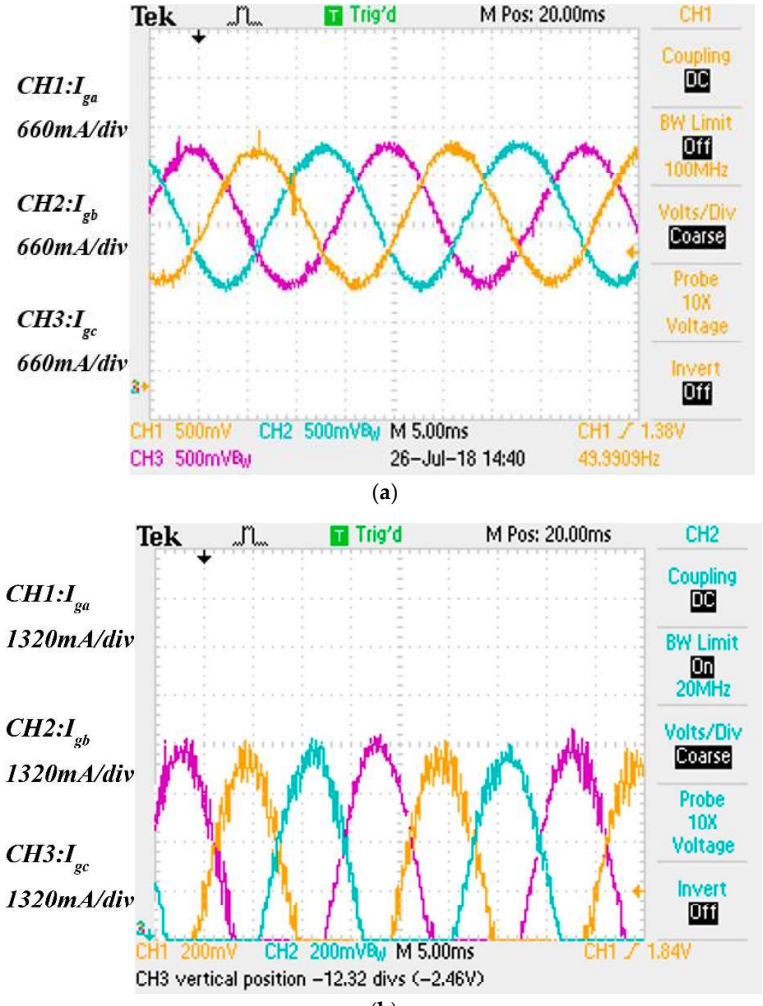


Figure 11. Waveforms of grid current with dc components at different current reference with the proposed scheme. (**a**) $i_{dref} = 1$ A. (**b**) Zoom-in detail of Figure 11a.

Tables 3 and 4 further show the percentage of the dc component and each individual harmonic with and without the dc component minimization as well as the total THD. As shown in Table 4,

with the proposed dc component minimization strategy, both the dc component and the harmonics in the three-phase currents are reduced, compared with the results shown in Table 3. Especially, the dc component has been effectively attenuated below 0.5% as defined by IEEE Standard 1547-2003. In addition, the THD has also been reduced from (7.68%, 6.81%, and 8.13%) to (6.52%, 6.38%, and 5.87%), respectively. These results have shown the effectiveness of the proposed dc component minimization control strategy.

Table 3. Harmonics and THD of the three-phase currents without the dc component suppression.

Three-Phase Currents		Harmonics Order											THD
		DC	1	2	3	4	5	6	7	8	9	10	
$i_{g\mathrm{a}}$	Current value (A)% of fundamental	19.1	100	2.10	1.67	0.57	0.90	0.65	1.28	0.73	0.36	1.75	7.68
$i_{g\mathrm{b}}$	Current value (A)% of fundamental	14.3	100	2.12	1.51	0.63	0.43	0.99	0.58	0.63	0.52	0.46	6.81
$i_{g\mathrm{c}}$	Current value (A)% of fundamental	33.4	100	3	0.25	1.03	1.20	0.4	0.38	0.61	0.78	1.39	8.13

Table 4. Harmonics and THD of the three-phase currents with the dc component suppression.

Three-Phase Currents		Harmonics Order											THD
		DC	1	2	3	4	5	6	7	8	9	10	
$i_{g\mathrm{a}}$	Current value (A)% of fundamental	0.19	100	1.33	0.81	0.39	1.90	0.85	0.72	0.67	0.24	0.15	6.52
$i_{g\mathrm{b}}$	Current value (A)% of fundamental	4.32	100	1.91	1.46	0.84	0.65	0.92	0.92	0.82	1.19	0.44	6.38
$i_{g\mathrm{c}}$	Current value (A)% of fundamental	3.17	100	1.72	1.16	1.38	0.73	0.52	0.25	0.22	0.69	0.34	5.87

6. Conclusions

In this paper, a dc component minimization suppression scheme in a three-phase transformer-less grid-connected system is proposed. The factors that influence dc components are analyzed in detail. SWDIM is implemented for precise dc component extraction even under frequency variation and harmonic distortion conditions. An adaptive BP-PID controller has been designed to enable the precise regulation of the dc components in stationary frame. Theoretical analysis and simulation results have proved the excellent performance of the proposed scheme. Based on a reduced small power hardware platform, experimental results have been given to verify the correctness of the proposed scheme. The proposed method can be well adopted in existing inverters for dc component minimization by adding suitable software programs. We suggest that further efforts can be concentrated on multilevel grid-connected inverters and matrix inverters.

Author Contributions: L.B. conceived and developed the ideas behind the present research and proposed the adaptive BP-PID controller for dc component suppression in the micro-grid system. L.B., L.H., Y.D. and Y.L. executed the hardware setup and software implementation, literature review, and manuscript preparation. Final review, including final manuscript corrections, was performed by K.T.C. and L.B.

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