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A Power and Data Decoupled Transmission Method for Wireless Power Transfer Systems via a Shared Inductive Link

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Abstract: Wireless Power Transfer (WPT) technology is gaining global popularity. However, in some applications, data transmission is also required to monitor the load states. This paper presents an alternative wireless power and data transmission method via the shared inductive link. With the method, the system presents three characteristics: (1) controllability and stability of the output voltage; (2) miniaturization in volume of the system; (3) decoupled transmission of power and data. The output voltage control is realized by a non-inductive hysteresis control method. In particular, data is transferred when the power transmission is blocked (i.e., the hysteresis switch is off). The interference between power and data transmission is very small. The signal to noise ratio (SNR) performance which is relevant to the interference from power transfer to data transfer and data transfer capacity, is studied and optimized. Both simulation and experimental results have verified the proposed method.

Keywords: wireless power transfer; data transmission; hysteresis control; signal to noise ratio (SNR)

1. Introduction

With the demand of transferring power without physical contact, wireless power transfer (WPT) technology is gaining global popularity [1–5] especially for applications in harsh environments [1,2,6–8]. In most cases, a WPT system is designed to provide a load with constant voltage. This can be realized by an open loop design to make the output voltage insensitive to load and coupling coefficient [9] or by a closed loop method to regulate the output voltage [10–12]. The closed loop regulation can be implemented at the primary or secondary side, and the primary side regulation is implemented by changing the input power while the secondary side regulation is implemented by varying the equivalent impedance. Due to the time-varying load characteristics of a practical WPT system, closed loop regulation is more suitable since it can maintain an accurate constant output voltage for variable load resistances.

In WPT applications such as electrical vehicles (EVs) and implant device charging, load status monitoring (e.g., battery status, load voltage, load current, etc.) on the primary side is usually required [13]. Thus data transmission from the secondary side to the primary side is needed. Although there exist some wireless data transmission technologies such as WiFi, Bluetooth and ZigBee, the shortcomings such as complicated paring [13,14] between the transmitter and receiver sides push people keep trying to realize the data transmission by utilizing the inherent wireless power transfer circuit [15,16]. Generally, the major requirement for such a WPT system with data transmission

and output voltage controllability is the decoupling so the transmission of power and data are not affected by each other.

As for wireless transmission of power and data in WPT systems, references [13,15,16] describe data transmission through the existing power coils, while [17] proposes data transmission by the use of extra data transfer coils. In references [13,15,16], the volume of the coupling structure (coils) is relatively small, since power and data are transferred through the same coupling coils. Nevertheless, its data processing circuit is difficult to design to increase the signal to noise ratio (SNR). In reference [17], the data processing circuit is relatively easy to design to increase SNR since the data transfer channel is separated from the power transfer channel, however, the added data inductive channel makes the volume of the coupling structure large. Reference [18] shows an alternative method for parallel transmission of power and data, whereby power is transferred through the fundamental component while data is transferred through the third-order harmonic component. Power and data are transferred through the same coupling structure, but the frequency modulation (FM) would affect the resonance of the power transfer resonant circuits. Reference [14] studied an inductive and capacitive combined parallel transmission of power and data, where data is transferred via the parasitic capacitances, but not all the applications have the required aluminum plates. Reference [13] shows that transferring information of load voltage and current only needs a slow data transfer rate. References [19,20] illustrated that power and data can be transferred through a time division multiplexing (TDM) method, and the transmission of power and data would not be affected by each other.

In this paper, an alternative wireless power and data decoupled transmission method is proposed. Compared with traditional power and data parallel transfer methods, the proposed method can utilize a short power blocking interval to transfer data and keep the power output continuous and stable at the same time. This method is beneficial for SNR improvement and high speed transmission rates. To implement this method, an AC bi-directional switch is added to control the data transmission flow and a hysteresis controller is utilized to realize the output voltage control. These features are verified by both the Bode plot analysis and experimental results.

2. System Overview

2.1. Hysteresis Voltage Control

To simplify the output voltage control circuit, a hysteresis voltage control method is utilized. The corresponding circuit is shown in Figure 1, where S is a decoupling switch, power transmission is blocked (from primary side to secondary side) when S is turned off. A push-pull inverter is used to generate the high frequency AC source. L_p, C_p and L_s, C_s constitute the primary parallel and secondary series resonant circuits, respectively. D_1 ~D_4 constitute the rectifier. R_{eq} is the equivalent input resistance of the rectifier circuit and equals to $8R_L/\pi^2$. C_L is the output filter capacitor and R_L is the load resistance. E and U_L are the input and load DC voltages, respectively.

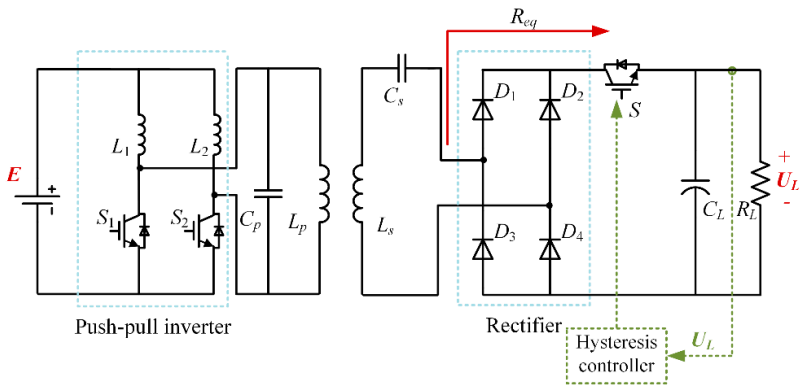


Figure 1. Power transfer circuit with hysteresis voltage control.

The hysteresis voltage control can be illustrated with the aid of Figure 2. Assuming the required constant output voltage is $U_{L\text{-}req}$ with a hysteresis tolerance band of $\pm u_t$. S will be switched to the on state when U_L is smaller than $U_{L\text{-}req} - u_t$ and switched to the off state when U_L is larger than $U_{L\text{-}req} + u_t$.

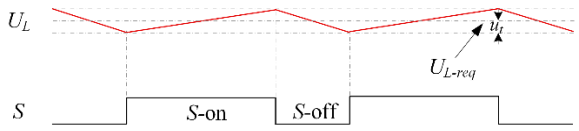


Figure 2. Waveforms to illustrate the hysteresis control.

2.2. Power and Data Transfer Principle

In some WPT applications such as implanted biomedical devices or robot charging, the information such as battery status, output voltage and output current should be transmitted from the secondary side to the primary side. The proposed data transfer circuit is shown in Figure 3, where S_d is an AC switch composed of two semiconductor switches (e.g., IGBTs or MOSFETs). C_{sd} is used to compensate L_s at the data carrier frequency. V_d is the injected data carrier while V_o is the received data carrier. L_d and C_d comprise an LC tuning circuit to maximize the output carrier V_o, satisfying $\omega_d = 1/\sqrt{L_d C_d}$, where ω_d is the angular frequency of the data carrier. R_d is the input resistance of the data processing circuit. The data transfer topology is shown in Figure 4, where the data transmitter side consists of a modulation module, while the data receiver side consists of a bandpass filter, an operational amplifier and a demodulation module. An amplitude shift keying (ASK) modulation method is used to generate the data carrier. The generation function of the data carrier can be given as:

$$d_c(t) = \begin{cases} A_c \cos(2\pi f_d t), & "1" \\ 0, & "0" \end{cases} \quad (1)$$

where f_d and A_c are the frequency and the amplitude of the data carrier, respectively.

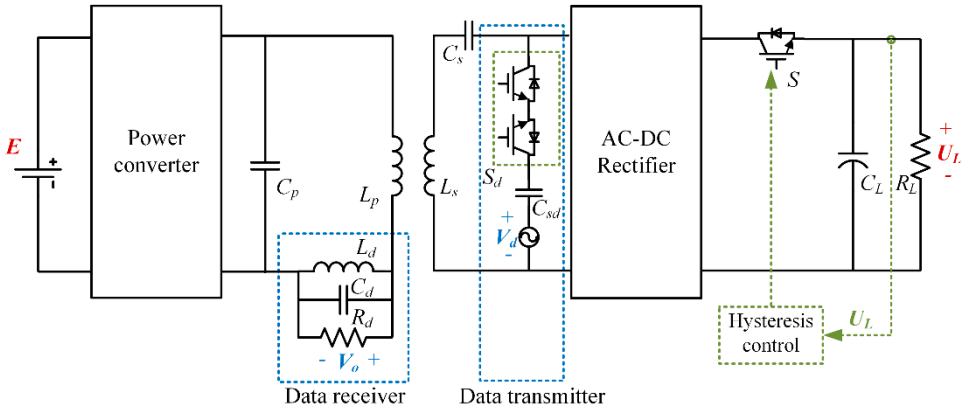


Figure 3. The proposed diagram of power and data transmission.

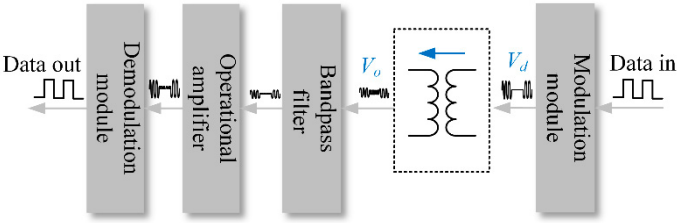


Figure 4. Data transfer topology.

Figure 3 shows that data is transferred during the off state of the decoupling switch S (S_d is turned on when S is off). The proposed system has two working modes: (1) when S is on and S_d is off, power is transferred to the load while data transmission is blocked; (2) when S is off and S_d is on, data is transferred from the secondary side to the primary side while the output capacitor C_L is free running. The circuits of these two working modes are shown in Figure 5.

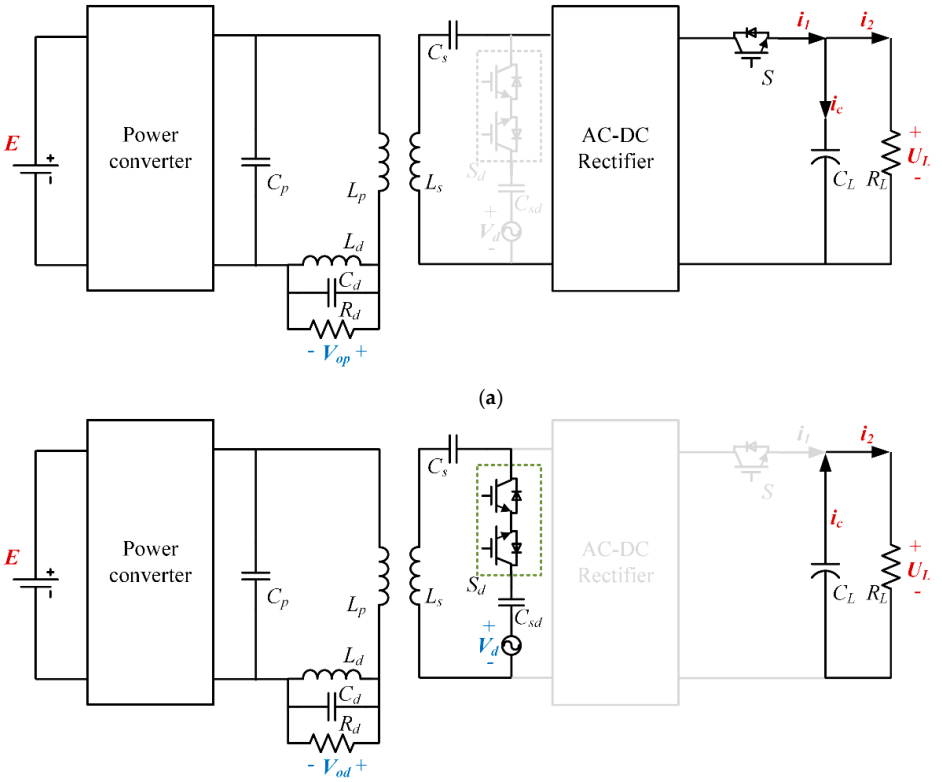


Figure 5. Circuit of the two working modes: (**a**) S is on and S_d is off; (**b**) S_d is on and S is off.

To simplify the analysis, the following assumptions are made: (1) the data carrier frequency f_d is selected higher than the power carrier frequency f_p. This is because the extra data transfer channel would not significantly affect the power transfer and the interference of power transfer on data transfer is easy to suppress; (2) the resonant frequencies of the primary and secondary resonant circuits are identical:

$$\omega_p = 2\pi f_p = \frac{1}{\sqrt{L_p C_p}} = \frac{1}{\sqrt{L_s C_s}}. \quad (2)$$

3. Interference of Extra Data Transfer Channel on Power Transfer

3.1. Interference of Extra Data Transfer Channel on Power Transfer

When considering the influence on power transfer due to the extra data transfer channel, two issues should be of concern. The first is the interference of data carrier transfer with power transfer; the second is the power transfer loss due to the data transfer circuit. However, since data is transferred when the switch S is off, so the interference of data carrier transfer on power transfer can be ignored. As for the power transfer loss due to the data transfer circuit, it can be monitored by the attenuation of output voltage U_L whether the data transfer circuit is added or not. The simplified power transfer circuit without and with the data receiver circuit are shown in Figure 6a,b respectively, where i_i is the equivalent input current source.

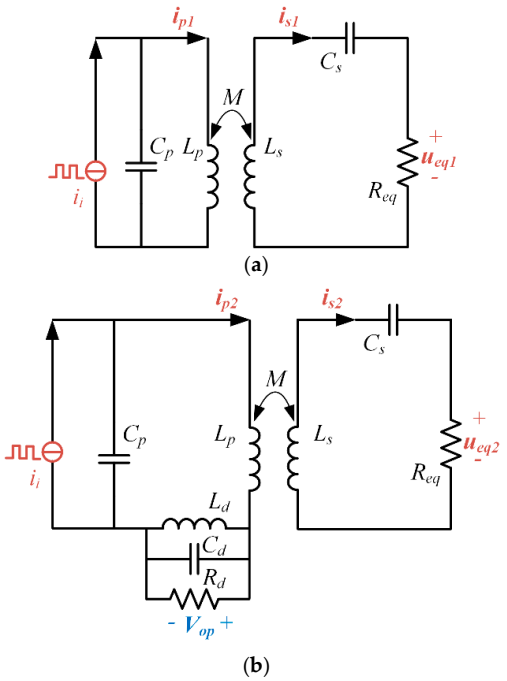


Figure 6. The simplified power transfer circuit: (**a**) without data receiver circuit; (**b**) with data receiver circuit.

For the original system shown in Figure 6a, the reflected resistance to the primary side is given by:

$$Z_r = \frac{\omega^2 M^2}{Z_s} \tag{3}$$

where Z_s is the secondary side loop impedance, given by $Z_s = j\omega L_s + 1/j\omega C_s + R_{eq}$. M is the mutual inductance.

The primary inductance current i_{p1} can be derived as:

$$i_{p1} = i_i \frac{(1/j\omega C_p)}{Z_{p1}} \tag{4}$$

where Z_{p1} is the impedance given by $Z_{p1} = j\omega L_p + 1/j\omega C_p + Z_r$.

The output voltage can be given by:

$$u_{eq1} = j\omega M i_{p1} \frac{R_{eq}}{Z_s} \tag{5}$$

The transfer function from the input current i_i to the output voltage u_{eq1} is:

$$G_{pp1}(\omega) = \frac{u_{eq1}}{i_i} = \frac{MR_{eq}}{C_p(j\omega L_p + 1/j\omega C_p + Z_r)Z_s} \tag{6}$$

As mentioned before, the data carrier is injected to the secondary side only when switch S is off (i.e., power transmission is blocked), the data transmitter circuit does not affect the power transfer. As for the data receiver circuit added in the primary side shown in Figure 6b, the influence can be monitored. The primary inductance current i_{p2} can be rewritten as:

$$i_{p2} = i_i \frac{(1/j\omega C_p)}{Z_{p2}} \tag{7}$$

where Z_{p2} is the impedance given by:

$$Z_{p2} = j\omega L_p + \frac{1}{j\omega C_p} + Z_r + Z_d \tag{8}$$

and Z_d is the impedance of the data receiver circuit, given by:

$$Z_d = \frac{1}{j\omega C_d + 1/j\omega L_d + 1/R_d} \tag{9}$$

$Z_{p2} = j\omega L_p + 1/j\omega C_p + Z_r + Z_d$, $Z_d = 1/(j\omega C_d + 1/j\omega L_d + 1/R_d)$.

So the output voltage can be given by:

$$u_{eq2} = j\omega M i_{p2} \frac{R_{eq}}{Z_s} \tag{10}$$

The transfer function from the current input i_i to the output voltage u_{eq2} can be calculated as:

$$G_{pp2}(\omega) = \frac{u_{eq2}}{i_i} = \frac{MR_{eq}}{C_p\left(j\omega L_p + 1/j\omega C_p + Z_r + Z_d\right)Z_s}. \tag{11}$$

By comparing the Bode plots of Equations (6) and (11), the interference on power transfer due to the addition of the data transfer channel can be monitored, and this will be presented in the following section.

3.2. Interference of Power Transfer on Data Transfer

As for the data transfer channel, the SNR should be designed to be pretty high [12]. There are two factors affecting the SNR performance: (1) the interference of the power transfer with the data transfer; (2) the output capacity of the data transfer. These two effects could significantly influence the SNR performance. For a well-designed data transfer channel, these two factors should be optimized. The interference of power transfer on data transfer should be minimized while the output capacity of data transfer should be maximized.

As for the interference of power transfer on data transfer, the circuit is shown in Figure 6b. According to Equation (7), the interference voltage V_{op} can be expressed as:

$$V_{op} = i_{p2} Z_d \tag{12}$$

The transfer function from the input current i_i to the data output V_{op} is:

$$G_{pd}(\omega) = \frac{V_{op}}{i_i} = \frac{-jZ_d}{\omega C_p\left(j\omega L_p + 1/j\omega C_p + Z_r + Z_d\right)} \tag{13}$$

If the parameters L_p, C_p, L_s and C_s satisfy the assumption shown in Equation (2), then Equation (13) can be simplified as:

$$G_{pd}\left(\omega_p\right) = \frac{V_{op}}{i_i} = \frac{-j}{\omega_p C_p\left({\omega_p}^2 M^2 / R_{eq} Z_d + 1\right)}. \tag{14}$$

Equation (14) shows that the interference transfer function relates to the parameters ω_p, C_p, R_{eq} (R_L), M and Z_d. In order to reduce the interference, we can increase R_L, Z_d or reasonably decrease ω_p, M and C_p.

3.3. Data Transfer Channel Analysis

In the above section, we have learnt that the reduction of power transfer interference on data transfer can be achieved by reasonably setting some parameters. In this section, the output capacity

of data transfer will be studied. When there is only data transfer in the system, the circuit is shown in Figure 7a, where the mutual inductance couplings on primary side coil and secondary side coil are represented by two controlled voltage sources $j\omega Mi_s$ and $-j\omega Mi_p$, respectively.

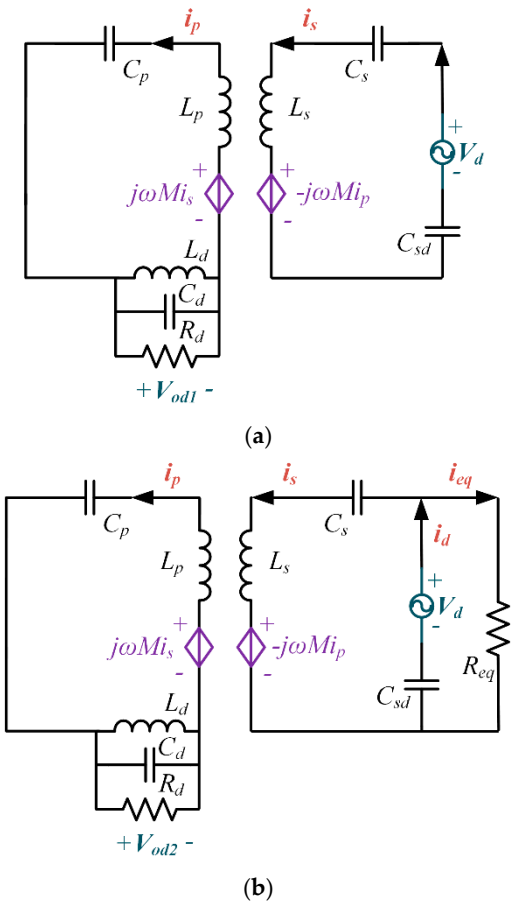


Figure 7. The simplified data transfer circuit: (**a**) proposed data transfer circuit; (**b**) traditional data transfer circuit.

According to Figure 7a, the following equations can be derived:

$$\begin{cases} V_d = i_s(j\omega L_s + 1/j\omega C_s + 1/j\omega C_{sd}) - j\omega Mi_p \\ j\omega Mi_s = i_p(j\omega L_p + 1/j\omega C_p) + V_{od1} \\ V_{od1} = i_p Z_d \end{cases} \tag{15}$$

The transfer function from the input data carrier V_d to the output data carrier V_{od1} can be expressed as:

$$G_{dd1}(\omega) = \frac{V_{od1}}{V_d} = \frac{j\omega MZ_d}{\omega^2 M^2 + Z_d Z_{sd} + (j\omega L_p + 1/j\omega C_p)Z_{sd}} \tag{16}$$

where $Z_{sd} = j\omega L_s + 1/j\omega C_s + 1/j\omega C_{sd}$.

As is mentioned before, L_s, C_{sd} and L_d, C_d resonate at data transfer frequency, so Equation (16) can be simplified as:

$$G_{dd1}(\omega_d) = \frac{j{\omega_d}^3 C_s C_p M R_d}{{\omega_d}^4 M^2 C_s C_p + {\omega_d}^2 L_p C_p - j\omega_d R_d C_p - 1} \tag{17}$$

Figure 7b is presented to compare the SNR of the proposed method (transferring data when power transfer is blocked) with the traditional method which transfers data when power is transferred. The following equations can be derived from Figure 7b:

$$\begin{cases} V_d = i_s(j\omega L_s + 1/j\omega C_s) + i_d/j\omega C_{sd} - j\omega M i_p \\ V_d = i_{eq} R_{eq} + i_d/j\omega C_{sd} \\ i_d = i_s + i_{eq} \\ j\omega M i_s = i_p\left(j\omega L_p + 1/j\omega C_p\right) + V_{od2} \\ V_{od2} = i_p Z_d \end{cases} \tag{18}$$

The transfer function from the input data carrier V_d to the output data carrier V_{od2} can be expressed as:

$$G_{dd2}(\omega) = \frac{V_{od2}}{V_d} = \frac{j\omega^2 M C_{sd} R_{eq} Z_d}{C_{sd} R_{eq}\left(\omega^3 M^2 + Z_d Z_{rs}\omega + Z_{rp} Z_{rs}\omega\right) - j\left(Z_d + Z_{rp}\right)\left(R_{eq} + Z_{rs}\right)} \tag{19}$$

where $Z_{rp} = j\omega L_p + 1/j\omega C_p$, $Z_{rs} = j\omega L_s + 1/j\omega C_s$.

By comparing the Bode plots of Equations (17) and (19), the data transfer capacity of the proposed method and the traditional method can be compared, and this will be presented in the following section.

3.4. Consideration for the Data Transfer Rate

Since the proposed method transferring data when switch S is off, the data transmission rate can be determined by:

$$d_r = d_{cr} \frac{t_{off}}{t_{on} + t_{off}} \tag{20}$$

where d_{cr} represents the conventional data transfer rate, t_{off} is the off-state time while t_{on} is the on-state time in one operation period of the switch S.

So in order to increase the data transfer rate, we can either increase d_{cr} or t_{off}. Increasing d_{cr} can be achieved by increasing the data carrier frequency. As for t_{off}, it can be calculated by:

$$t_{off} = -R_L C_L \ln\left(\frac{U_{l-req} - u_t}{U_{l-req} + u_t}\right). \tag{21}$$

Equation (21) shows that the time interval of the off state can be increased when we reasonably increase the product of R_L and C_L.

4. Simulation Studies

In this section, Bode plot simulation studies are presented to verify the feasibility of the proposed method. The parameters of the system are shown in Table 1, where the frequencies of power and signal are empirically determined as 91 kHz and 10 MHz, respectively, and then L_p, C_p, L_s, C_s can be determined accordingly. The load R_L is 10 Ω, and the required voltage is 16 V, with a hysteresis band of ±0.5 V.

Table 1. System parameters.

Parameter	Value	Parameter	Value
L_p	50 μH	L_s	50 μH
C_p	60 nF	C_s	61 nF
M	12.9 μH	E	20 V
L_1,L_2	150 μH	R_L	10 Ω
f_p	91 kHz	f_d	10 MHz
$U_{L\text{-}req}$	16 V	u_t	0.5 V

4.1. Bode Plot Analysis of Power Transfer with and without Data Transfer

The Bode plots of the power transfer without data transfer (G_{pp1} shown in Equation (6)) from i_i to u_{eq1} and power transfer with data transfer (G_{pp2} shown in Equation (11)) from i_i to u_{eq2} are shown in Figure 8, where we can see that the difference between "with data transfer" and "without data transfer" can be ignored. This verifies that the addition of the data transfer channel has almost no impact on the power transfer.

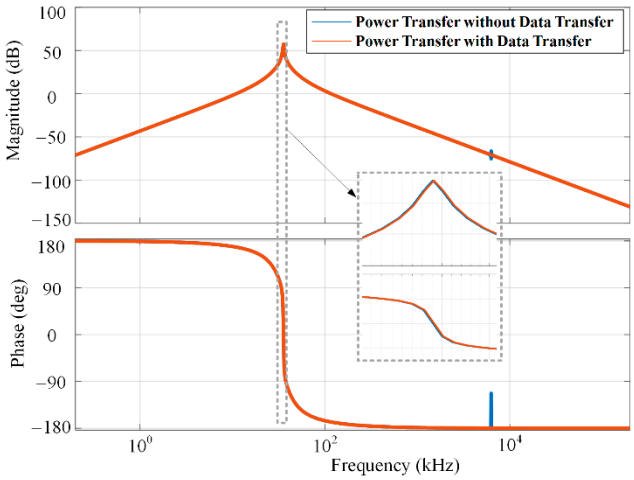


Figure 8. Bode plots of G_{pp1} and G_{pp2}.

4.2. Bode Plot of the Interference from Power Transfer to Data Transfer

The Bode plot of the power transfer interference on the data transfer (G_{pd} shown in Equation (13)) from i_i to V_{op} is shown in Figure 9. From Figure 9, we can see that the magnitude of the interference at the power transfer frequency is around −15 dB, which is pretty low for data transfer, therefore, the SNR can remain pretty high.

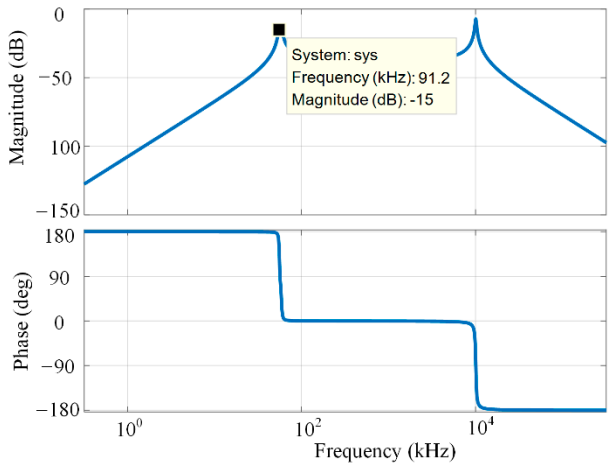


Figure 9. Bode plot of the interference from power transfer to data transfer.

4.3. Bode Plot Analysis of the Proposed and Traditional Data Transfer Channel

The Bode plots of the proposed data transfer channel (G_{dd1} shown in Equation (16)) from V_d to V_{od1} and traditional data transfer channel (G_{dd2} shown in Equation (19)) from V_d to V_{od2} are shown in Figure 10, which shows that the data transfer capacity of the proposed channel is larger than the

traditional channel at the data carrier frequency, so the proposed method for transferring data when power transfer is blocked is more suitable for data transfer.

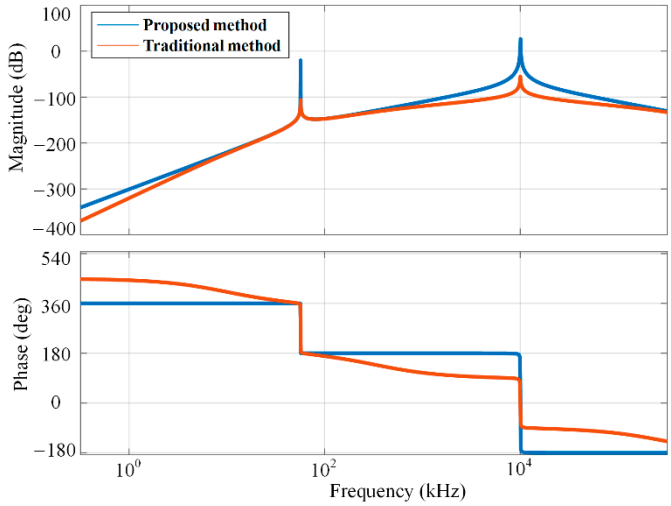
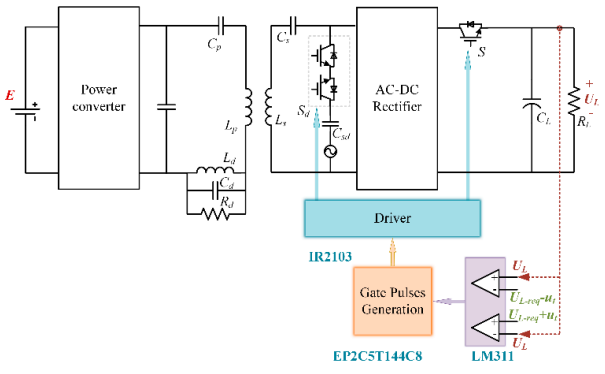


Figure 10. Bode plots comparison between the proposed and traditional data transfer channel.

5. Experimental Verification

To verify the proposed method, an experimental prototype is built according to Figure 3 with the parameters shown in Table 1. For the primary side push-pull inverter, an IRF3610 MOSFET is used as the switch device. For the secondary side rectifier, a SS36 Schottky diode is selected. The detailed power and data transfer circuit is shown in Figure 11. For the secondary side power transfer circuit, LM311 chip is used as the voltage comparator, the comparison signal is fed to the field programmable gate array (FPGA) chip (Altera Cyclone II EP2C5T144C8). Afterward, the FPGA chip determines the on-off state of the switches S and S_d. For the data transfer circuit, the modulation is produced by a CD4051 chip; a ceramic filter chip is used as the bandpass filter while a LT1816 chip is used as the operational amplifier. The demodulation circuit consists of an envelop detector to get the envelop of the carrier and a comparator (LM311 chip) to discriminate the data.



(**a**)

Figure 11. *Cont.*

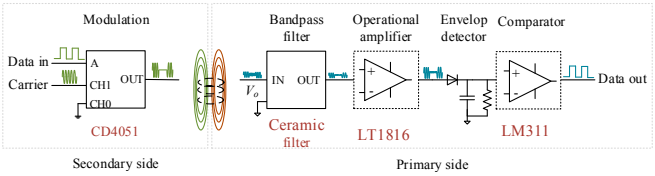


Figure 11. Detailed power and data transfer circuit of the experimental prototype: (**a**) detailed power transfer circuit; (**b**) detailed data transfer circuit.

5.1. Interference Analysis of the Data Transfer Channel to Power Transfer

As is indicated before, the interference from data transfer channel to power transfer can be monitored by the output voltage U_L. Figure 12 shows the experiment results with and without data transfer, where channel 1 indicates the output voltage, channel 4 indicates the voltage of C_p, and channel 2 indicates the output data.

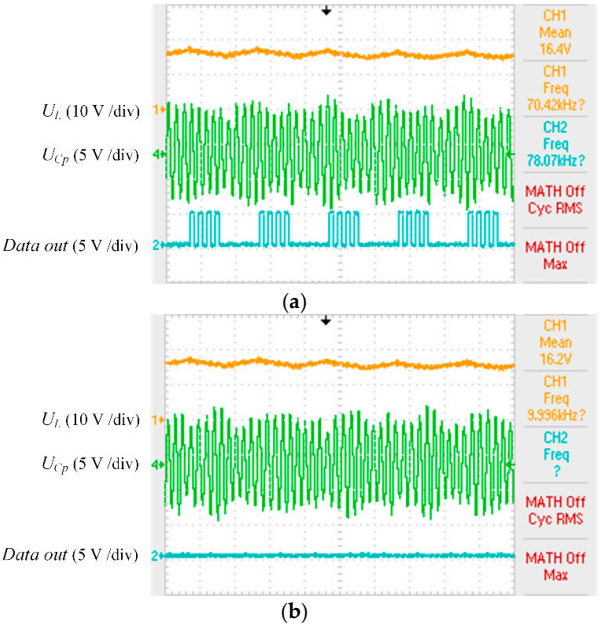


Figure 12. The monitored interference of data transfer to power transfer: (**a**) with data transfer; (**b**) without data transfer.

Figure 12a shows that the mean value of U_L with data transfer is 16.4 V, while Figure 12b shows that the mean value of U_L without data transfer is 16.2 V. Such a small difference indicates the interference of data transfer to power transfer can be ignored. This verifies the Bode plots shown in Figure 8. Furthermore, the system efficiency of Figure 12a is 71%, and the data transfer rate is 560 kbps.

5.2. Comparison between the Proposed and Traditional Data Transfer Method

Figure 13 shows the comparison results between the proposed and traditional data transfer as mentioned in Figure 7. Figure 7a shows the proposed data transfer circuit while Figure 7b shows the traditional data transfer circuit. Channel 1 indicates the output voltage U_L, channel 4 indicates the output voltage of the amplifier, and channel 2 indicates the output data.

Figure 13a shows that data transfer with the proposed method is stable, while Figure 13b shows that data transfer with a traditional circuit failed. The amplitude of channel 4 shows that the amplifier output of the proposed method is larger than that of the traditional circuit, thus the data transfer

capacity of the proposed method is larger than that of the traditional circuit. These results verify the modeling of the transfer function in Section 3 and the Bode plot analysis shown in Figure 10.

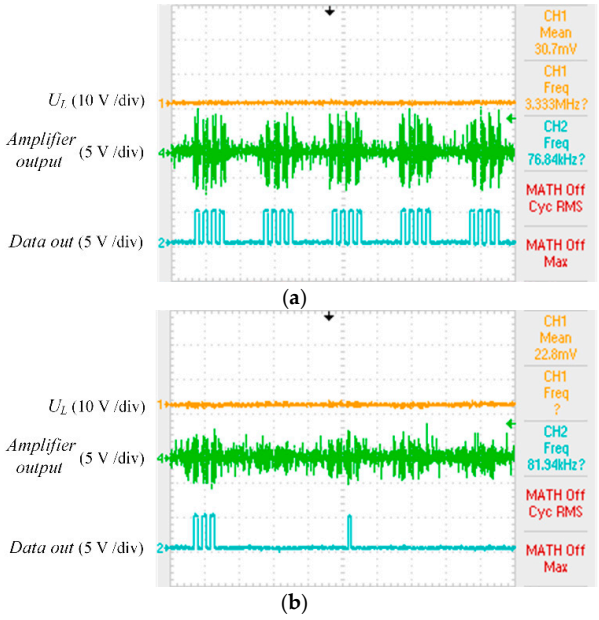


Figure 13. Comparison between the proposed and traditional data transfer: (**a**) proposed method; (**b**) traditional circuit.

5.3. Analysis of the Data Transfer Rate

Equation (20) shows that in order to increase the data transfer rate, we can either increase the conventional data transfer rate or the conduction duty cycle of S_d. Figure 14a shows the case by increasing the conventional data transfer rate, while Figure 14b indicates the case by increasing the conduction duty cycle of S_d.

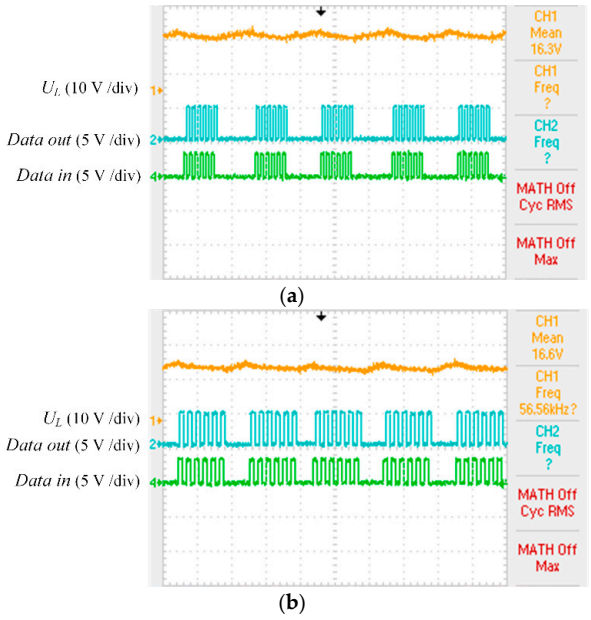


Figure 14. Increasing of the data transfer rate by: (**a**) increasing the conventional data transfer rate; (**b**) increasing conduction duty cycle of S_d.

Both Figure 14a,b show the output voltage is controlled to be around 16 V. In addition, the data transfer rate can be increased through these two methods, i.e. by increasing the conventional data transfer rate or increasing the conduction duty cycle of S_d.

5.4. Comparasion Results with the Published Literatures

Table 2 shows the comparison results between the proposed method and the traditional ways studied in [13–18]. Since the power transfer and data transfer functions of the proposed method are decoupled, the SNR is very high, so as the data transfer rate can reach 560 kbps. It should be noted that a 25 W prototype was set up for demonstration. This method could be used in high power systems due to its high SNR characteristics. Moreover, the data transfer method is especially suitable to monitor the load status in WPT applications such as biomedical implants and robot charging.

Table 2. System parameters.

Reference	Bit Rate (kbps)	Transferred Power(W)	Potential Applications
[13]	2.16	700	EVs (Electrical Vehicles)
[14]	230	40	Peer to peer wireless power transfer (WPT)) with metal shielding such as in EVs
[15]	20	500	High power WPT with low frequency such as in EVs
[16]	19.2	250	Drilling systems
[17]	N/A	N/A	Biomedical implants
[18]	6	N/A	N/A
This paper	560	25	Robots, biomedical implants, etc.

6. Conclusions

This paper proposes a decoupled wireless power and data transmission method via the same inductive link. The method system presents two particular features. The first is that a hysteresis controller controls the power flow. This makes it easy to realize miniaturization for non-inductive design at the secondary side. The second is that data is transferred when the output capacitor is free running to achieve uninterrupted power output. Therefore, the interference between power and data flow is very small. Our Bode plots analysis verifies the effectiveness of the proposed data transfer method. Furthermore, an experimental prototype is built according to the proposed method, where the power and data transfer frequencies are 91 kHz and 10 MHz, respectively. The output power is 25 W with an efficiency of 71%, and the data transfer bit rate reaches 560 kbps.

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References

1. Covic, G.A.; Boys, J.T. Inductive Power Transfer. *Proc. IEEE* **2013**, *101*, 1276–1289. [CrossRef]
2. Hui, S.Y.R. Planar Wireless Charging Technology for Portable Electronic Products and Qi. *Proc. IEEE* **2013**, *101*, 1290–1301. [CrossRef]
3. Mi, C.; Buja, G.; Choi, S.Y.; Rim, C.T. Modern advances in wireless power transfer systems for roadway powered electric vehicles. *IEEE Trans. Ind. Electron.* **2016**, *63*, 6533–6545. [CrossRef]
4. Hui, S.Y.R. Magnetic Resonance for Wireless Power Transfer [A Look Back]. *IEEE Power Electron. Mag.* **2016**, *3*, 14–31. [CrossRef]

5. Dai, X.; Li, X.; Li, Y.; Hu, A.P. Maximum Efficiency Tracking for Wireless Power Transfer Systems with Dynamic Coupling Coefficient Estimation. *IEEE Trans. Power. Electron.* **2018**, *33*, 5005–5015. [CrossRef]
6. Qu, X.; Han, H.; Wong, S.C.; Tse, C.K.; Chen, W. Hybrid IPT Topologies with Constant Current or Constant Voltage Output for Battery Charging Applications. *IEEE Trans. Power. Electron.* **2015**, *30*, 6329–6337. [CrossRef]
7. Chen, L.; Boys, J.T.; Covic, G.A. Power Management for Multiple-Pickup IPT Systems in Materials Handling Applications. *IEEE J. Emerg. Sel. Top. Power Electron.* **2015**, *3*, 163–176. [CrossRef]
8. Gati, E.; Kampitsis, G.; Manias, S. Variable Frequency Controller for Inductive Power Transfer in Dynamic Conditions. *IEEE Trans. Power. Electron.* **2017**, *32*, 1684–1696. [CrossRef]
9. Low, Z.N.; Chinga, R.A.; Tseng, R.; Lin, J. Design and test of a high-power high-efficiency loosely coupled planar wireless power transfer system. *IEEE Trans. Ind. Electron.* **2009**, *56*, 1801–1812.
10. Li, H.; Li, J.; Wang, K.; Chen, W.; Yang, X. A Maximum Efficiency Point Tracking Control Scheme for Wireless Power Transfer Systems Using Magnetic Resonant Coupling. *IEEE Trans. Power Electron.* **2015**, *30*, 3998–4008. [CrossRef]
11. Zhong, W.X.; Hui, S.Y.R. Maximum Energy Efficiency Tracking for Wireless Power Transfer Systems. *IEEE Trans. Power Electron.* **2015**, *30*, 4025–4034. [CrossRef]
12. Zhong, W.X.; Hui, S.Y.R. Maximum Energy Efficiency Operation of Series-Series Resonant Wireless Power Transfer Systems Using On-Off Keying Modulation. *IEEE Trans. Power. Electron.* **2018**, *33*, 3595–3603. [CrossRef]
13. Huang, C.C.; Lin, C.L.; Wu, Y.K. Simultaneous wireless power/data transfer for electric vehicle charging. *IEEE Trans. Ind. Electron.* **2017**, *64*, 682–690. [CrossRef]
14. Li, X.; Tang, C.; Dai, X.; Deng, P.; Su, Y. An Inductive and Capacitive Combined Parallel Transmission of Power and Data for Wireless Power Transfer Systems. *IEEE Trans. Power. Electron.* **2018**, *33*, 4980–4991. [CrossRef]
15. Wu, J.; Zhao, C.; Lin, Z.; Du, J.; Hu, Y.; He, X. Wireless power and data transfer via a common inductive link using frequency division multiplexing. *IEEE Trans. Ind. Electron.* **2015**, *62*, 7810–7820. [CrossRef]
16. Sun, Y.; Yan, P.X.; Wang, Z.H.; Luan, Y.Y. The parallel transmission of power and data with the shared channel for an inductive power transfer system. *IEEE Trans. Power Electron.* **2016**, *31*, 5495–5502. [CrossRef]
17. Wang, G.; Wang, P.; Tang, Y. Analysis of dual band power and data telemetry for biomedical implants. *IEEE Trans. Biomed. Circuits Syst.* **2012**, *6*, 208–215. [CrossRef] [PubMed]
18. Zhou, Y.; Zhu, X.; Wu, L.; Wang, B. Study of Wireless Power and Information Transmission Technology based on the Triangular Current Waveform. *IEEE Trans. Power. Electron.* **2018**, *33*, 1368–1377.
19. Wu, J.; Zong, S.; He, X. Power/signal time division multiplexing technique based on power electronic circuits. In Proceedings of the 26th Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Fort Worth, TX, USA, 6–10 March 2011; pp. 1710–1714.
20. Jiang, C.; Chau, K.T.; Ching, T.W.; Liu, C.; Han, W. Time-Division Multiplexing Wireless Power Transfer for Separately Excited DC Motor Drives. *IEEE Trans. Mag.* **2017**, *53*, 1–5. [CrossRef]