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Extraction of Junction Temperature of SiC MOSFET Module Based on Turn-On dI_{DS}/dt

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Abstract: In this paper, a method of extracting the junction temperature based on the turn-on current switching rate (dI_{DS}/dt) of silicon carbide (SiC) metal-oxide semiconductor field effect transistors (MOSFETs) is proposed. The temperature dependence of dI_{DS}/dt is analyzed theoretically, and experimentally to show that dI_{DS}/dt increases with the rising junction temperature. In addition, other factors affecting dI_{DS}/dt are also discussed by using the fundamental device physics equations and experiments. The result shows that the increase of the DC-link voltage V_{DC}, the external gate resistance $R_{G\text{-}ext}$, and the decrease of the driving voltage V_{GG} can increase the temperature sensitivity of the dI_{DS}/dt. A PCB (printed circuit board) Rogowski coil measuring circuit based on the fact that the SiC MOSFET chip temperature and dI_{DS}/dt is estimated in a linear way is designed to obtain the junction temperature. The experimental results demonstrate that the proposed junction temperature extracting is effective.

Keywords: junction temperature extraction; silicon carbide; switching transients; thermo-sensitive electrical parameter

1. Introduction

In recent years, power semiconductor devices such as the insulated gate bipolar transistor (IGBT) and the metal-oxide semiconductor field effect transistors (MOSFETs) have been widely applied in many industrial fields especially fields with high reliability requirements in new energy, wind power generation, and automotive and aerospace industries [1]. Therefore, the reliability issues have become the focus of increasing concern. In particular, the novel wide band gap (WBG) devices, which are high electron mobility transistors such as silicon carbide (SiC) power MOSFET or gallium nitride (GaN), can significantly improve power density and conversion efficiency. However, due to the lack of related technology and the instability of the gate oxide layer, the WBG devices require significant condition monitoring to ensure its reliability [2–4]. Studies have shown that 31% of failures in power electronic converters can be attributed to the failure of power devices while 60% of device failures are due to thermal stress. In fact, due to the different thermal expansion coefficients of several materials in power semiconductor modules, the accumulation of thermal stress will eventually lead to aging failure. In an actual operating condition, the higher the junction temperature is, the smaller the safety margin of the operation is. Additionally, the greater the junction temperature fluctuations are, the shorter the life of the thermal cycle is. Therefore, the measurement or estimation of junction temperature is essential for its condition monitoring [5,6]. Obtaining this temperature in real time during the operation of the converter can effectively improve the status monitoring system of the SiC MOSFET. In addition, using the junction temperature-based control algorithm can enhance the lifetime of the module [7].

The current methods for obtaining the power semiconductor junction temperature are mainly through a direct measurement method and an indirect measurement method. Direct measurement methods are based on optical and physical contact methods that use infrared cameras (IR) and thermocouples to measure the junction temperature, but they need to destroy the module package structure [8,9]. This method uses an internal implanted thermistor sensor to obtain temperature, but it is limited by the accuracy and bandwidth of the sensor and the dynamic response is slow (a few milliseconds are required). This means the methods based on optical and physical contact are limited in practical industrial applications. Indirect measurement methods mainly include the RC thermal impedance model [10,11] and the thermo-sensitive electrical parameter (TSEP). The RC thermal resistance network model mainly includes the Foster and Cauer models, but they do not consider changes in the thermal impedance caused by aging, which results in the inability to obtain accurate junction temperatures. Based on the TSEP, the temperature estimation of the standard package module can be performed non-invasively without modifying the module itself and only the electrical parameters of the device need to be obtained. Many studies have found that the TSEP method is the most promising solution for monitoring the junction temperature of the module [12]. The high-precision and fast-response temperature measurement of the power device can be performed, and the junction temperature can be measured online or offline using TSEP. This is a very extensive research field. Reference [13] uses the on-resistance R_{on} to obtain the junction temperature of the IGBT. However, due to the low on-resistance of the SiC MOSFET (several tens of mΩ), a very precise measurement circuit is required and the switching frequency of the SiC MOSFET is high. It is difficult to measure the junction temperature accurately. In Reference [14], the IGBT junction temperature was measured using the Miller plateau voltage (V_{GP}). However, due to the high switching speed of the SiC MOSFET, the turn-on transient is only few hundred nanoseconds, which means the length of the Miller platform is very short and is difficult to measure. Reference [15] provides a method for measuring the junction temperature using the threshold voltage (V_{TH}) of the IGBT. Physically, V_{TH} is the minimum gate bias inducing an inversion layer of free electrons underneath the gate oxide. It creates a conductive channel between the drain and source in MOSFET or the collector and emitter in IGBT. Since this voltage is not well defined, a quasi-threshold voltage (gate voltage of drain current reaching 10% of rated current) can only be obtained by detecting the value of the drain current. Reference [16] uses the turn-off delay of IGBT to measure the junction temperature, but SiC MOSFET is a unipolar switching device and does not include any extracting minority carriers during the turned off transient. Therefore, the junction temperature cannot be measured using the temperature sensitivity of the minority carrier during the turn off transient. Reference [17] proposed a method to obtain the junction temperature based on the peak value of the gate current $I_{G\,peak}$ during the SiC MOSFET turn-on transient. Based on the positive temperature coefficient of the internal gate resistance ($R_{G\text{-}in}$), SiC MOSFET can generate different gate currents at different temperatures. The junction temperature is extracted by obtaining the peak value of the gate current.

Reference [18] includes an analysis of the relationship between dI_{DS}/dt and the junction temperature during the SiC MOSFET turned on and off transient. However, it lacks the experimental research on the large current module and does not design a measurement circuit to define the junction temperature. In summary, compared to silicon semiconductors, there are few studies on the junction temperature of silicon carbide semiconductors. Due to the wide bandgap characteristics of SiC MOSFET, some methods of extracting junction temperature can be used on silicon IGBT but cannot be applied to SiC MOSFET. In this paper, based on the switching characteristics of SiC MOSFET, the junction temperature is obtained by the turn-on current switching rate (dI_{DS}/dt). Firstly, it is analyzed that the temperature sensitivity of dI_{DS}/dt is mainly related to the negative temperature coefficient of the threshold voltage (V_{TH}). Second, an experimental platform was established to demonstrate the good linear relationship between dI_{DS}/dt and the junction temperature. The effects of gate drive resistance R_G, the supply voltage V_{DC}, load current I_{DS}, and the drive voltage V_{GG} on dI_{DS}/dt have been experimentally verified. Lastly, a small and economical Rogowski coil measuring

circuit for obtaining the dI_{DS}/dt is proposed. The circuit can be embedded in the SiC MOSFET driver. The feasibility of the circuit to obtain the junction temperature is verified by experiments. In practical engineering applications, considering the switching loss and frequency, an intelligent driver method is proposed to measure the junction temperature of the SiC MOSFET without increasing the switching loss.

2. Theoretical Analysis of Turn-On dI_{DS}/dt Temperature Dependence

Figure 1a shows the cell structure of the planar SiC MOSFET. It can be seen that the cell of the SiC MOSFET is mainly composed of the gate, source, drain, oxide layer, N-drift region, N-base region, and Junction Field-Effect Transistor (JEFT) region. The figure also shows the route of the electron carrier flow, the position of inversion layer channel, and the distribution of parasitic capacitance.

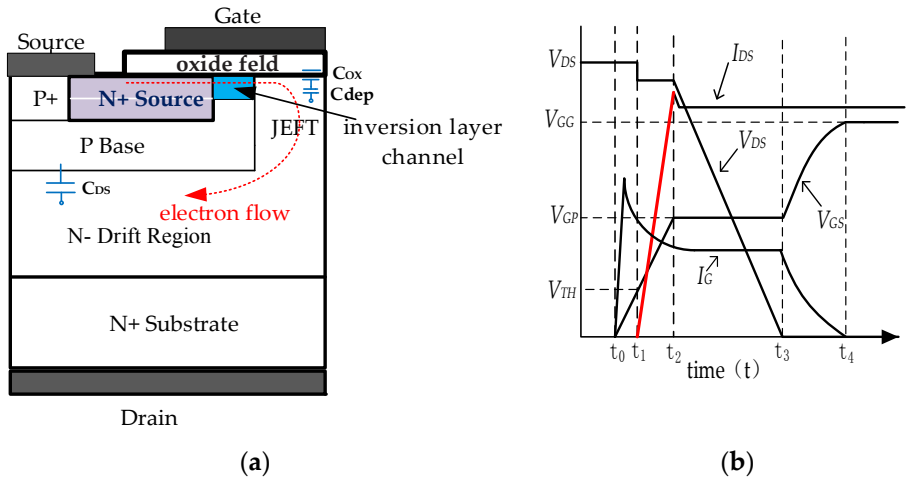

Figure 1. (**a**) Cell Structure of planar silicon carbide (SiC) metal-oxide semiconductor field effect transistor (MOSFET) (N-channel); (**b**) Typical SiC MOSFET turn-on transient waveforms under an inductive load.

Figure 1b shows the typical SiC MOSFET turn-on transient waveforms under an inductive load. In order to facilitate the theoretical analysis, the parasitic inductance of the switching loop is neglected [19]. This switching process can be divided into four phases to analyze further. Before t_0, SiC MOSFET is blocked, the driving voltage $V_{GG} = U_{off}$, the drain-source voltage $V_{DS} = V_{DC}$ (DC-link voltage), and the gate current I_G is zero.

In Phase 1 ($t \in [t_0,t_1]$), the turn-on pulse trigger at t_0, the driving voltage $V_{GG} = U_{on}$, and the gate current I_G first performs a step to its maximum value and then starts to decay. At the same time, the gate voltage V_{GS} begins to increase. Due to the forward bias of V_{GS}, holes in the P base region are first squeezed out to form a depletion layer. With the increase of V_{GS}, the electrons (minority carriers) in the P base region begin to gather under the gate oxide layer to form an inversion layer channel when the energy band is bent to the surface potential, which is equal to the body potential. V_{GS} rises to the threshold voltage V_{TH} when the inversion layer channel is formed at t_1. t_{TH} is the turn-on delay time. When initiating the turn-on until V_{GS} reaches V_{TH}, it can be calculated by using Equation (1) where R_G is the gate total resistance and C_{ISS} is the input capacitance. The expression for V_{TH} can be obtained from reference [18] where q is the charge constant, V_{FB} is the flat-band voltage (related to the oxide layer and semiconductor interface charge and gate material), ξ_{sic} is the dielectric constant of the semiconductor, and N_A is the doping concentration. C_{OX} is the oxide layer capacitance, T is the

absolute temperature (thermodynamic temperature), the Fermi potential ψ_B is the potential difference between the mid-gap and the Fermi level far from the surface, and K is the Boltzmann constant.

$$t_{TH} = t_1 - t_0 = R_G C_{ISS} \ln(\frac{V_{GG}}{V_{GG} - V_{TH}}) \tag{1}$$

$$V_{TH} = V_{FB} + 2\psi_B + \frac{\sqrt{4\xi_{sic} KT \cdot N_A \ln(N_A/n_i)}}{C_{OX}} \tag{2}$$

$$\psi_B = \frac{KT}{q} \ln(\frac{N_A}{n_i}) \tag{3}$$

Using Equation (3), it can be seen that ψ_B is related to the doping concentration and temperature of the semiconductor and n_i is the concentration of the carrier. If the start time of turn-on is 0, the changing rate of the gate voltage can be calculated by using the equation below.

$$\frac{dV_{GS}}{dt} = \frac{V_{GG}}{R_G \cdot C_{ISS}} e^{-\frac{t}{R_G \cdot C_{ISS}}} \tag{4}$$

Phase 2 ($t \in [t_1,t_2)$) is the inversion layer channel established at time t_1. The electron carriers start to enter in the JFET region and the drain-source current I_{DS} starts to increase. When I_{DS} reaches the rated current, the freewheeling diode starts to reverse recovery and the I_{DS} reaches its maximum value at time t_2. Due to the influence of the parasitic inductance between the drain and source, the drain-source voltage V_{DS} drops by a small step, but since V_{DS} >> ($V_{GG}-V_{TH}$), SiC MOSFET is in the saturation region, which means the expression of the drain current I_{DS} can be calculated by using the following equation:

$$I_{DS} = \frac{\beta}{2}(V_{GS}(t) - V_{TH})^2 \tag{5}$$

$$\beta = \frac{W_{CH} \mu_{CH} \cdot C_{OX}}{L} \tag{6}$$

In the above equations, β is the gain coefficient, W_{CH} is the channel width of the inversion layer, μ_{CH} is the effective mobility of the channel electrons, C_{OX} is the capacitance of the oxide layer, and L is the channel length. The current switching rate dI_{DS}/dt can be calculated together with Equation (4) and the derivative of Equation (5), which is shown below.

$$\frac{dI_{DS}}{dt} = \beta(V_{GS} - V_{TH}) \frac{V_{GG}}{R_G \cdot C_{ISS}} e^{-\frac{t}{R_G \cdot C_{ISS}}} \tag{7}$$

In Phase 3 ($t \in [t_2,t_3)$), when the drain-source current I_{DS} reaches the maximum value at time t_2, the gate voltage V_{GS} rises to the Miller plateau voltage V_{GP}, V_{GS} remains basically unchanged, and I_{DS} starts to fall to the rated current. After the reverse recovery of the freewheeling diode is complete, the gate current I_G charges to the Miller capacitance reversely. At the same time, the drain-source voltage V_{DS} begins to drop and drops to a very low on-state voltage at t_3. The Miller plateau stage ends.

In Phase 4 ($t \in [t_3,t_4)$), the gate capacitance C_{GS} is charged by the gate current I_G after t_3. V_{GS} starts to increase exponentially and rises to the driving voltage V_{GG} at t_4. In addition, I_G decreases to zero. At the end of this phase, the SiC MOSFET is fully turned on.

From the SiC MOSFET turn-on process, it can be seen that temperature-related factors include the threshold voltage V_{TH} and the drain current change rate dI_{DS}/dt. When Equations (2) and (3) are combined, the temperature is derived to obtain Equation (8). From Equation (2), the threshold voltage V_{TH} is a function of temperature. As the temperature is raised, the band bending ($2\psi_B$) required to induce an inversion layer decreases due to the rapid increase in the intrinsic carrier concentration (n_i) in Equation (3). This is partially offset by the temperature pre-factor (KT) and the increased ionization of acceptors N_A when the temperature is raised. However, as the temperature rises, the Fermi level moves closer to the mid-gap. Therefore, the band bending ($2\psi_B$) needed to reach the threshold decreases.

This reduces the threshold voltage, which is shown in Equation (2) [20]. Therefore, the threshold voltage decreases with an increasing temperature and shows a negative temperature coefficient.

$$\frac{dV_{TH}}{dT} = \frac{d\psi_B}{dT}\left(2 + \frac{2}{C_{OX}}\sqrt{\frac{\xi_{sic} q N_A}{\psi_B}}\right) \tag{8}$$

The derivation of the temperature is obtained by using Equation (7).

$$\frac{d^2 I_{DS}}{dt \cdot dT} = \frac{V_{GG}}{R_G \cdot C_{ISS}} e^{-\frac{t}{R_G \cdot C_{ISS}}}\left(\frac{d\beta}{dT}(V_{GS} - V_{TH}) - \beta\frac{dV_{TH}}{dT}\right) \tag{9}$$

From Equation (9), it can be concluded that the temperature coefficient of dI_{DS}/dt is related to the gate threshold voltage V_{TH} and the temperature coefficient of the gain coefficient β. Based on Equation (6), the gain coefficient β is proportional to the channel width W_{CH}, the effective mobility of the channel μ_{CH}, and the oxide capacitance C_{OX}, but is inversely proportional to channel length L. W_{CH}, μ_{CH}, and C_{OX} are related to the manufacturer's process and are constant under the same module, which means β only relates to μ_{CH}. In the silicon semiconductor, μ_{CH} is about half of the mobility of the drift region while, in 4H-SiC, μ_{CH} is only 5–10% of the mobility of the drift region. It is mainly affected by the surface roughness scattering, Coulomb scattering, and phonon scattering of the semiconductor and oxide interfaces [21]. The main effect of μ_{CH} is Coulomb scattering at room temperature. As the temperature increases, the surface roughness scattering and Coulomb scattering decrease and a large number of phonon scattering increases, which results in a decrease of the carrier mobility. Therefore, μ_{CH} decreases with an increasing temperature. From Equation (6), β displays a negative temperature coefficient, but due to the wide bandgap characteristics of SiC MOSFET, μ_{CH} is very low and the temperature sensitivity of β is also low. Therefore, the negative temperature coefficient of V_{TH} dominates the negative temperature coefficient of β [21]. The temperature coefficient of dI_{DS}/dt ($(dI_{DS})^2/(dt \cdot dT)$) is mainly affected by the threshold voltage V_{TH}.

Reference [22] proposed that the input capacitor C_{ISS} is also affected by the temperature because C_{ISS} includes Miller capacitance and gate capacitance C_{GS} where the gate capacitance C_{GS} does not change with temperature. The Miller capacitance is composed of the oxide layer capacitance C_{OX} and depletion layer capacitance C_{dep}. In general, C_{OX} does not change with the temperature. The expression of C_{dep} is shown in the equation below.

$$C_{dep} = A\sqrt{\frac{\xi_{sic} q N_A N_D}{2V_{DS}(N_A + N_D)}} \tag{10}$$

In Equation (10), A is the effective area of the capacitor area, ξ_{sic} is the dielectric constant, q is the unit charge, N_D, N_A is the doping concentration of the donor and acceptor, and V_{DS} is the drain voltage of SiC MOSFET. When the temperature rises, the doping concentration increases, and the Miller capacitance increases with a rise in temperature. It shows a positive temperature coefficient. However, since the rise of the drain-source current I_{DS} mainly occurs in Phase 2 (t_1, t_2), the drain voltage V_{DS} is large during this period, which means the depletion capacitance C_{dep} is small. The Miller capacitance is mainly the oxide capacitance C_{OX} [20]. Therefore, the temperature effect of the input capacitor C_{ISS} can be ignored.

In summary, due to the negative temperature coefficient of the threshold voltage (a negative sign before dV_{TH}/dT in Equation (9)), the turn-on dI_{DS}/dt shows a positive temperature coefficient and the SiC MOSFET turns on faster at a higher temperature.

3. Experimental Verification of dI_{DS}/dt Temperature Dependence

3.1. Relationship between dI_{DS}/dt and Junction Temperature

In order to demonstrate dI_{DS}/dt temperature dependence, a 1.2 kV, 180 A SiC MOSFET module (BSM180D12P2C101, ROHM Semiconductor, Kyoto, Japan) [23] was used to build a double pulse experimental platform, which is shown in Figure 2. The module has two SiC MOSFETs switches in series including one as a test device and the other as a freewheeling diode (D_1). The module has a parasitic inductance L_S between source S and auxiliary source S' and it can be seen that L_S is 13 nH from the manual. In the experiment, the DC-link voltage was measured using a high-voltage differential probe (N2891A, Agilent Technologies, Santa Clara, CA, USA) and the drain current was measured using a Rogowski coil (CWTMini1B, PEM, Nottingham, UK). The oscilloscope used for capturing the data was Agilent MSO8064A with a bandwidth of 600 MHz. The SiC MOSFET module is placed on the adjustable heating plate and coated with thermal grease on the substrate. The substrate of the module is closely attached to the heating plate and each temperature is adjusted. The heating process takes a long time in order for the junction temperature (T_j) of the chip can be considered equal to the temperature of the heating plate. Each experiment is performed from a low temperature to a high temperature, which ensures that there is no heat wasted inside the chip. In addition, it improves the measurement accuracy. The experimental circuit is shown in Figure 3.

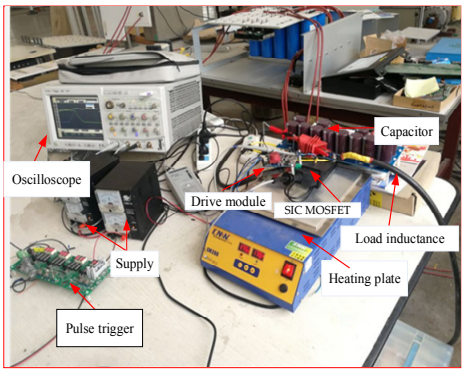

Figure 2. Double pulse experimental platform.

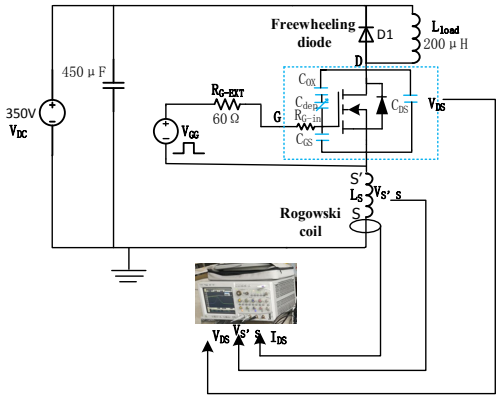

Figure 3. Experimental circuit diagram.

The DC-link voltage V_{DC} = 350 V, the load inductance L_{LOAD} = 200 μH, the external resistor R_G = 60 Ω, and the driving voltage V_{GG} = 18 V. The SiC MOSFET was tested at 60 °C, 75 °C, 100 °C, 125 °C, and 150 °C for double-pulse measurements. The drain current I_{DS} waveforms (measured by the Rogowski coil) of several temperatures are shown in Figure 4. It can be seen that the dI_{DS}/dt *of*

150 °C is greater than 60 °C. Therefore, the dI_{DS}/dt increases when the temperature is raised due to the negative temperature sensitivity of the threshold voltage V_{TH}. In addition, at higher temperatures, the inversion layer forms earlier and the drain-source current I_{DS} takes the shortest time to reach the rated current. At the same time, the intrinsic carrier concentration increases with a rising temperature, more carriers flow through the channel, and dI_{DS}/dt becomes larger. Therefore, dI_{DS}/dt shows a positive temperature coefficient, which is consistent with the above theoretical analysis during the turn on transient. In the experiment, the voltage of the parasitic inductance L_S between the auxiliary source S' and the source S is measured, which is shown in Figure 5. It can be seen that the peak value of $V_{S'S}$ increases with an increasing temperature and shows a better linear relationship. The dI_{DS}/dt can be obtained by Equation (11). The voltage $V_{S'S}$ is 1.6 V at 75 °C and 1.9 V at 150 °C. Therefore, it has a difference of 300 millivolts. The resolution of $V_{S'S}$ is 4 mV/°C and the junction temperature can be obtained in real time by using Equation (12) where K_0 is the temperature resolution. This is related to the manufacturer's production process and product type. $V_{S'S}|_{T_0}$ is the $V_{S'S}$ value at temperature T_0.

$$\frac{dI_{DS}}{dt} = \frac{V_{s's}}{L_S} \tag{11}$$

$$T = K_0\left(V_{S'S} - V_{S'S}|_{T_0}\right) + T_0 \tag{12}$$

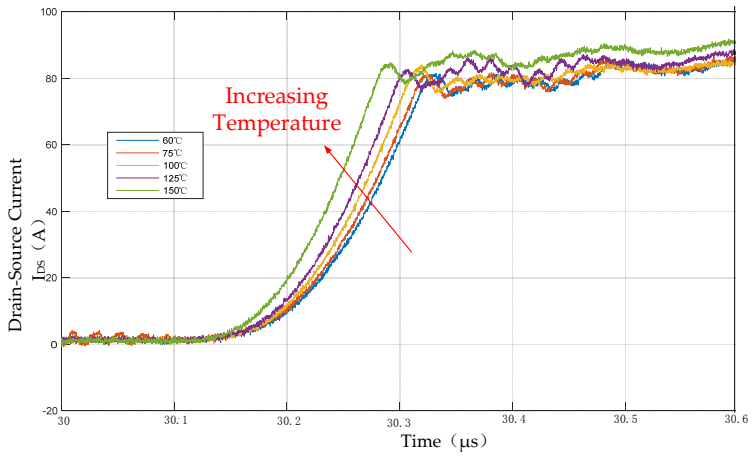

Figure 4. Waveforms of the drain-source current at different temperatures.

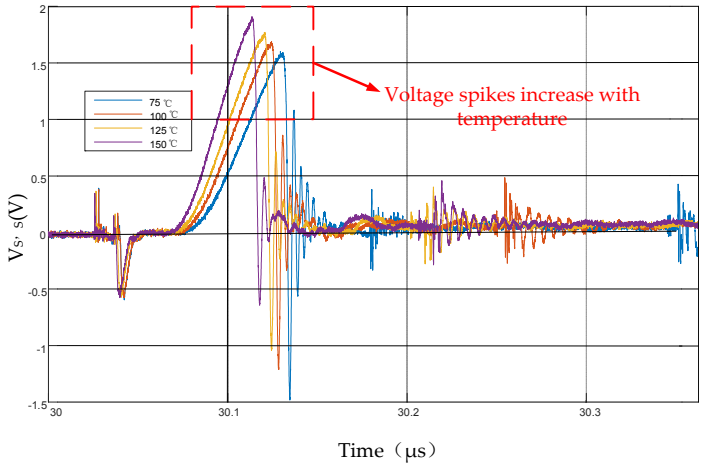

Figure 5. Parasitic inductance L_S induced the voltage waveform at turn-on.

3.2. Influence of Other Factors on dI_{DS}/dt

If dI_{DS}/dt is used as the parameter of TSEP for SiC MOSFET condition monitoring, its relationship with other parameters must be calibrated. The temperature sensitivity of dI_{DS}/dt needs to be removed from these factors in order to be used for the junction temperature detection. From Equations (7) and (9), it is clearly shown that the factors affecting the dI_{DS}/dt are gate resistance R_G, the DC-link voltage V_{DC}, the load current, the gate voltage V_{GG}, and the junction temperature T_j. The relationship between them is shown in Figure 6. The current change rate dI_{DS}/dt increases when the junction temperature T_j, the drive voltage V_{GG}, and the DC-link voltage V_{DC} increase. However, dI_{DS}/dt decreases with increasing gate resistance R_G. The load current cannot be determined by using the formula. The following experiments are used to verify their relationship.

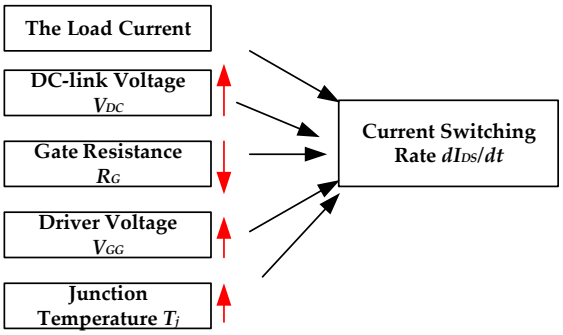

Figure 6. Effect of increasing influence factors on dI_{DS}/dt.

3.2.1. Effect of Load Current and DC-link Voltage on dI_{DS}/dt

The effect of the load current on the temperature sensitivity of dI_{DS}/dt was analyzed in the double-pulse experiment, and the load current can be adjusted by changing the pulse duration of the turn-on voltage V_{GG}. The experiments were performed at the DC-link voltage V_{DC} = 350 V, the driving resistance $R_{G\text{-}ext}$ = 60 Ω, the junction temperature T_j = 150 °C, and a range of load current from 50 A to 160 A. The experimental waveform is shown in Figure 7. It can be seen that dI_{DS}/dt did not change substantially under the different current at the same temperatures. Figure 8 shows that, at the same current, the higher the temperature is, the greater the dI_{DS}/dt is and the better linearity is. Therefore, dI_{DS}/dt is not disturbed by the fluctuation of the load current and it is beneficial to use it as TSEP for the junction temperature extraction of the SiC MOSFET under practical conditions.

In order to verify the effect of the DC-link voltage V_{DC} on the SiC MOSFET, the temperature of SiC MOSFET is kept constant at 150 °C and the drain-source current I_{DS} = 80 A at a steady state. Double-pulse experiments were performed at different DC-link voltages (100 V, 120 V, 180 V, 200 V, 250 V, and 380 V), respectively. The turn-on I_{DS} and V_{DS} waveforms are shown in Figure 9. It can be seen that, at the same temperature and rated current, there is only a slight increase in dI_{DS}/dt of the DC-link voltage with a difference of 280 V. The voltage $V_{S'S}$ induced by parasitic inductance L_S is measured and shown in Figure 10. It can be seen that the peak value of $V_{S'S}$ is also a slight increase with the increase of V_{DC}, which means that dI_{DS}/dt increases slightly with V_{DC}. As the DC-link voltage increases, more charges are discharged in the N- drift region increasing the depletion layer width. This will also decrease the depletion layer capacitance C_{dep}. Based on Equation (10), it can also be seen that C_{dep} decreases with increasing DC-link voltage. Therefore, the Miller capacitance is reduced by increasing V_{DC}, which, in turn, reduces the input capacitance C_{ISS} and speeds up the turn-on transient of the SiC MOSFET. However, C_{dep} is small in this stage (in Phase 2, the drain voltage V_{DS} is large) and dI_{DS}/dt shows a slight increase. However, the DC-link voltage V_{DC} is often constant in voltage source converter applications, which means the influence of V_{DC} on dI_{DS}/dt is less important. The dI_{DS}/dt temperature coefficient is usually calibrated to accommodate different DC-link voltages in a new operating environment. In addition, the slight fluctuation of the DC-link voltage has little effect on

the dI_{DS}/dt in the actual operating conditions, which also facilitates the use of the dI_{DS}/dt as a TESP parameter for junction temperature extraction.

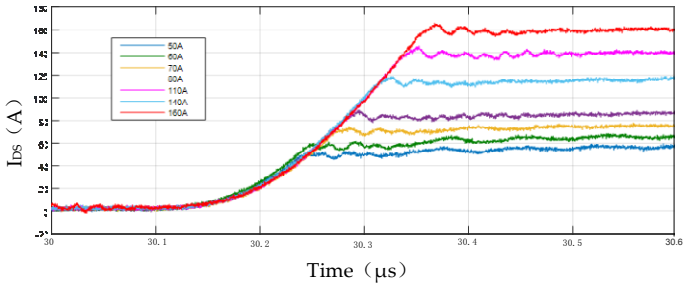

Figure 7. The measured I_{DS} turn-on current transients for different load currents ($R_{G\text{-}ext}$ = 60 Ω, T_j = 150 °C).

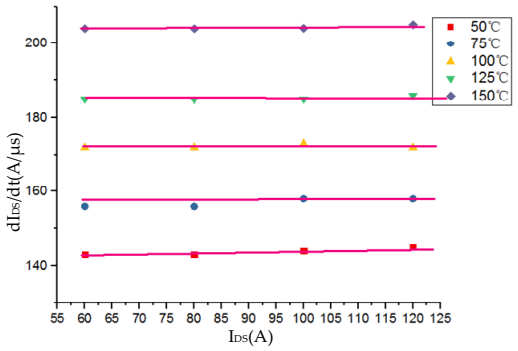

Figure 8. The values of dI_{DS}/dt at different temperatures ($R_{G\text{-}ext}$ = 60 Ω).

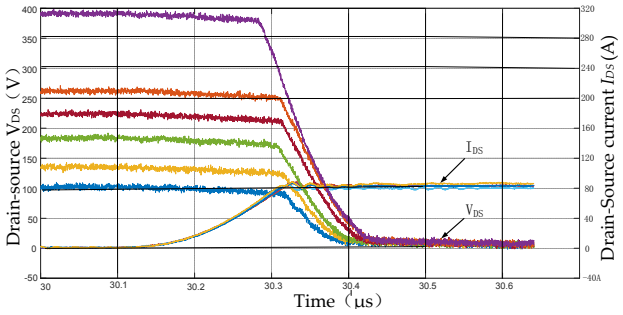

Figure 9. The turn-on I_{DS} and V_{DS} waveforms at different DC-link voltages.

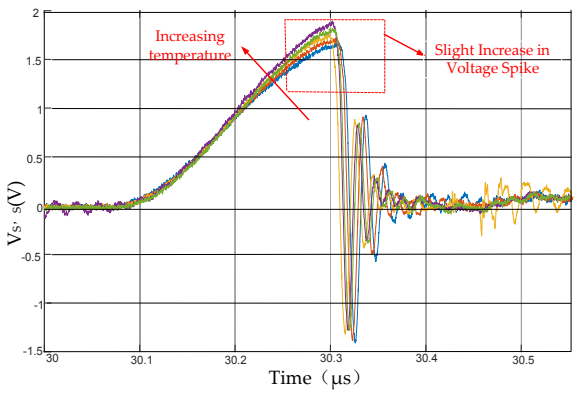

Figure 10. Parasitic inductance induced voltage waveforms at different DC-link voltages.

3.2.2. The Effect of Drive Resistance on dI_{DS}/dt

As known in silicon MOSFETs and IGBTs, the external drive resistance ($R_{G\text{-}ext}$) also affects the turn-on dI_{DS}/dt of SiC MOSFET. In order to observe the effect of the $R_{G\text{-}ext}$ on dI_{DS}/dt, the heating plates were adjusted to 50 °C, 75 °C, 100 °C, 125 °C, and 150°C, respectively. Each adjustment waits for one hour for the junction temperature of the chip to reach the set temperature. The rated current remains at 150 A and the waveforms of I_{DS} observed from different $R_{G\text{-}ext}$ are shown in Figure 11. As observed from Figures 11 and 12, the dI_{DS}/dt reduces as the resistance increases and the switching speed becomes slower. Since the increase of $R_{G\text{-}ext}$ reduces the gate current I_G, the gate voltage V_{GS} charges slowly to the gate capacitance C_{GS} and V_{GS} reaches the threshold voltage for a longer time (introduced from Equation (1)). In addition, the time that V_{GS} reaches the Miller platform voltage also becomes longer (in Phase 2), which means dI_{DS}/dt will decrease when $R_{G\text{-}ext}$ increases (introduced in Equation (7)). However, a small $R_{G\text{-}ext}$ increases dI_{DS}/dt, but the gate parasitic inductance cannot be suppressed in a way that reduces the temperature sensitivity of dI_{DS}/dt by decreasing the gate voltage that reaches the chip [24]. It can be also seen from Figures 11 and 12 that temperature sensitivity of dI_{DS}/dt shows better linearity under a large $R_{G\text{-}ext}$ and there is less oscillation in the waveform of I_{DS} at a large drive resistance, which creates an easy way to obtain dI_{DS}/dt. In addition, $R_{G\text{-}in}$ is the equivalent of the distribution resistance of the gate polysilicon and metal connection in MOSFET. Reference [25] confirmed that $R_{G\text{-}in}$ shows a positive temperature coefficient. If $R_{G\text{-}ext}$ is large, the temperature effect of $R_{G\text{-}in}$ is suppressed and it can be defaulted as R_G ($R_G = R_{G\text{-}ext} + R_{G\text{-}in}$). This does not change with increasing temperature, which means dI_{DS}/dt has better temperature sensitivity under larger $R_{G\text{-}ext}$. Equation (9) also suggests that the increase of R_G decreases the coefficient in front of $d\beta/dT$, which increases the temperature sensitivity of dI_{DS}/dt.

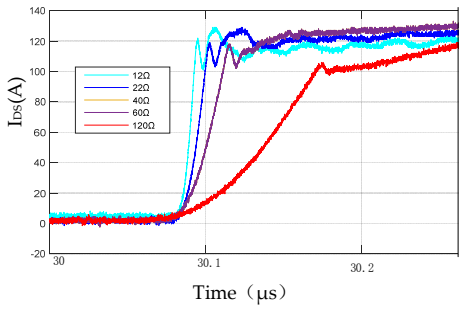

Figure 11. Drain current waveforms with different resistors.

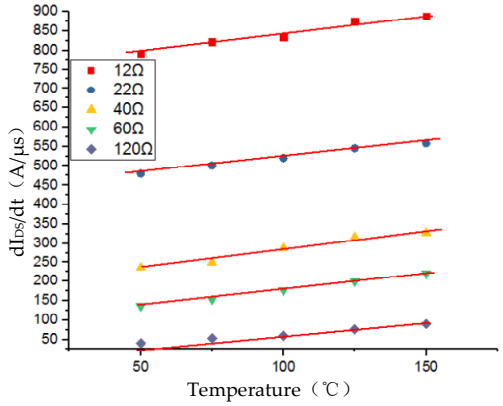

Figure 12. The dI_{DS}/dt under different resistances and temperatures.

In summary, the experimental and theoretical analysis are consistent and dI_{DS}/dt shows better temperature sensitivity under the larger R_G. Based on the experiment of this module, it is found that

$R_{G\text{-}ext}$ shows a better temperature sensitivity when it is around 60 Ω (relative to $R_{G\text{-}in}$, which is already very large). Since $R_{G\text{-}ext}$ is so large, dI_{DS}/dt is too small, which makes the measurement difficult.

3.2.3. Driving Voltage V_{GG} Effect on dI_{DS}/dt

Combined with the theoretical analysis of the second part, it can be seen from Equation (7) that the reduction of the driving voltage V_{GG} will reduce the dI_{DS}/dt. However, from Equation (9), it can be deduced that the decrease of V_{GG} reduces the coefficient of $d\beta/dT$, which increases the positive temperature coefficient of dI_{DS}/dt. In order to verify the influence of V_{GG} on the temperature coefficient of dI_{DS}/dt, the DC-link voltage V_{DC} is kept at 350 V, the driving resistance is $R_{G\text{-}ext}$ = 60 Ω, and I_{DS} at a steady state is 100 A. The double-pulse experiment was performed at different driving voltages of 12 V, 15 V, 18 V, and 20 V and different temperature points of 50 °C, 75 °C, 100 °C, 125 °C, and 150 °C, respectively. Figure 13 shows the waveforms of I_{DS} with different drive voltages of 12 V and 20 V, respectively. Figure 14 shows the dI_{DS}/dt values for different temperatures under the four driving voltages. It can be seen from Figure 13 that, as the driving voltage decreases, dI_{DS}/dt becomes smaller. However, there is a greater range of variation with the junction temperature when the driving voltage V_{GG} = 12 V. Using the dI_{DS}/dt measured at 50 °C when V_{GG} is 12 V as a reference, the value of dI_{DS}/dt at 150 °C increases by 1.2 times. Similarly, using the dI_{DS}/dt measured at 50 °C when V_{GG} = 20 V as a reference, the value of dI_{DS}/dt at 150 °C increases by 1.12 times. At the same time, the reduction of V_{GG} reduces the switching speed and the oscillation of I_{DS} that facilitates the measurement of the dI_{DS}/dt. Therefore, dI_{DS}/dt shows better temperature sensitivity at low drive voltages. However, it can be seen from Figure 14 that the dI_{DS}/dt is too low when the driving voltage is reduced, which makes it difficult to measure. In addition, if V_{GG} is too low, the module will not be completely turned on and it will work in the active area. Therefore, it is best to select a driving voltage of 12 V based on this module.

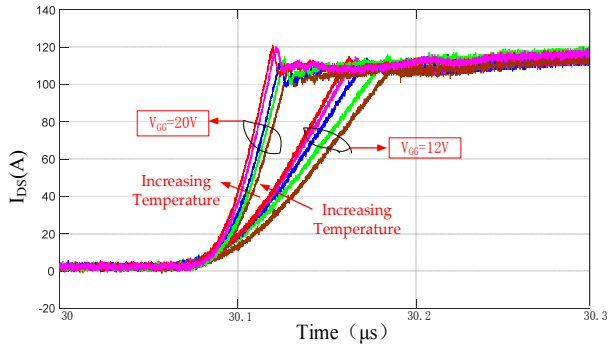

Figure 13. Different temperature drain current waveforms for two drive voltages.

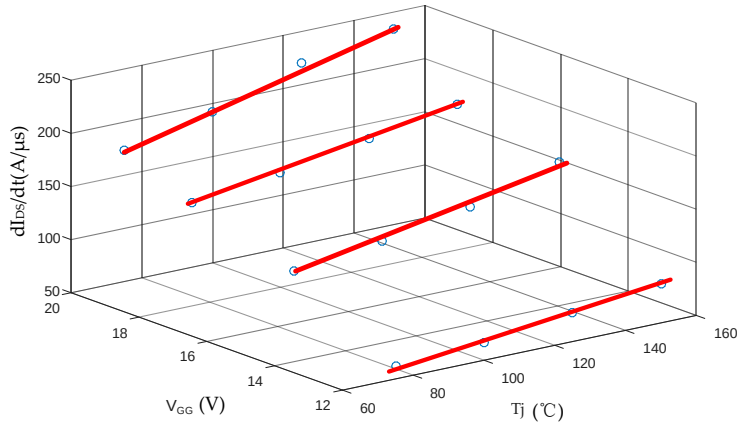

Figure 14. dI_{DS}/dt values for different temperatures under four driving voltages.

4. Design Measuring Junction Temperature Circuit and Experimental Verification

The dI_{DS}/dt as a real-time junction temperature extraction for SiC MOSFETs can be achieved using the following method. For the SiC MOSFET module with a source auxiliary terminal S, it is possible to measure the peak value of the induced voltage $V_{S'S}$ generated by the parasitic inductance L_S between the source assist S' and the source S during the SiC MOSFET turn-on transient. The value of L_S can be found in the device manual. According to the formula $V_{S'S} = L(dI_{DS}/dt)$, the value of dI_{DS}/dt can be obtained. Figure 15 shows the peak value measurement circuit of $V_{S'S}$, but the above circuit is only suitable for SiC MOSFET modules with an auxiliary source. In order to target all modules, a measurement circuit based on the printed circuit board (PCB) Rogowski coil [26] was proposed. The measurement circuit is shown in Figure 16a. It consists of two high-precision operational amplifiers (LM7171), a diode, a storage capacitor of 4.7 nF, and a discharge resistor R_1. The first LM7171 is mainly used to acquire the parameters of the dI_{DS}/dt sensed by the PCB Rogowski coil and is used to isolate the high voltage. The second LM7171 mainly amplifies the resolution according to the actual needs. It facilitates the acquisition of the one-to-one correspondence between dI_{DS}/dt and the junction temperature. From Figure 17b, it can be seen that the circuit occupies a small space and the cost is low so that it can be embedded in the drive module. The PCB Rogowski coil can be directly mounted on the terminal of the SiC MOSFET module, which offers a new idea for engineering applications.

In order to verify the feasibility of the circuit, the driving voltage is 12 V under the voltage and current level of 350 V and 100 A and the double pulse experiments are carried out at the working junction temperature of SiC MOSFET at 50 °C, 75 °C, 100 °C, 125 °C, and 150 °C, respectively. The magnification of the measurement circuit is 1 (This value can be changed by adjusting the ratio of R_2 to R_3) and the output waveform is shown in Figure 17. It can be seen that each temperature corresponding to the measured voltage shows better linearity. The measured voltage is 0.4 V at 50 °C, and 0.8 V at 150 °C. In addition, the resolution is 4 mV/°C. The resolution can be increased by increasing the amplification of the operational amplifier. The Junction temperature of SiC MOSFET can be obtained by using Equation (13) where T_1 is the calculation temperature, K_1 is the resolution (250 °C/mV), and V_1 is the measuring voltage by this measuring circuit.

$$T_1 = K_1(V_1 - 0.4) + 50 \tag{13}$$

To further test the feasibility of extracting the junction temperature of this circuit, the heating plate is adjusted to different temperatures. The measured voltage is obtained by the measuring circuit of Figure 16 and the measured temperature can be calculated by using Equation (13). The result is shown in Table 1. It can be observed that, compared with the actual junction temperature, the maximum deviation of the calculated temperature does not exceed 5 °C. Therefore, this circuit for extracting the junction temperature of SiC MOSFET is feasible. In an actual operation, the junction temperature and the measurement voltage corresponding to the calculated temperature are converted into the digital signals by the A/D module (Analog to Digital Converter) and are stored in the Field–Programmable Gate Array (FPGA) of the driving module. The junction temperature is obtained by looking up the table.

As mentioned above, dI_{DS}/dt has better temperature sensitivity under a small drive voltage and a large drive resistance, but it also brings about an increase in the switching loss. Since the real work does not need to extract the junction temperature at every moment, an intelligent driver [27] can be used to set a small time period to make the driver open SiC MOSFET under the large resistance and small drive voltage for the junction temperature extraction. After the data is acquired, the original small drive resistance and large gate voltage are restored. Therefore, the accurate junction temperature can be extracted while satisfying fast switching frequency and small switching loss. In summary, it is feasible to extract the junction temperature from SiC MOSFET based on dI_{DS}/dt.

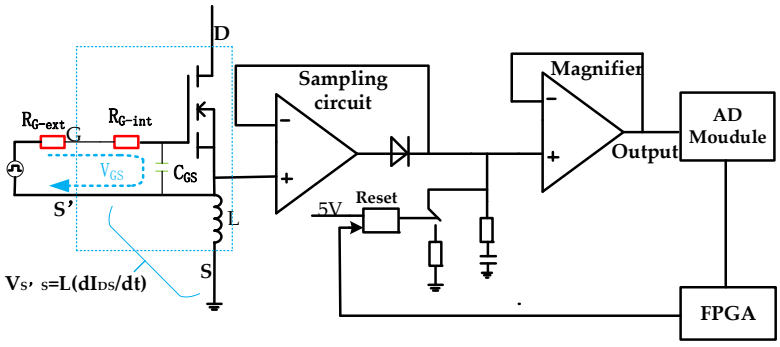

Figure 15. Parasitic inductance induced the voltage $V_{S'S}$ measurement circuit when it is turned on.

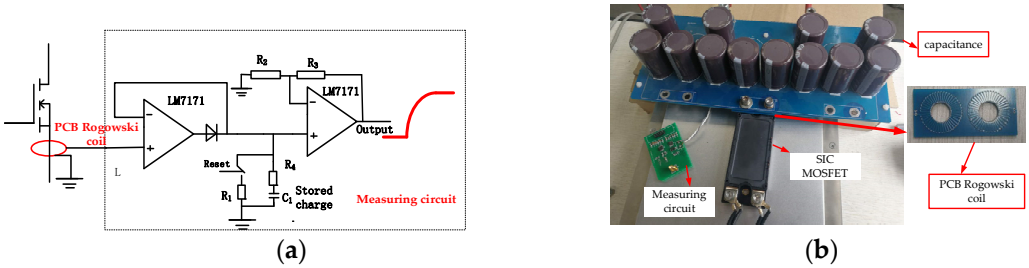

Figure 16. (**a**) dI_{DS}/dt measuring circuit based on printed circuit board (PCB) Rogowski coil; (**b**) measurement circuit appearance.

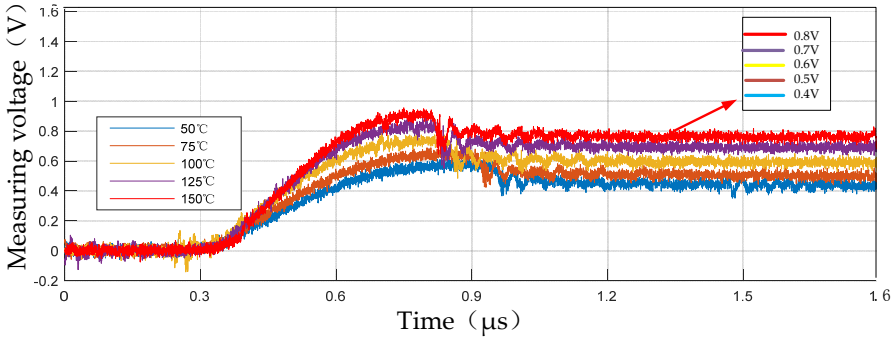

Figure 17. Measurement circuit output waveforms at different temperatures.

Table 1. The measured voltage by the measuring circuit at different temperatures and the temperature calculated by using Equation (13).

Junction Temperature	60 °C	70 °C	110 °C	130 °C	140 °C
Measured Voltage	0.43 V	0.5 V	0.655 V	0.73 V	0.755 V
Calculation Temperature	57.5 °C	75 °C	114 °C	133 °C	139 °C
Deviation	−2.5 °C	5 °C	4 °C	3 °C	−1 °C

5. Conclusions

In this paper, the temperature dependence of the turn-on dI_{DS}/dt of SiC MOSFET is discussed using device mathematical models and experiments. It is shown that dI_{DS}/dt increases with a rising temperature as a result of the negative temperature sensitivity of the threshold voltage V_{TH}. Afterward, other factors affecting dI_{DS}/dt are analyzed. It was found that rising DC-link voltage V_{DC} values

and external gate resistance $R_{G\text{-}ext}$ as well as the decrease of the driving voltage V_{GG} can increase the temperature sensitivity of dI_{DS}/dt. However, the load current has no effect on dI_{DS}/dt. Therefore, there is a good temperature sensitivity of dI_{DS}/dt under large drive resistance and small drive voltage. Lastly, a small and low-cost PCB-based Rogowski coil measurement circuit was designed. The dI_{DS}/dt obtained by this circuit exhibits a near linear dependency on temperature with a resolution of 4 mV/°C (the resolution can be increased by adjusting the amplification factor). When the actual application needs junction temperature extraction, the intelligent driver sends a detection signal to turn on the SiC MOSFET under a small drive voltage and a large drive resistance. The value of dI_{DS}/dt is obtained by measuring the circuit based on the PCB Rogowski coil. Afterward, the operating junction temperature of SiC MOSFET is obtained by the junction temperature database.

Future work will focus on designing intelligent drivers that can be embedded into the junction temperature detection (based on the junction temperature extraction of turn-on dI_{DS}/dt) to use for SiC MOSFET health monitoring (the dI_{DS}/dt temperature sensitivity of aging devices is different). This further tracks the aging of devices and provides an estimation of remaining life.

Author Contributions: G.T. and D.H. conceived and designed the experiments. D.H. and C.G. designed and performed the simulations. J.Z. performed the experiments. D.H. and C.L. wrote the paper.

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Conflicts of Interest: The authors declare no conflict of interest.

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