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A Novel Analytical Formulation of SiC-MOSFET Losses to Size High-Efficiency Three-Phase Inverters

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Abstract: This paper presents a novel analytical loss formulation to predict the efficiency of three-phase inverters using silicon carbide (SiC) metal—oxide—semiconductor field-effect transistors (MOSFETs). The proposed analytical formulation accounts for the influence of the output current harmonic distortion on the conduction losses as well as the impact of the output parasitic capacitances and the deadtime on the switching losses. The losses are formulated in balanced conditions to select suitable SiC MOFETs for the desired target efficiency. To validate the proposed methodology, a 3-phase inverter is designed to present full load efficiency in excess of 99% when built using SiC MOSFETs antiparalleled with SiC Schottky diodes selected for the specified full load efficiency. Experimental assessment of the designed inverter efficiency is compared with the expected values from the proposed analytical formulation and shown to match or exceed the predicted results for loads ranging from 40% to 100% of full load.

Keywords: SiC MOSFETs; EV inverter; high-efficiency inverters; inverter losses

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1. Introduction

Silicon carbide (SiC) power semiconductors low losses and now widespread availability are feeding the continuous demand for higher efficiencies and higher power densities in power electronic converters. The higher operating voltages of power SiC MOSFET devices, regarding power Si MOSFETs, and their lower switching losses compared to power equivalent Si IGBT devices place SiC MOSFETs as the frontrunner semiconductors for electrical vehicles (EVs) and hybrid electrical vehicles (HEV) motor drives among other applications [1].

The advantages of SiC power semiconductors over Si power semiconductors are well documented and highlighted across multiple papers [2–4]. Two clear advantages stand out from the aforementioned works, (1) the reduced chip size area for high efficiency (>99%) converters promising higher power densities and (2) the ability to withstand higher operating temperatures.

Recent studies have also reviewed the past, current, and future applications of SiC power semiconductors showing promising penetration across a variety of areas, emphasizing the numerous advantages of EV motor drives [5,6]. The increase in efficiency brings a reduction in the cooling requirements with clear contributions to the power density whose importance is as meaningful as the cost. Furthermore, the increased efficiency also translates into EVs adopting smaller battery packs, reducing their weight, and increasing the cruising distance [7]. It should still be pointed out that the use of SiC MOSFETs can translate in higher investment costs, both on the development and manufacturing of the inverter, and is as such reserved for applications where the efficiency benefits outweigh these additional costs. A 1% efficiency increase is usually enough to recover the initial extra costs along the converter lifetime.

Inverters with SiC MOSFET technology might aim for unparalleled power densities and efficiencies, as reported in many published works presenting inverter designs showing efficiencies higher than 99% [8–12]. These five works propose distinct approaches for the inverter design, however, they all present a power density lower than 20 kW/dm^3 while [13–17] present converters with power densities higher than 20 kW/dm^3 but they have efficiencies lower than 99%. Figure 1 depicts the above-mentioned works in terms of their efficiency and power density.

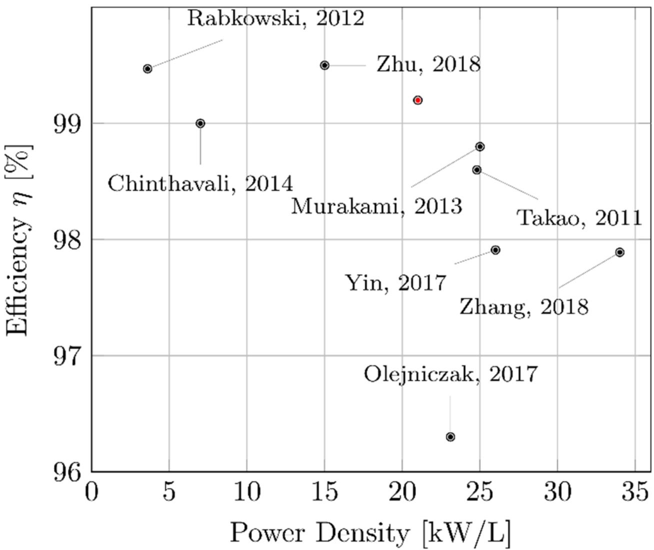


Figure 1. Map of efficiencies vs. power densities for inverters using SiC MOSFETs with the inverter developed to validate this work marked in red [9–17].

Estimating inverter efficiencies in an early stage of the design process is extremely important. Changing the power semiconductors (e.g., if the required efficiencies are not attained) later in the design stages or in an early production stage comes with considerable costs. As such, it is desirable to have a loss formulation that allows for a preliminary selection of the power semiconductors devices to attain a desired efficiency.

The authors of [18] conclude that in three-phase SiC MOSFET inverter motor drives, 99% of the losses come from the power semiconductor modules where the SiC MOSFET itself is responsible for about 96.5% of the total losses, as these inverters do not need magnetic components. As such, a suitable loss formulation for early-stage design should depend mostly on the SiC MOSFET parameters and on the characteristics of the load. It is still important to note that this approximation is application dependent and losses in magnetic components can be significant and eventually considered for an accurate estimation of the converter losses, if magnetic components are embedded in the inverter.

Several efforts to obtain loss models of a single SiC MOSFET have been recently made. The authors of [19,20] review and list several loss computation methods for a wide set of SiC power semiconductor devices. These methods can be roughly divided into physics-based models, behavioral models, and analytical models. Physics-based models depend on a wide set of constructive parameters of the semiconductors that are not easily accessible to power converter designers [21]. Behavioral models depend on transient simulations, which can take extensive computational effort making it inefficient to compare different MOSFETs.

Analytical formulations can be considerably faster to compute but ultimately may have less accuracy than physics-based or behavioral models. As an example, in [22] an analytical model is shown to be 3000 times faster than a physics-based model with similar accuracy to compute the switching losses for a single turn-ON and turn-OFF event. This formulation divides the switching transient in six different stages and provides an analytical loss formulation for each one. However, despite its accuracy, the formulation is not easily adaptable for a three-phase inverter operation with multiple switching events across a

period of low frequency AC output current. A similar conclusion can also be taken for the work in [23], which considers both the SiC MOSFET and the SiC Schottky diode.

Efforts toward an analytical model that can predict the losses on a three-phase inverter can be found in [10] using a piecewise linear model for the switching losses to obtain the energy associated with each commutation during the fundamental output period. The results show a good approximation at higher output powers; however, the error increases substantially for lower output powers.

A loss formulation with a similar goal to the one presented in this paper can be found in [24] but for a three-level neutral-point-clamped inverter where twice as many semiconductors are used. However, the formulation is presented in an integral form and as such, it either depends on a transient simulation to know the profiles of the voltage and current across the semiconductors or assume a constant derivative of the voltages and currents across the semiconductor. Furthermore, it disregards the effect of the deadtime in the switching losses. The influence of this deadtime in a bridge configuration with SiC semiconductors leads to reduced switching losses at higher output currents and increased switching losses at lower output currents [25].

A more complete formulation, but still without the influence of the deadtime, can be found in [26]. This formulation is suitable to be used in early design stages as long as the characteristics of the switching energies variation with the output current for a given DC link voltage are known or extracted by a double pulse test (which can be costly to compare multiple semiconductors). This formulation was tested experimentally with low relative errors for output powers close to nominal.

Most loss formulations assume an even distribution of the losses across the three inverter legs, balanced loads, and AC voltages together with a balanced modulator. When the inverter is in abnormal operating conditions, such as load asymmetries or phase faults, the assumption of evenly distributed losses might not hold. The wide set of potential asymmetric operating conditions that could result in unbalanced operating conditions make it impractical to simulate or even devise pure analytical models to account for all these possibilities. Statistical model verification methods for power electronics converters as described in [27] are a modern approach to provide insight on the expected abnormal operating conditions, and have been successfully applied to multi-level three-phase inverters in [28].

The contribution proposed in this paper is a novel analytical formulation that considers the influence of the output current THD as well as the converter deadtime in the estimation of the conduction and switching losses. The proposed formulation depends only on the characteristics of the load, switching frequency, and parameters that can be typically extracted directly from the device's datasheets. The influence of the reverse recovery time is neglected since it is considered that external SiC Schottky diodes are used which have reverse recovery times and currents much smaller than the more traditional PiN diodes [29].

The new formulation is presented in the next section. Section 3 discusses the semiconductor selection process within the proposed methodology and explores application-specific insights about the proposed formulation. In Section 4, the proposed formulation is experimentally tested against a three-phase SiC inverter and the results are compared and discussed. Conclusions are taken in Section 5, followed by appendixes about formula derivation and experimental measurements uncertainty analysis.

2. Three-Phase Inverter Efficiency Formulation

The inverter efficiency η can be defined considering the input power P_i and the output power P_o. Assuming the output power is known, the efficiency is:

$$\eta = \frac{P_o}{P_i} = \frac{P_o}{P_o + \sum P_{losses}} = \frac{1}{1 + \sum \frac{P_{losses}}{P_o}} \tag{1}$$

where $\sum P_{losses}$ is the sum of all the converter losses. As seen in (1), the efficiency value is dominated by the ratio $\sum P_{losses}/P_o$. This ratio can be expressed as:

$$\sum \frac{P_{losses}}{P_o} = \frac{1-\eta}{\eta} \quad (2)$$

Therefore, if the three-phase SiC is to be designed for an efficiency of around 99.3% then the term $\sum P_{losses}/P_o$ should be around 0.70%.

Assuming most losses are in the SiC MOSFETs, the term $\sum P_{losses}$ may be decomposed into conduction, P_{ON}, and the switching losses, P_{SW} resulting in an efficiency given by:

$$\eta = \frac{1}{1+\frac{P_{ON}}{P_o}+\frac{P_{SW}}{P_o}} \quad (3)$$

Throughout the following subsections the losses ratios P_{ON}/P_o and P_{SW}/P_o will be expanded to account for the traditional conduction and switching losses along with the influence of the parasitic capacitances and harmonic distortion. The inverter is assumed to use external SiC Schottky diodes and as such, losses from the diodes reverse recovery process are negligible [30].

2.1. Computation of the Conduction Losses Ratio P_{on}/P_{sw}

Most inverter pulse width modulators (PWM) switch every semiconductor evenly, therefore equally sharing the losses among the SiC MOSFETs of the three inverter legs. Assume that all the six SiC-MOSFETs have equal channel resistance R_{DSon}, with root mean square (RMS) current $I_{ORMS}/\sqrt{2}$, where I_{ORMS} is the RMS value of the fundamental harmonic output current per inverter phase. The line to neutral voltage is V_{ORMS} and the balanced load has power factor F_p. The on-state losses ratio, considering only the fundamental component of the output current, P_{ONf}/P_o can be estimated as:

$$\frac{P_{ONf}}{P_o} = \frac{6}{3V_{0RMS}I_{0RMS}F_p} R_{DSon}\frac{I_{0RMS}^2}{2} = \frac{R_{DSon}I_{0RMS}}{V_{0RMS}F_p} \quad (4)$$

This equation shows that the ratio P_{ONf}/P_o is proportional to R_{DSon}, and increases linearly with the fundamental harmonic output current I_{ORMS}, while decreasing for increasing V_{ORMS} at constant F_p. Introducing the inverter power modulation index m_p of the inverter powered at constant voltage U_{DC}, $m_p = \sqrt{6}V_{ORMS}/U_{DC}$, Equation (4) can be written as:

$$\frac{P_{ONf}}{P_o} = R_{DSon}\frac{\sqrt{6}I_{0RMS}}{m_p U_{DC} F_p} = R_{DSon}\frac{P_o}{3V_{0RMS}^2 F_p^2} = R_{DSon}\frac{2P_o}{m_p^2 U_{DC}^2 F_p^2} \quad (5)$$

This shows that the on-state losses ratio (for the fundamental current component) at constant U_{DC} and F_p, still raises linearly with the output power P_o, and increases as m_p and F_p decrease at constant I_{ORMS}. The on-state losses ratio is proportional to the output power and inversely proportional to U_{DC}^2 at constant F_p and m_p.

Furthermore, considering an equivalent load impedance magnitude Z_0, that is $I_{0RMS} = V_{0RMS}/Z_0 = m_p U_{DC}/\left(\sqrt{6}Z_0\right)$, then (5) can be further simplified to:

$$\frac{P_{ONf}}{P_o} = R_{DSon}\frac{\sqrt{6}m_p U_{DC}}{m_p U_{DC} F_p \sqrt{6} Z_0} = \frac{R_{DSon}}{F_p Z_0} \quad (6)$$

This shows that the P_{ONf} ratio depends only on the ratio of the transistor on-state resistance R_{DSon} to load impedance magnitude Z_0, at a constant power factor F_p. Therefore, to minimize on-state losses the ratio R_{DSon}/Z_0 should be minimized.

The above formulation for the conduction losses assumes a purely sinusoidal output current, thereby neglecting the effects of the output current ripple. Given that the behavior of the current ripple depends upon the selected modulation scheme and/or controllers, an analytical approach to account for the current ripple in the losses calculations will mostly be application dependent. Contributions with such analytical approaches for modulation methods can be found in [31,32].

However, as an approximation, the power loss formulation can be attained only from the total harmonic distortion (THD) of the output current. The RMS value of the output current considering all the harmonics, I_{0TRMS} can be given by:

$$I_{0TRMS} = I_{0RMS}\sqrt{1+THD^2} \tag{7}$$

The on-state losses can then be computed considering the true RMS output current:

$$P_{ON} = 3R_{DSon}I_{0TRMS}^2 = 3R_{DSon}I_{ORMS}^2(1+THD^2) \tag{8}$$

As such the conduction losses can be divided in two terms, one following the formulation in (5) and (6) complemented with an additional term to account for the output current THD, P_{ONd}:

$$\frac{P_{ONd}}{P_o} = \frac{3R_{DSon}I_{ORMS}^2 THD^2}{3V_{0RMS}I_{0RMS}F_p} = \frac{R_{DSon}I_{0RMS}THD^2}{V_{0RMS}F_p} = \frac{R_{DSon}}{F_pZ_0}THD^2 \tag{9}$$

The conduction losses ratio P_{ON}/P_o can then be written as

$$\frac{P_{ON}}{P_o} = \frac{P_{ONf}}{P_o} + \frac{P_{ONd}}{P_o} = \frac{R_{DSon}I_{0RMS}}{V_{0RMS}F_p}\left(1+THD^2\right) = \frac{R_{DSon}}{F_pZ_0}(1+THD^2) \tag{10}$$

Note that the output power P_o was computed accounting only for the fundamental component output current for two reasons: (1) most inverter loads output power is only related to the fundamental frequency (e.g., electrical machines); (2) it allows a simple but accurate enough relation between the conduction losses and the output power.

2.2. Computation of the Switching Losses

Switching losses are often computed by considering the falling and rising times of the current, t_{fi} and t_{ri}, and the falling and rising times of the voltage, t_{fu} and t_{ru}, along with the typical waveforms of the drain to source current, $i_{DS}(t)$, and the drain to source voltage, $v_{DS}(t)$. The typical switching waveforms can be found in Figure 2 where v_{hdr} and v_{lrd} are the high and low driving voltages of the SiC MOSFET, v_{th} and v_{plt} are the MOSFET threshold and gate plateau voltages, respectively.

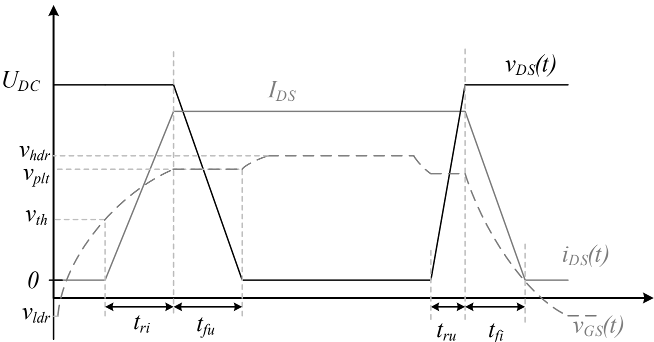


Figure 2. Simplified depiction of the turn-ON and turn-OFF process of a MOSFET device assuming constant derivatives for the channel current and the device drain to source voltage.

Considering the times of the above figures the turn-ON and turn-OFF losses are normally computed considering the triangular area formed by the multiplication of the current and voltage waveforms. Additionally, some authors include an additional term to account for the dissipation of the energy stored in the parasitic output capacitance C_{oss} [22] while others contest that its inclusion results in an overestimation of the switching losses [25].

The switching losses estimation as described in [22,25] is only valid for setups as the double pulse test. When MOSFETs are used to build an inverter leg a more careful inspection is required. Figure 3 details four different commutation scenarios for a single inverter leg: Two transitions from high-side conduction to low-side conduction and two transitions from low-side conduction to high-side conduction both with positive and negative output phase currents.

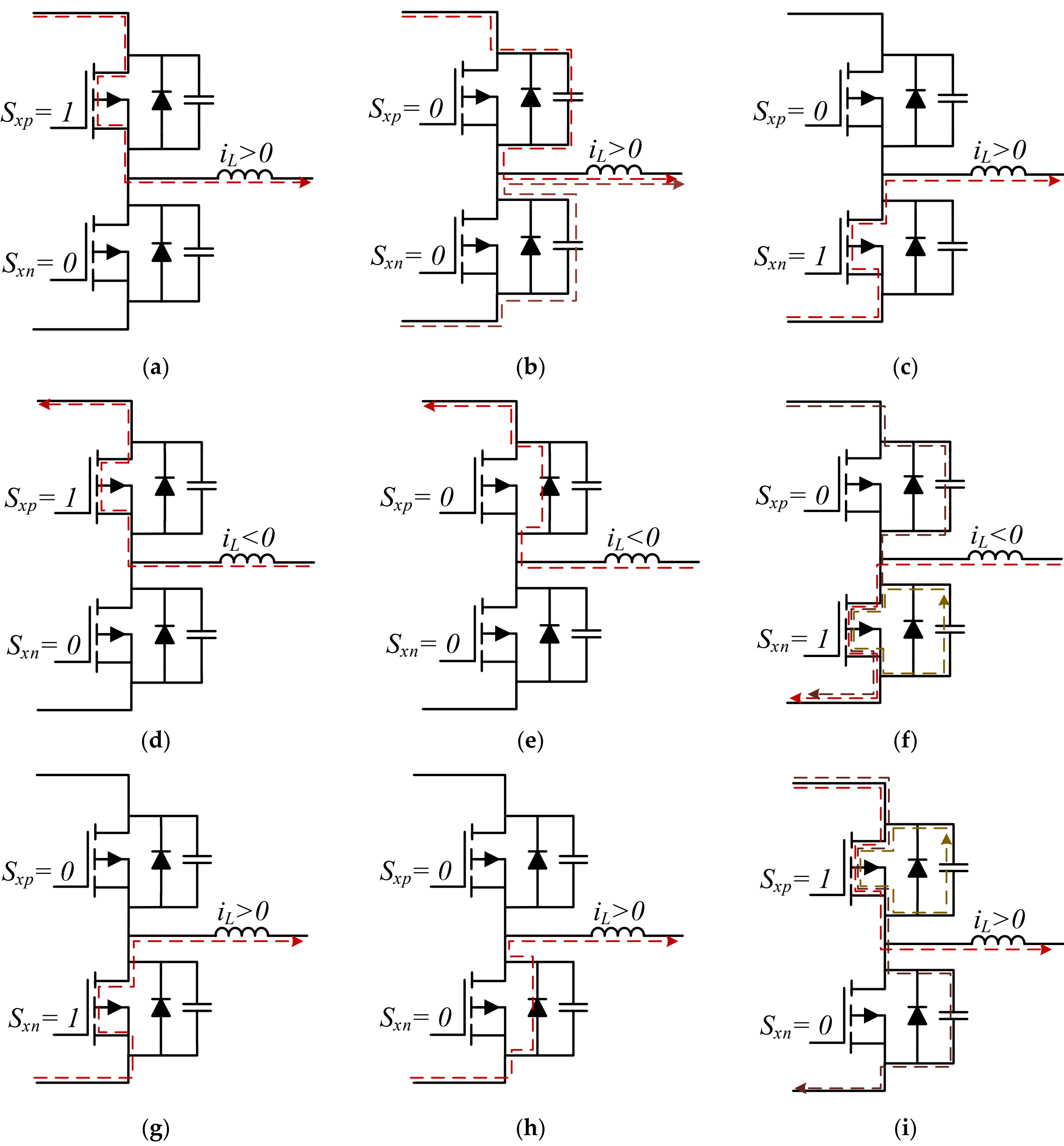


Figure 3. *Cont.*

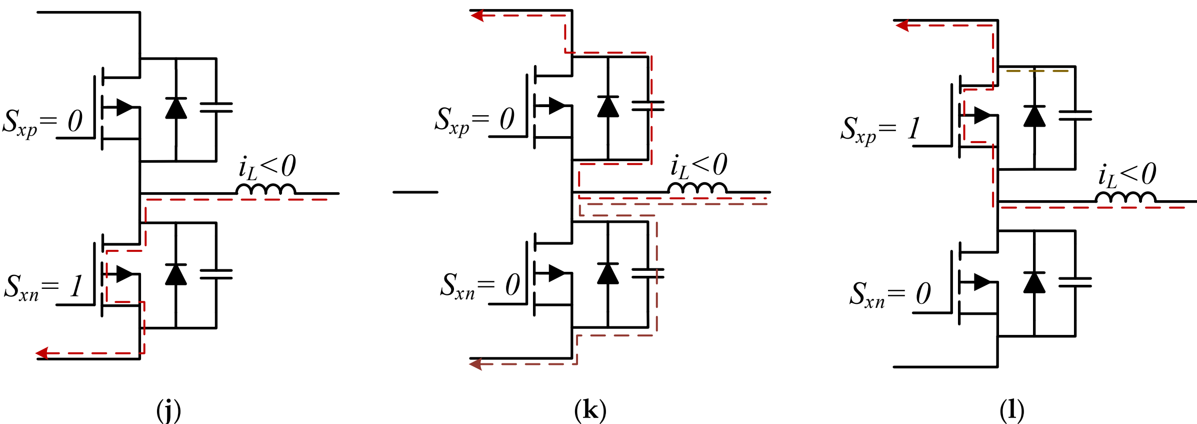


Figure 3. Depiction of the commutation process for an inverter leg with parasitic output capacitances and external SiC Diodes. (**a**–**c**) Commutation from high side to low side with positive output current. (**d**–**f**) Commutation from high side to low side with negative output current. (**g**–**i**) Commutation from low side to high side with positive output current. (**j**–**l**) Commutation from high side to low side with negative output current.

Consider the scenario shown in Figure 3a–c, that illustrates the inverter leg commutation from the high side ($S_{xp} = 1$) to the low side ($S_{xn} = 1$) with a positive phase current $i_L > 0$. The commutation starts with the gate driving signal to open the upper MOSFET ($S_{xp} = 0$) which removes the MOSFET conduction channel charge carriers, previously carrying the inductor current i_L. Considering ideal switching this current would go into the S_{xn} antiparallel diode.

Consider similar upper and lower parasitic capacitances, C_T, (as depicted in Figure 3) given by the sum of the MOSFET parasitic output capacitance, C_{oss}, and the external diode parasitic capacitance, C_d such that $C_T = C_{oss} + C_d$. During the deadtime no MOSFET is driven ON, therefore considering that the output current is positive, both upper and lower parasitic capacitors will charge and discharge trough the load current, respectively (as shown in Figure 3b).

Consider first that the positive load current is high enough to conclude the charging and the discharging process of these capacitors before the lower MOSFET is driven ON. In these circumstances S_{xn} can do a soft commutation with almost zero voltage and the only losses term will be the turn-OFF of the upper MOSFET. An identical conclusion can be obtained for the commutation from the low side to high side with a negative phase current (Figure 3j–l).

Consider now the scenario in Figure 3d–f, where a commutation from high-side conduction to low-side conduction is depicted with a negative phase current. At the instant the upper MOSFET is driven OFF the output current will progressively be carried through the SiC diode keeping the lower parasitic capacitance charged, as a result the turn-OFF process of the upper MOSFET results in a soft commutation with close to zero voltage. During the deadtime the phase current goes through the upper diode and consequently the lower and upper capacitances remain respectively charged and discharged Figure 3e.

The last step of this commutation is the turn-ON process of the lower MOSFET. Once S_{xn} is driven to the ON state then multiple current paths appear (Figure 3f): (1) The output phase current that was circulating through the upper diode is forced through the S_{xn} MOSFET channel. (2) S_{xn} parasitic output capacitance must also be discharged through the MOSFET channel. (3) The current required to charge the parasitic output capacitance of S_{xp} must also conduct through the channel of S_{xn}. The commutation from low side to high side with positive output current shares the same process and is depicted in Figure 3g–i.

To conclude, during a single switching period there will be one turn-ON and one turn-OFF process contributing to losses. If the output current is positive enough then the upper MOSFET turn-ON commutation and the lower MOSFET turn-OFF commutation

will contribute to the switching losses. If the output current is negative enough then this conclusion is reversed. Note that this is only true if, and only if, the output phase current is high enough to charge and discharge the parasitic capacitances during the deadtime.

Hereby follows the loss formulation taking the above-described process into account. The contribution of the turn-ON and turn-OFF losses of both MOSFET (which happen a single time per period, T, per inverter leg) can be written as:

$$\frac{P_{SWI}}{P_o} = \frac{3 I_{DS} U_{DS}}{3 V_{0RMS} I_{0RMS} F_p} \frac{t_{fu} + t_{ri} + t_{ru} + t_{fi}}{2T} \tag{11}$$

It important to note that the I_{DS} current in (11) is not constant along one period of the fundamental output sinusoidal current. However, for a prior efficiency forecast the I_{DS} current can be estimated considering the average of the instantaneous MOSFET current values over one half-period of the fundamental harmonic output current giving $I_{DS} = \sqrt{2} I_{ORMS} / \pi$:

$$\frac{P_{SWI}}{P_o} = \frac{2\sqrt{3} I_{0RMS}}{\pi m_p I_{0RMS} F_P} \frac{t_{fu} + t_{ri} + t_{ru} + t_{fi}}{2T} = \frac{\sqrt{3}}{\pi m_p F_P} \frac{t_{on} + t_{off}}{T} \tag{12}$$

where $t_{on} = t_{fu} + t_{ri}$ and $t_{off} = t_{ru} + t_{fi}$. This losses ratio decreases linearly with m_p and F_p while increasing linearly with the switching frequency, $1/T$, and the switching times t_{fu}, t_{ri}, t_{ru}, and t_{fi}. Remarkably, in the conditions highlighted above, this losses ratio does not depend on the amplitudes of the currents and voltages.

Note that t_{fu}, t_{ri}, t_{ru}, and t_{fi} are normally extracted from the devices datasheets for a given set of operating conditions. t_{ri} and t_{fi} can be extracted from the input parasitic capacitance of the MOSFET, C_{iss}, the gate resistance R_g and the gate driving voltages. For simplicity, consider that the values of t_{ru}, t_{fu}, t_{ri}, and t_{ru} are known. These values can be computed directly from parameters available in the device's datasheets, either presented directly or from the parasitic capacitances and driving voltages. An estimation of these times accounting for the influence of non-flat Miller plateau region can be found in [33].

The relation in (12) accounts only for one of the three current paths described in the turn-ON process and is missing the contributions of the currents that results from the charging and discharging of the parasitic capacitances. Assuming a single hard commutation per inverter leg, the hard commutation will have to handle the discharge current of one parasitic capacitance and the charge current of the opposite. The losses contribution from the charge and discharge of the parasitic capacitances C_T can be shown to be:

$$\frac{P_{SWC}}{P_o} = \frac{3\left(2 \frac{1}{2T} C_T U_{DC}^2\right)}{3 V_{orms} I_{orms} F_p} = \frac{C_T U_{DC}^2}{V_{orms} I_{orms} F_p T} \tag{13}$$

Using the relations for m_p and I_{orms} used in (5) and in (6), respectively, (13) can be simplified to:

$$\frac{P_{SWC}}{P_o} = \frac{\sqrt{6} C_T U_{DC}^2}{m_p U_{DC} I_{orms} F_p T} = \frac{6 C_T Z_0}{m_p^2 F_p T} \tag{14}$$

This result shows that the parasitic capacitance C_T contributes linearly to the P_{SWC}/P_o ratio. This ratio also reduces quadratically with m_p and F_p while it increases linearly with the load impedance, Z_0, and the switching frequency, $1/T$.

The complete switching losses ratio is given by:

$$\frac{P_{SW}}{P_o} = \frac{P_{SWI}}{P_o} + \frac{P_{SWC}}{P_o} = \frac{\sqrt{3}}{\pi m_p F_P} \frac{t_{on} + t_{off}}{T} + \frac{6 C_T Z_0}{m_p^2 F_p T} \tag{15}$$

Notice that both terms increase with the decrease in m_p, however the term related to the parasitic capacitance depends on the square value of m_p as such the influence of this component to the overall losses would be more significant for lower values of m_p.

It is once again important to note that the relation in (15) assumes that the output current is always high enough to ensure that the charge/discharge process of the parasitic capacitors is performed before the end of the deadtime. In practice, since the output current is sinusoidal, it is expected that during a time interval of the fundamental output period an additional losses term needs to be considered. This time interval, t_c, is depicted in Figure 4 and depends mostly on the parasitic output capacitance of the SiC MOSFET, the selected deadtime and the output phase peak current.

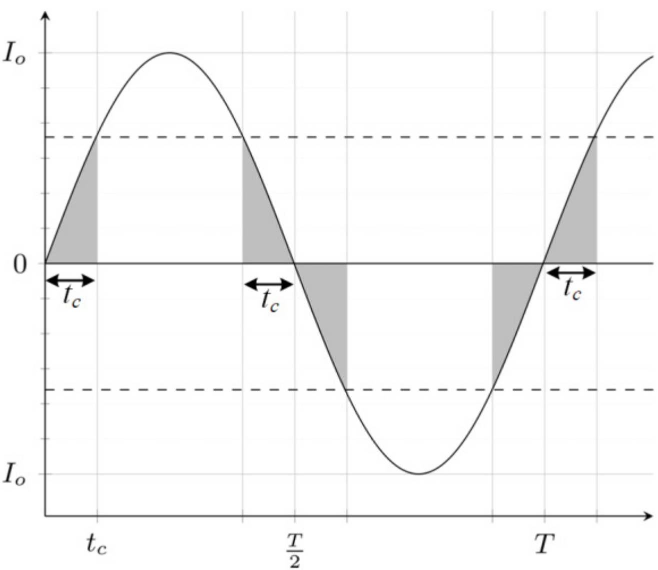


Figure 4. Representation of the zones (in grey) where the combination of deadtime and output current are not enough to respectively charge and discharge the parasitic output capacitances of the SiC MOSFET and SiC Diode in a inverter leg configuration.

Considering the deadtime, t_d, this additional loss term can be shown to be (Appendix A):

$$\frac{P_{SWa}}{P_o} = \left(\frac{\sqrt{3}}{2\pi m_p F_P}\frac{t_{on}+t_{off}}{T} + \frac{3C_T Z_0}{m_p^2 F_p T}\right)\left(2\text{arcsin}\left(\frac{2\sqrt{3}C_T Z_o}{m_p t_d}\right)/\pi\right) \quad (16)$$

The relation in (16) depends on the a priori knowledge of the deadtime which depends on several design parameters. To have a formulation suitable for an early-stage selection of the inverter semiconductors the following approximation is proposed:

$$\frac{P_{SWa}}{P_o} = \left(\frac{\sqrt{3}}{2\pi m_p F_P}\frac{t_{on}+t_{off}}{T} + \frac{3C_T Z_0}{m_p^2 F_p T}\right)(1-m_p) \quad (17)$$

The concept behind this alternative is that for lower values of m_p the expected output current amplitude, for constant Z_0, is also lower and as such the portion of the fundamental output period where the additional losses term is required is also higher. The difference between (16) and (17) will be shown to be negligible in the experimental results.

The switching losses terms with the above-described compensation can be then given by:

$$\frac{P_{SW}}{P_o} = \frac{P_{SWI}}{P_o} + \frac{P_{SWC}}{P_o} + \frac{P_{SWa}}{P_o} = \left(\frac{\sqrt{3}}{2\pi m_p F_P}\frac{t_{on}+t_{off}}{T} + \frac{3C_T Z_0}{m_p^2 F_p T}\right)(3-m_p) \quad (18)$$

The switching losses ratio increases with the switching times, parasitic capacitance, and output load impedance, and reduces with increasing F_p, T, and m_p.

3. Considerations of the Proposed Methodology, Semiconductor Selection, and Case Study

The complete formulation for the three-phase SiC MOSFET inverter can then be given by:

$$\eta = \frac{1}{1 + \frac{P_{ON}}{P_o} + \frac{P_{SW}}{P_o}} = \frac{1}{1 + \frac{R_{DSon}}{F_p Z_0}(1 + THD^2) + \left(\frac{\sqrt{3}}{2\pi m_p F_P} \frac{t_{on}+t_{off}}{T} + \frac{3C_T Z_0}{m_p^2 F_p T} \right)(3 - m_p)} \quad (19)$$

Since the output power factor and the load impedance are not independent variables the proposed formulation can be further simplified to account only for the resistive component of the load impedance, since $F_p = R_0/Z_0$ the converter efficiency can be written as:

$$\eta = \frac{1}{1 + \frac{P_{ON}}{P_o} + \frac{P_{SW}}{P_o}} = \frac{1}{1 + \frac{R_{DSon}}{R_0}(1 + THD^2) + \left(\frac{\sqrt{3}}{2\pi m_p F_P} \frac{t_{on}+t_{off}}{T} + \frac{3C_T R_0}{m_p^2 F_p^2 T} \right)(3 - m_p)} \quad (20)$$

Considering that for a high enough output power, the converter losses are dominated by the semiconductor losses, and then the characteristics of the SIC MOSFET device must fulfill the following:

$$\begin{aligned} R_{DSon} &\leq \lambda \frac{1-\eta}{\eta} \frac{R_0}{(1+THD^2)} \\ t_{on} + t_{off} &\leq (1-\lambda) \frac{1-\eta}{\eta} \frac{2\sqrt{3}}{3} \frac{\pi m_p F_P T}{(3-m_p)} - 2\pi\sqrt{3} \frac{C_T R_0}{m_p F_p} \end{aligned} \quad (21)$$

where λ is the weighting factor allowing a compromise between switching losses and conduction losses. These equations provide a way to size the semiconductor parameters to attain a given efficiency at a given output power.

The relations in (21) allow to roughly size the semiconductor parameters as a function of the converter operating point and the characteristics of the load. Figure 5 illustrates this reasoning. Considering a constant modulation index and a constant power factor Figure 5 shows traces that represent the minimum relation between $t_{on} + t_{off}$ and R_{DSon} to attain a desired efficiency η = 99.3% for different values of R_0. The interpretation of this result can be made as follows: for a load resistance of 11 Ω all semiconductors depicted satisfy the desired efficiency constrain. For a load resistance of 6 Ω only S2 and S5 should be considered. The list of the semiconductor's parameters depicted in Figure 5 can be seen in Table 1.

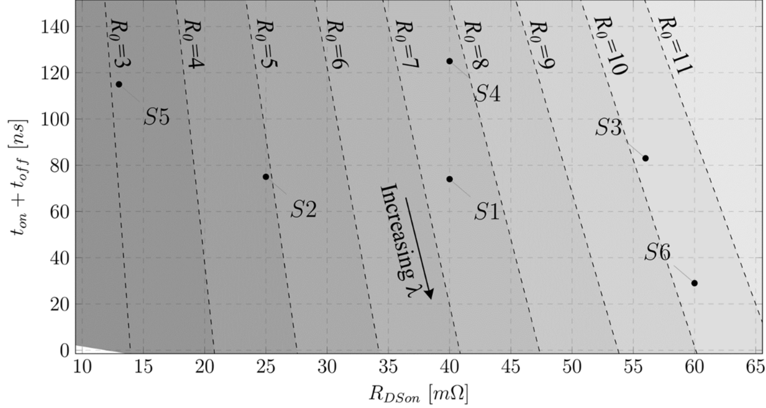


Figure 5. Relation between the SiC MOSFET turn-ON plus turn-OFF times with the channel ON-state resistance for a minimum efficiency of 99.3% at diffent values of the load resistance at constant power factor and modulation index. (R_0 resistance in Ω).

Table 1. List of considered semiconductors and their respective properties shown in Figure 4.

Semiconductor	V_{DSS} [V]	t_{on}+t_{off} [ns]	R_{DSon} [mΩ]	Coss [pF]
S1-Wolfspeed C2M0040120D	1200	74	40	171
S2-Wolfspeed C2M0025120D	1200	75	25	224
S3-OnSemi NTBG040N120SC1	1200	83	56	139
S4-OnSemi NVH4L040N120SC1	1200	107	40	137
S5-Wolfspeed CAS120M12BM2	1200	115	13	980
S6-Infineon AIMW120R060M1H	1200	29	60	58

A similar consideration can be made for a varying power factor keeping everything else constant, as shown in Figure 6. In this illustrative set of conditions with a constant load resistance R_0 = 10 Ω, only the semiconductors S5, S2, and S1 can attain an efficiency of at least 99.3% for a load with a power factor of 0.4 (a value selected to merely illustrate a potential selection process). The visual inspection of both Figures 5 and 6 also reveals that for the selected operating conditions, the requirements for the switching times of the semiconductor are more influenced by the load power factor than from the load resistance, while the requirements for the R_{DSon} will be mostly dictated by the real component of the load impedance.

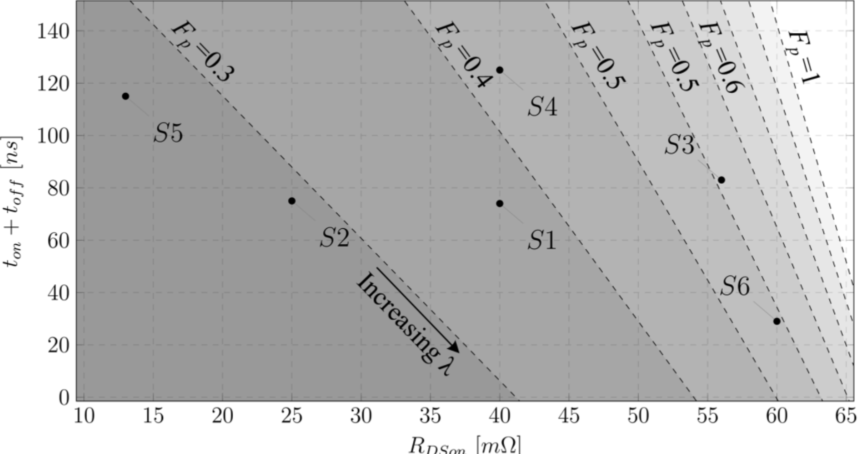


Figure 6. Relation between the SiC MOSFET turn-ON plus turn-OFF times with the channel ON-state resistance for a minimum efficiency of 99.3% at diffent values of the load power factor with a constant output load resistance and modulation index.

Supposing that the power modulation index, the load impedance, and the power factor are all kept constant, and the output power is changed by regulating the DC supply voltage, the partial derivatives of the ratios with respect to the supply voltage yield:

$$\begin{aligned} \frac{\partial P_{ON}/P_o}{\partial U_{DC}} &= 0 \\ \frac{\partial P_{SW}/P_o}{\partial U_{DC}} &= 0 \end{aligned} \tag{22}$$

This shows that the on-state losses ratio and switching losses ratio remain constant for a variable input voltage if Z_0 and m_p are kept constant.

Suppose now that output power is changed by varying the resistive component R_0 of the load impedance Z_0 while the power modulation index and the supply voltage are kept constant. Since $F_p = R_o/Z_0$ the partial derivatives of the losses ratio to the resistive part of the load yield:

$$\begin{aligned} \frac{\partial P_{ON}/P_o}{\partial R_0} &= -\frac{\left(1+THD^2\right)R_{DSon}}{R_0^2} \\ \frac{\partial P_{SW}/P_o}{\partial R_0} &= \frac{3C_T(3-m_p)}{F_p^2 m_p^2 T} \end{aligned} \tag{23}$$

This shows that the switching losses ratio will increase linearly with increasing R_0 as long as F_p, m_p, and T are kept constant. Furthermore, and as expected, the on state losses ratio decreases with increasing R_0 indifferently from the values of m_p, F_p, or T.

Finally, suppose that the output power is changed by varying the modulation index while both the supply voltage and resistive component R_0 of the load impedance are kept constant, the partial derivative of both ratios with respect to m_p yield:

$$\begin{cases} \frac{\partial P_{ON}/P_o}{\partial m_p} = 0 \\ \frac{\partial P_{SW}/P_o}{\partial m_p} = -\frac{\sqrt{3}(t_{on}+t_{off})}{F_p m_p^2 \pi T} - \frac{(6-m_p)3C_T R_0}{F_p^2 m_p^3 T} \end{cases} \quad (24)$$

This shows that the on-state losses ratio will keep constant when varying the power modulation index m_p while the switching loss ratio will decrease with m_p at constant F_p and R_0 although with a smaller derivative for higher value of m_p.

To close the analysis of the proposed loss formulation, a 3-phase SiC MOSFET inverter was considered where the properties of the semiconductor are given by the device S1 of Table 1. Considering a fixed modulation index $m_p = 1$ and a voltage $U_{DC} = 600$ the expected converter efficiency as a function of the load impedance Z_0 is depicted in Figure 7. These results can be quickly attained for a variety of semiconductors with little computational effort allowing to compare a wide range of semiconductors devices. This comparison would be unpractical using most physics based or behavioral models.

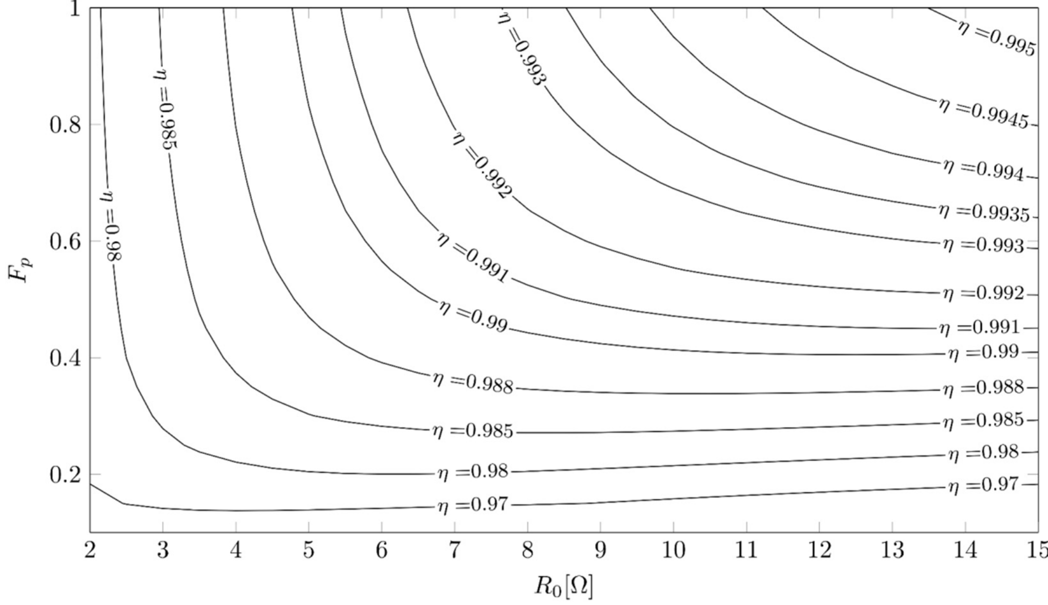


Figure 7. Analytically obtained efficiency of a 3 phase SiC MOSFET Inverter with device S4 from Table 1 as a function of the load impedance here divided in resistance and power factor.

According to the results shown in Figure 7 an inverter designed and built with Wolfspeed C2M0040120D SiC MOSFET (S1) should be able to have an efficiency higher than 99.2% with a load with $R_0 \geq 10\ \Omega$ and $F_p \geq 0.7$.

4. Experimental Results

To obtain experimental validation a three-phase SiC-MOSFET inverter was built and designed with the semiconductor device S1. The resulting inverter is shown in Figure 8, with a resulting power density of 21 kW/L.

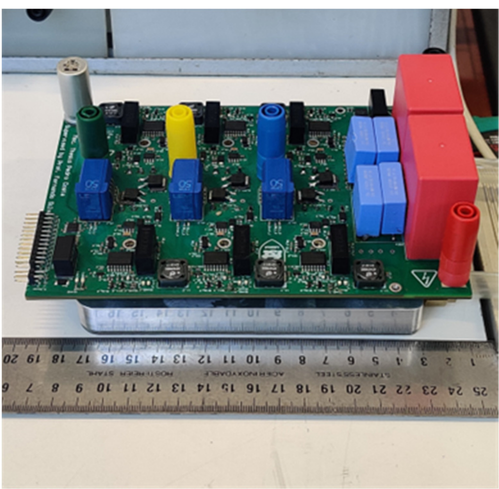


Figure 8. Three-phase SiC MOSFET inverter under test with a water-cooled cooling plate. Ruler scale in cm.

The inverter efficiency was measured at different output powers. Two test setups were performed. In the first test, at constant input DC voltage $U_{DC} = 600$ V, the output power was varied using an adjustable power modulation index. In the second test, at a constant power modulation index $m_p = 1$, the output power was varied by changing the input DC voltage. The inverter efficiency was attained from the direct measurements of the input and output powers. During experiments, the temperature of the inlet water is kept at approximately the ambient temperature of 20 °C.

The experimental setup can be seen in Figure 9. It consists of a 15 kW power supply with embedded output voltage, current, and power measurement (Keysight N8955A), two additional current probes (Center 223 high-resolution clamp meter), a voltmeter (Center 122), the designed inverter system and the respective cooling circuit, a three-phase RL load and a power quality analyzer, Fluke 435-II.

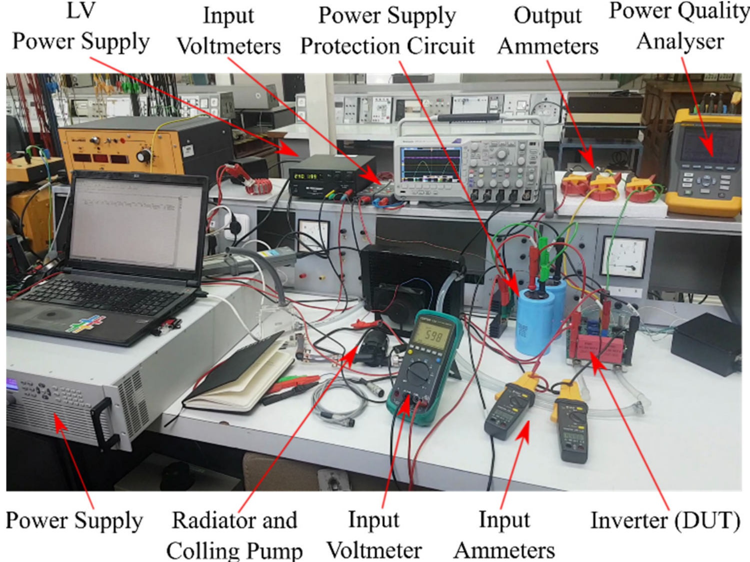


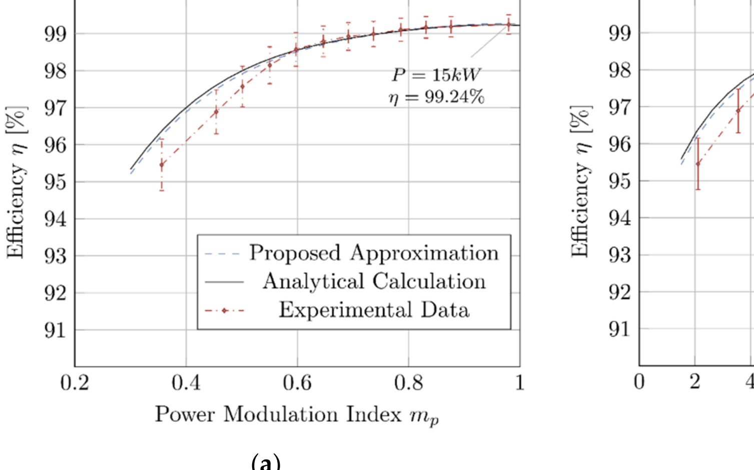
Figure 9. Experimental laboratory setup used to attain the efficiency of the three-Phase SiC Inverter. The 15 kW loads are on the back of the test bench.

All the experiments were made using a space vector pulsewidth modulation (SVM) with a switching frequency $f_{sw} = 20$ kHz with a deadtime $t_d = 100\ ns$ in order to obtain the predicted efficiency of 99.2%. Using the S1 device, higher switching frequencies led to lower efficiencies. An example of an acquisition set for increasing power with constant

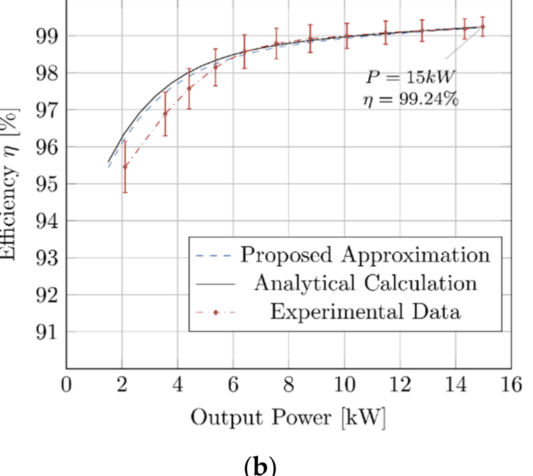
input voltage can be seen in Table 2 showing the obtained experimental efficiency η and the theoretically obtained efficiency using the approximation of (17), η_{t1}, and using directly the influence of the deadtime as per (16), η_2.

Table 2. Example of the acquired and calculated quantities for the results presented in Figure 10.

$\overline{U_{DC}}$ [V]	m	$\overline{I_{DC}}$ [A]	$\overline{P_{in}}$ [W]	$\overline{P_{out}}$ [W]	THD [%]	η [%]	η_{T1} [%] [%]	η_{T2} [%]
598.6	0.356	3.848	2210	2110	5.5	95.45	96.23 [−0.82]	96.37 [−0.96]
598.6	0.454	6.318	3669	3551	4.1	96.77	97.49 [−0.74]	97.61 [−0.87]
598.6	0.501	7.720	4521	4412	3.9	97.57	97.94 [−0.37]	98.03 [−0.47]
598.6	0.550	9.298	5465	5364	3.1	98.15	98.20 [−0.06]	98.28 [−0.14]
598.6	0.597	11.010	6500	6408	2.4	98.57	98.46 [−0.11]	98.53 [−0.05]
598.6	0.647	12.913	7638	7546	2.1	98.79	98.67 [−0.11]	98.72 [−0.07]
598.6	0.692	14.963	8865	8770	1.4	98.92	98.83 [−0.09]	98.87 [−0.05]
598.6	0.737	17.160	10,186	10,083	1.0	98.99	98.97 [−0.02]	98.99 [−0.05]
598.6	0.786	19.480	11,583	11,480	0.8	99.10	99.05 [−0.05]	99.07 [−0.04]
598.5	0.831	21.633	12,902	12,795	0.8	99.17	99.12 [−0.05]	99.13 [−0.04]
598.5	0.876	24.153	14,442	14,325	0.6	99.18	99.15 [−0.03]	99.16 [−0.02]
598.5	0.978	25.203	15,087	14,973	0.5	99.24	99.23 [−0.01]	99.23 [−0.02]



(**a**)



(**b**)

Figure 10. Efficiency vs. Power Modulation Index (**a**) and Output Power (**b**) comparison between experimental results (dashed) and analytical calculation.

The comparison between the experimentally obtained efficiencies and the analytical calculations obtained from the loss formulations are graphically depicted in Figure 9, the presented measurement errors are further discussed in Appendix B which discusses the uncertainty analysis.

The results shown in Figure 10 compare the experimental results with the proposed analytical formulation. The solid line represents the expected efficiency when computing the switching losses as per (16). The dashed line represents the proposed approximation of the switching losses as per (17). The results show that the proposed approximation closely follows the analytical formulation that depends on the deadtime.

From around 5 kW to 15 kW, the deviation is lower than 0.2%, corresponding to modulation indexes higher than 0.5; however, for lower output powers, the measured efficiencies are lower than the ones predicted (nearly 1% prediction error). Despite being within the estimated measurement uncertainty there is a clear trend for higher deviation in lower modulation indexes. Three main factors are pointed out as potential reasons for this difference: 1—The proposed formulation only accounts for the semiconductor

losses not considering other losses sources such as the input capacitors, drivers, and corresponding isolated power supplies, whose losses start to be significant at lower output powers; 2—For lower modulation indexes, the approximation for the deadtime influence considered in Appendix A can be insufficient if, for most of the fundamental output period, the deadtime is not enough to circulate the energy between the two capacitors; 3—The analytical results assume a constant load, therefore excluding small variations due to load different operating temperatures.

The distinct contribution of the switching and conduction losses for the results obtained in Figure 10 can be seen in Figure 11 computed according to the proposed analytical formulation. These results can provide insight to the designer on potential efficiency gains. As expected, the switching losses have a higher relative contribution for lower output powers where the influence of the deadtime in the switching losses is higher.

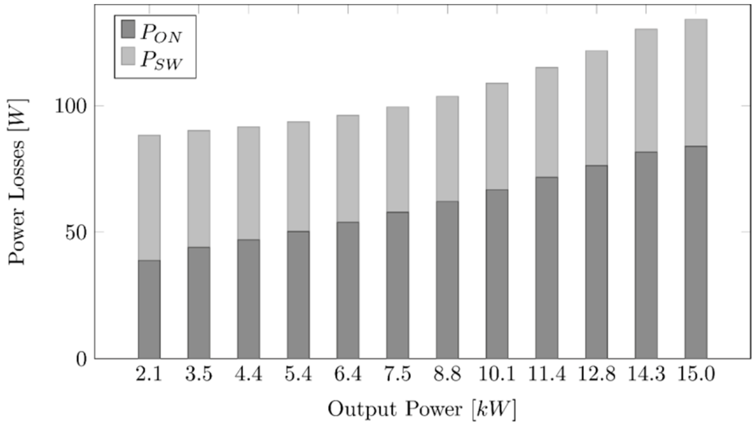


Figure 11. Analytical estimation of the separate contribution of conduction and switching losses for the total losses measured in the experimental setup.

Figure 12 shows the obtained results for an experimental setup where the output power was varied by increasing the DC input voltage with a constant power modulating index m_p, and a constant output impedance Z_0. Once again, there is a visible deviation (but within measurement uncertainty) of around 0.2% for smaller input voltages (Figure 12a), but a closer prediction for output powers higher than 4 kW (Figure 12b). Notice that according to (22), the efficiency should hold constant; the discrepancies for lower output powers are once again justified mainly from additional losses besides the semiconductor losses and not accounted for in the analytical formulation.

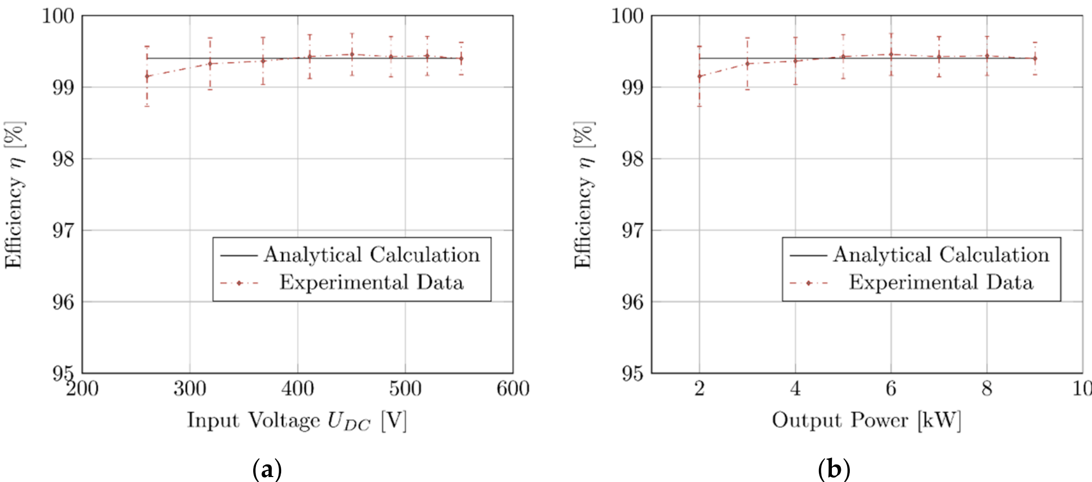


Figure 12. Efficiency vs. Input Voltage (**a**) and output power (**b**) comparison between experimental results (dashed) and analytical calculation (solid).

5. Conclusions

This work proposed an efficiency-oriented formulation for SIC semiconductor selection and efficiency prediction of a three-phase inverter considering the semiconductor losses. The formulation is suited for the correct sizing of the semiconductors to attain a given efficiency goal, using only the SiC manufacturers data and required output power and load. The formulation considers the influence of the THD in the conduction losses as well as the influence of the deadtime in the switching losses. These results are of practical validity for an early sizing of the semiconductor parameters for a given target efficiency or to evaluate the potential efficiency for a given semiconductor.

The proposed formulation does not make assumptions on the modulation schema or controller making only use of the application-specific parameters (input and output voltages, output power ...) and semiconductor characteristics (t_{on}, t_{off}, R_{DSon} ...) making an even more practical approach for early design stage semiconductor sizing.

A SiC MOSFET inverter was built and planned for a target efficiency (at the nominal operating point) of at least 99.2% using the proposed sizing method. A set of experimental measurements of efficiency was made for a varying output power with a varying modulation index, and a varying output power with a varying input voltage, both with constant loads. Results of said measurements were compared with predictions taken from the proposed formulation. Nominal output power led to an efficiency around 99.2% with estimation errors smaller than 0.1%.

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Data Availability Statement: No new data were created or analyzed in this study. Data sharing is not applicable to this article.

Conflicts of Interest: The authors declare no conflict of interest.

Appendix A

Assuming a constant load current during the commutation time and rise and fall voltages across the SiC MOSFET with constant slopes, the minimum output current, i_{Lmin} that can discharge one output capacitance, C_T, and charge another output capacitance C_T is given by:

$$i_{L\min} = \frac{2C_T U_{DC}}{t_d} \quad \text{(A1)}$$

Describing a single-phase current as $\sqrt{2}I_{orms}\sin(\omega t)$ equaling to the current i_{Lmin} and solving for time yields:

$$\sqrt{2}I_{orms}\sin(\omega t) = I_c \Rightarrow t_c = \arcsin\left(I_c/\sqrt{2}I_{orms}\right)/\omega \quad \text{(A2)}$$

The time t_c represents the time at which the output phase current equals the minimum current i_{Lmin}. Replacing (A1) in (A2) and using the relation for I_{orms} described in (6) it is possible to further simplify t_c to:

$$t_c = \arcsin\left(\frac{2C_T U_{DC}\sqrt{6}Z_o}{\sqrt{2}m_p U_{DC} t_d}\right)/\omega = \arcsin\left(\frac{2\sqrt{3}C_T Z_o}{m_p t_d}\right)/\omega \quad \text{(A3)}$$

During a full period of the output current wave the time portion, τ, where the output current is not enough to fully charge and discharge the output parasitic capacitances is given by:

$$\tau = 4\frac{t_c}{T} = 4\text{arcsin}\left(\frac{2\sqrt{3}C_T Z_o}{m_p t_d}\right)\frac{1}{2\pi f_{sw} T} = \frac{2}{\pi}\text{arcsin}\left(\frac{2\sqrt{3}C_T Z_o}{m_p t_d}\right) \quad \text{(A4)}$$

Considering that $Z_0 = R_0/F_p$ then:

$$\tau = \frac{2}{\pi}\text{arcsin}\left(\frac{2\sqrt{3}C_T R_0}{m_p F_p t_d}\right) \quad \text{(A5)}$$

Finally following the same the same methodology as the one presented for the switching losses it can be assumed that an additional set of 3 commutations needs to be considered. This can be performed with the same formulation presented above with the additional factor of τ and $\frac{1}{2}$. The τ factor represents the fraction of the output period that the additional commutations are taking place. The $\frac{1}{2}$ factor is justified because for these additional commutations the capacitors voltages have been partially discharged/charged during the deadtime which on average results that the switching is conducted with half of the U_{DC} voltage.

$$\frac{P_{SWa}}{P_o} = \frac{1}{2}\left(\frac{P_{SWI}}{P_o} + \frac{P_{SWC}}{P_o}\right)\tau = \left(\frac{\sqrt{3}}{2\pi m_p F_P}\frac{t_{fu}+t_{ri}}{T} + \frac{3C_T Z_0}{m_p^2 F_p T}\right)\left(2\text{arcsin}\left(\frac{2\sqrt{3}C_T Z_o}{m_p t_d}\right)/\pi\right) \quad \text{(A6)}$$

Appendix B

Efficiency was computed as the quotient between the output and input measured powers. The input power measurement was made indirectly through the measurement of the input voltage and input current which were both measured with multiple devices and multiple samples per device.

The input current was measured using the embedded measurement of the power supply with an uncertainty $\Delta i_1 = 60$ mA and two current clamp meters with an uncertainty $\Delta i_{2,3} = 1\% i_x + 5$ mA where i_x is the measured value of the current for each current clamp meter.

The input voltage is measured by a similar process, using the embedded measurement of the power supply with an uncertainty $\Delta v_1 = 1.5$ V and two voltmeters with uncertainties $\Delta v_{2,3} = 0.2\% v_x + 0.2$ V where v_x is the measured voltage. The output power was measured by a direct power measurement with $\Delta p_{ac1} = 1\% p_{acx}$ where p_{acx} is the measured power and by the measurement of the RMS values of the current and voltage and the power factor with uncertainties $\Delta v_{ac} = 0.1\% v_{acx}$, $\Delta i_{ac} = 0.25\% i_{acx} \pm 0.05$ A and $\Delta FP = 0.1\% FP_x$ where v_{acx}, i_{acx} and FP_x are the measurements of the AC voltage, AC current, and power factor respectively.

The final measurement for each quantity is obtained through a weighted mean with the form:

$$\overline{x} = \sum_{j=1}^{k} \alpha_j x_j \quad , \quad \alpha_i = \frac{\Delta_j^{-1}}{\sum_{l=1}^{k} \Delta_l^{-1}} \quad , \quad j = 1,\ldots,k \quad \text{(A7)}$$

where Δ_j is the uncertainty associated with the measurement j, and k is the total number of measurements including the measurements from different equipment. Notice that $\sum \alpha_j = 1$. The combined uncertainty for each measurement is then given by [34]:

$$\overline{\Delta}_j = \sqrt{\frac{1}{\sum_{i=1}^{k} 1/\Delta_i^2}} \quad \text{(A8)}$$

To obtain the uncertainty of the input power measurement the uncertainty propagation must be taken into account, the relative uncertainty of the input power measurement can be given by:

$$\frac{\overline{\Delta}_p}{\overline{p}} = \sqrt{\left(\frac{\overline{\Delta}_v}{\overline{v}}\right)^2 + \left(\frac{\overline{\Delta}_i}{\overline{i}}\right)^2} \quad \text{(A9)}$$

The output power relative uncertainty is given as a combination of direct power measurement uncertainty and the uncertainty from the power computed through the output voltage current and power factor using (A7) and (A8), where Δp_{ac2} is obtained by:

$$\frac{\overline{\Delta}_{pac2}}{\overline{p}_{ac}} = \sqrt{\left(\frac{\overline{\Delta}_{vac}}{\overline{v}}\right)^2 + \left(\frac{\overline{\Delta}_{iac}}{\overline{i}}\right)^2 + \left(\frac{\overline{\Delta}_{FP}}{\overline{FP}}\right)^2} \quad \text{(A10)}$$

The uncertainty of the efficiency measurement can be obtained by the propagation of the relative uncertainties through the quotient of the powers:

$$\frac{\Delta_\eta}{\overline{\eta}} = \sqrt{\left(\frac{\overline{\Delta}_p}{\overline{p}}\right)^2 + \left(\frac{\overline{\Delta}_{pac}}{\overline{p}_{ac}}\right)^2} \quad \text{(A11)}$$

Since the absolute uncertainties depend on the measured values the efficiency uncertainty varies along the power profile, with a maximum absolute value of 0.81% at the lower output powers, and a minimum of 0.26% at the maximum value.

Each of the results in Figures 10 and 12 depicts the obtained uncertainties for each measurement along the output power variation. Notice that the higher the output power the lower the uncertainty.

To further reduce the uncertainty of the measured efficiency other measurement methods should be considered, such as the indirect measurement of the losses through temperature increase [35,36].

It is important to notice that the experimental data and uncertainty are related to the total power losses, while the analytical data only accounts for the losses of the MOSFETS justifying the difference for lower output powers.

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