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Design and Real-Time Implementation of a Control System for SiC Off-Board Chargers of Battery Electric Buses

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Abstract: Emerging wide bandgap (WBG) semiconductors, such as silicon carbide (SiC), will enable chargers to operate at higher switching frequencies, which grants the ability to deliver high power and enhances efficiency. This paper addresses the modeling of a double-sided cooling (DSC) SiC technology-based off-board charger for battery electric buses (BEBs) and the design of its control and real-time (RT) implementation. A three-phase active front-end (AFE) rectifier topology is considered in the modeling and control system design for the active part of the DC off-board charger. The control system consists of a dual-loop voltage–current controller and is used to ensure AC to DC power conversion for charging and to achieve the targeted grid current total harmonic distortion (THD) and unity power factor (PF). Linear and nonlinear simulation models are developed in MATLAB/Simulink for optimum control design and to validate the voltage and current control performances. Four types of controllers (i.e., proportional–integral (PI), lead–lag, proportional–resonant (PR), and modified proportional–resonant (MPR)) are designed as current controllers, and a comparative analysis is conducted on the simulation model. In addition, the final design of the dual-loop controller is implemented on the RT–FPGA platform of dSpace MicroLabBox. It is then tested with the charger to validate the control performance with experimental data. The simulation and experimental results demonstrate the correct operation of the converter control performance by tracking the reference commands.

Keywords: e-bus; wide bandgap; active front end; off-board charger; control; real-time implementation; simulation modeling

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1. Introduction

The share of battery electric buses (BEBs) used in public transportation is steadily increasing every year, as BEBs are beneficial in our battle against global warming, considering the electric energy comes from a clean energy mix. However, an appropriate off-board charging infrastructure is required to charge BEBs in an efficient way. Such chargers are intended to have high power ratings and fast charging speeds, and are less limited by size or weight [1]. They consist of power electronic converters (PECs), which transform three-phase incoming AC grid power into a variable DC output power to charge the battery of the BEB. PECs are designed to protect the power quality of the grid through the consumption of a sinusoidal current, which reduces the THD of the line current with PF control in order to comply with international standards, such as IEC-1000-3-2 and IEEE-519 [2]. They are also designed to charge batteries with variable voltages and current levels while keeping the batteries safe [3].

Recently, advanced WBG materials (SiC and GaN) have been introduced into the switching technology of PECs [4,5]. Semiconductor materials based on WBG technology

offer interesting features over traditional Si materials, as shown in Figure 1. These include high voltage operation and a low leakage current, high-frequency operation, high thermal conductivity, high electron saturation speed, and high electron mobility. Traditional Si semiconductor-based PECs are commercially available. Studies show that WBG-based semiconductor technology has advantages over standard Si devices. SiC reduces power losses by 25% and volume by 50% by operating at a high frequency [6,7]. Accordingly, SiC-based semiconductors are very suited for BEBs' DC charger applications due to their high switching frequency, high voltage, high power, and high-temperature operation. However, state-of-the-art research is needed to integrate WBG-based devices into existing and new applications. Indeed, there is a lack of accurate models of such systems and new controllers to cope with the devices' high switching frequencies and fast dynamics. Moreover, the commercially available off-board chargers for BEBs mostly have an efficiency >95% [8]. This research aims to design a charger for the specification of BEBs to enhance efficiency >97% and reduce size and weight through the integration of WBG semiconductors.

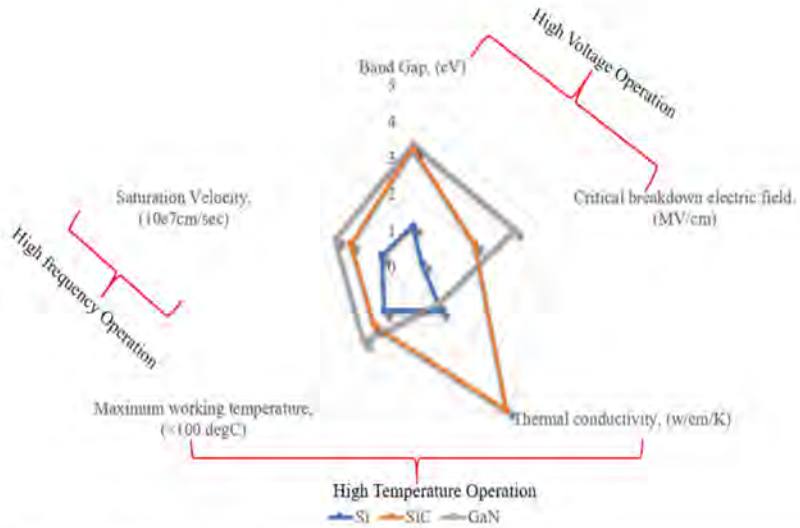


Figure 1. Characteristics of Si, SiC, and GaN.

Numerous control techniques have been discussed in the literature to prevent high energy transfer damage at high power [9]. Most control procedures were established for grid-side AFE converter applications. They are based on direct active and reactive power control [10]. The conventional technique of battery chargers is known as constant current–constant voltage (CC–CV). The basic premise of this technique is that the battery is charged to a certain voltage with a maximum constant current according to cell capacity and then charged at a constant voltage until the drawn current decreases to C/10 or less, where C states the charge or discharge rate of the battery over one hour. The CC–CV control helps to speed up the battery charging time. Thus, a standard dual-loop control strategy is proposed for the application of high power and high voltage DC off-board chargers of BEBs. The controller controls the DC battery voltage and current through active–reactive power control. The new vision of this study is to integrate the WBG SiC semiconductor and appropriate control approach for the emerging application of BEBs off-board chargers. Another study is needed to determine which controller, such as PI, Lead-League, PR, or MPRC, is relevant for the high-frequency dynamics of SiC devices and the high-power DC chargers of BEBs. The outer loop controls the battery parameters, and the inner loop controls the grid powers and quality [10]. The inner loop control bandwidth is chosen based on the operating frequency of the switching device to achieve the desired response [11,12].

Research shows that the control design and implementation of accurate real-time controllers is another challenge for PECs. Conventionally, digital embedded controllers such as microprocessors, microcontrollers, and digital signal processors (DSPs) have been used to implement pulse-width modulation (PWM) algorithms for PECs. However, tech-

niques based on these controllers have the disadvantages of limited functionality and low computational speed for complex PWM circuits [13]. Xilinx has developed a programmable logic tool called Field-Programmable Gate Array (FPGA) [14]. It can be applied to real-time hardware-in-the-loop (HIL) implementation due to its performance, computing capacity, and ability to perform parallel data processing [14]. An FPGA consists of thousands of logic gates grouped together as configurable logic blocks to facilitate high-level circuit design [15]. They are preferred for prototyping application-specific integrated circuits (ASICs) because of their configuration and program capabilities [13].

FPGAs provide significant opportunities for power electronic applications and real-time hardware emulation. Currently, FPGAs appear as an alternative to the digital control of high-frequency PWM converters over DSPs and DSCs. Rapid control prototyping (RCP) platforms based on FPGAs, such as dSPACE and Opal-RT, are new technologies for designing and validating controllers in model-in-the-loop (MIL) simulations without actually implementing them in hardware systems [16]. Such platforms can be used for reconfigurability, co-simulation, HIL, automated Verilog hardware description language (VHDL) code generation, and system scalability, and enable embedded design engineers to quickly build state-of-the-art digital control algorithms while reducing design and testing time [17–19]. Therefore, RCP–FPGA is probably the most suitable tool for implementing all the digital functions of WBG-based power converters. It highlights the potential of such devices as it demonstrates the need for high-frequency control and modulation [20,21].

This research is also dedicated to implementing real-time controls in the FPGA platform so that WBG devices can be integrated into state-of-the-art applications to operate at higher frequencies beyond the limits of the conventional DSP.

The DSC SiC MOSFET based on advanced technology is used for charger development. A new double-sided liquid cooling concept has been applied to cool the charger's DSC modules at a high power. The control strategy is designed for the SiC off-board charger to charge the batteries in different operational modes with voltage and current control. The controller is designed using the analytical model according to the passive filters of the converter, then tested in simulation at rated power. Disturbance rejection analyses are performed in simulations before implementing real time (RT) to determine which controller is suitable for this application. Four types of controllers, namely the PI, lead–lag, PR, and MPR controllers, are analyzed in simulation. The discrete FPGA-based controller is implemented on RT dSpace microlabbox using Xilinx Vivado. Finally, a test is performed on an experimental setup based on DSC SiC modules at 40 kHz. It demonstrates the behaviour of an off-board charger with compact DSC SiC switches to contribute to all studies dedicated to WBG semiconductors in Electrical Vehicle (EV) applications. The results can be used to develop compact and highly efficient EV converters. The FPGA-based implemented controller can also generate PWM signals at higher switching frequencies such as 100 kHz and 200 kHz.

This paper is arranged into different sections. Section 2 of this paper describes the system architecture. Section 3 clearly illustrates the linear modeling and control design optimization. In Section 4, the results of the dynamic simulation model are explained. Section 5 is dedicated to the real-time implementation of the controller in FPGA/Xilinx of dSpace MicrolabBox, whereas Section 6 describes the experimental setup and experimental results. Finally, the conclusions are provided in Section 7.

2. System Architecture

The three-phase AFE converter was selected in this study, since it is often employed in high-power applications. As shown in Figure 2, the architecture comprises of a low frequency (LF) isolation transformer, an inductor–capacitor (LC) filter, and a SiC-based AC/DC converter operating at a 40 kHz switching frequency [14], which converts three-phase incoming AC power into a variable DC output power. For the controller design and to get the best potential outcomes in terms of performance, efficiency, and power losses, accurate modelling of this AFE converter is essential [5,22].

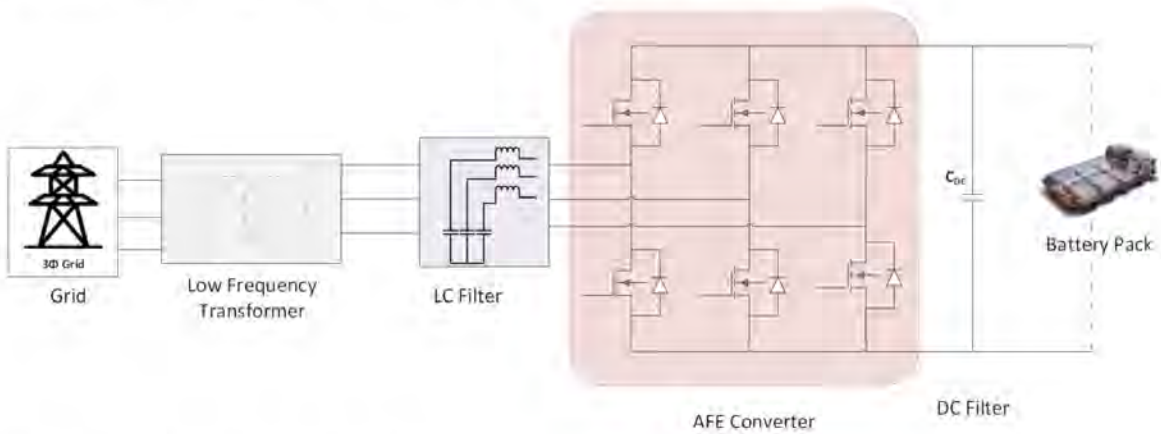


Figure 2. Off-board charger topology.

3. System Modeling and Control Design

3.1. Linear Modeling

Deriving the mathematical or linear model of a system is a long process. Models are necessary for understanding the system's dynamics and for verifying compliance with the system's requirements. In the form of state space, a linear model was built based on the generalized system model. This linear model was used for offline control design and stability and controllability analysis. In dq0 frames of reference, the linear model of the AFE converter (as depicted in Figure 3) was generated [7,22].

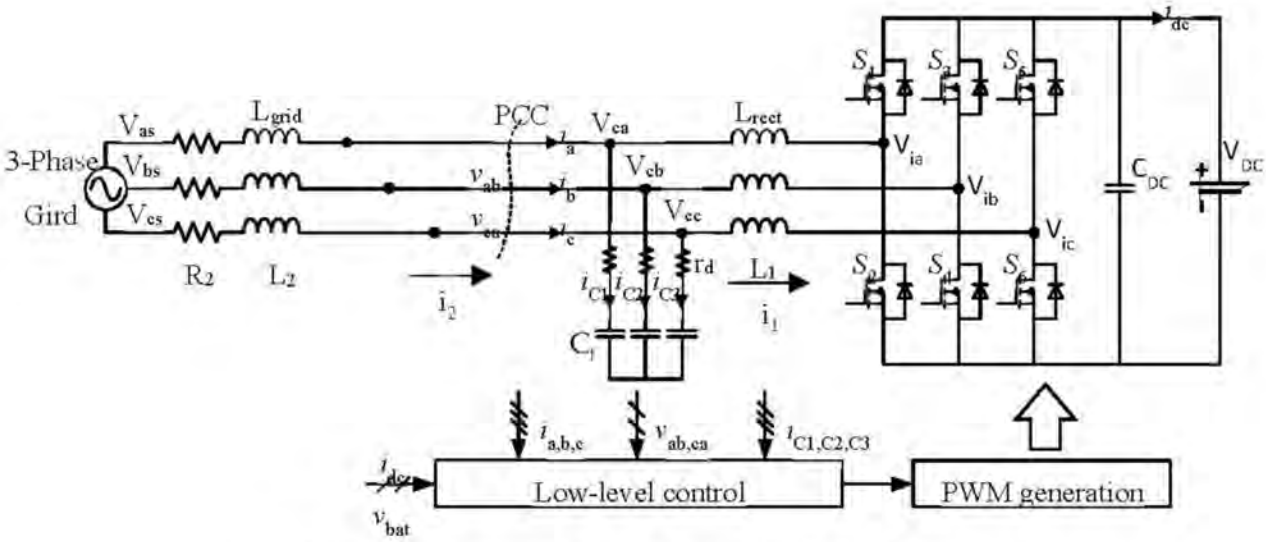


Figure 3. Circuit and control diagram of the SiC off-board charger.

The high rated power of the AC–DC converter needed to guarantee a high PF on the AC grid and an appropriate total harmonic distortion (THD) for the grid line currents.

The off-board charger's specifications and AC and DC passive filters are illustrated in Table 1.

Table 1. Charger specifications.

Parameters	Value
Power (P, kW)	175
Line frequency (f_{AC}, Hz)	50
Switching frequency ($f_{sw,}$ kHz)	40
AC voltage (V_{AC}, V)	400
DC Voltage (V_{dc}, V)	600–800
Rectifier inductor (L_{rect}, uH)	100
Grid inductor (L_{grid}, uH)	1
Capacitor (C_f, uF)	10
Damping resistance (r_d, Ohm)	0.04
DC capacitor (C_{dc}, mF)	0.85

An analytical-based model was created for the off-board charger of the AC–DC converter. Equations (1)–(7) were derived in a dq0- frame of reference for the AFE three-phase converter, also based on Figure 3 [22]. The differential first-order equations with LCL filter and DC filter were used to create the state space linear model [11,12].

$$V_{ds} = R_{l2}i_{2ds} + R_d i_{2ds} + L_2\frac{di_{2ds}}{dt} - \omega L_2 i_{2qs} + V_{cd} - R_d i_{1ds} \tag{1}$$

$$V_{qs} = R_{l2}i_{2qs} + R_d i_{2qs} + L_2\frac{di_{2qs}}{dt} + \omega L_2 i_{2ds} + V_{cq} - R_d i_{1qs} \tag{2}$$

$$0 = -i_{2ds} + C_f\frac{dV_{cd}}{dt} - \omega C_f V_{cq} + i_{1ds} \tag{3}$$

$$0 = -i_{2qs} + C_f\frac{dV_{cd}}{dt} + \omega C_f V_{cd} + i_{1qs} \tag{4}$$

$$-V_{ids} = R_{l1}i_{1ds} + R_d i_{2ds} + L_1\frac{di_{1ds}}{dt} - \omega L_1 i_{1qs} - V_{cd} - R_d i_{2ds} \tag{5}$$

$$-V_{iqs} = R_{l1}i_{1qs} + R_d i_{1qs} + L_1\frac{di_{1qs}}{dt} + \omega L_1 i_{1ds} + V_{cq} - R_d i_{2qs} \tag{6}$$

$$C_{DC}\frac{dV_{dc}}{dt} = \frac{3}{2}M_d i_{1ds} + \frac{3}{2}M_q i_{1qs} - \frac{V_{dc}}{R} \tag{7}$$

where V_{ds}, V_{qs}, V_{0s} [V] are the grid AC voltages; i_{2ds}, i_{2qs}, i_{1ds}, i_{1qs} [A] are the AC currents of the grid and inductor side, respectively, in the dq0 frame; V_{DC} [V] is DC voltage, V_{id}, V_{iq} [V] are converter voltages; [V] are voltages across the AC capacitor; and M_d, M_q are modulation indices in the dq reference frame. [μH] is the grid inductance and L_1 [μH] is the converter side inductance. The line voltages angular frequency ω [rad/s] is represented by $\omega = 2\pi f_{AC}$.

The generalized state-space model of the AC–DC converter was obtained in A, B, C, and D matrices for the dq0 reference frame, as mentioned in Equations (9) and (10).

$$\frac{dx}{dt} = Ax + Bu \tag{8}$$

$$y = Cx + Du \tag{9}$$

A generalized state-space model of A, B, C, and D matrices was derived after solving the first-order differential equations of the LCL filter and DC filter for the three-phase AC/DC converter in the dq axis. For optimum control design and disturbance rejection analysis, this state-space model was used. $x = \left[i_{2d}\ i_{2q}\ V_{cd}\ V_{cq}\ i_{1d}\ i_{1q}\ V_{dc}\right]^T$, $u = \left[V_{id}\ V_{iq}\ V_{ds}\ V_{qs}\ \right]^T$

$$A = \begin{bmatrix} -\frac{R_l+R_d}{L_2} & \omega & -\frac{1}{L_2} & 0 & \frac{R_d}{L_2} & 0 & 0 \\ -\omega & -\frac{R_l+R_d}{L_2} & 0 & -\frac{1}{L_2} & 0 & \frac{R_d}{L_2} & 0 \\ \frac{1}{C_f} & 0 & 0 & \omega & -\frac{1}{C_f} & 0 & 0 \\ 0 & \frac{1}{C_f} & -\omega & 0 & 0 & -\frac{1}{C_f} & 0 \\ \frac{R_d}{L_1} & 0 & \frac{1}{L_1} & 0 & -\frac{R_l+R_d}{L_1} & \omega & 0 \\ 0 & \frac{R_d}{L_1} & 0 & \frac{1}{L_1} & -\omega & -\frac{R_l+R_d}{L_2} & 0 \\ 0 & 0 & 0 & 0 & \frac{3d_d}{2C_{DC}} & \frac{3d_q}{2C_{DC}} & -\frac{1}{RC_{DC}} \end{bmatrix}, B = \begin{bmatrix} 0 & 0 & \frac{1}{L_2} & 0 \\ 0 & 0 & 0 & \frac{1}{L_2} \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ -\frac{1}{L_1} & 0 & 0 & 0 \\ 0 & -\frac{1}{L_1} & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix}, C = [1]_{7\times7}, D = [0]_{7\times4}$$

3.2. Control Design and Optimization

The control system of the charger delivered DC voltage regulation. The approach adjusted the required voltage according to charging demand and checked the amount of line current passing through the converter and its ripple. The PWM signals for the six switches of the three-phase AC–DC converter inside the off-board charger were generated by the control system. As shown in Figure 4, the control consisted of an outer DC bus voltage control loop and an inner dq-current control loop. In control design optimization, control performance was optimized by tuning control gains to achieve appropriate overshoot, undershoot, rise time, and settling time. In addition, different types of controllers were designed and implemented in simulation to find a suitable controller for this application, namely PI, Lead-League, PR, and MPR controllers.

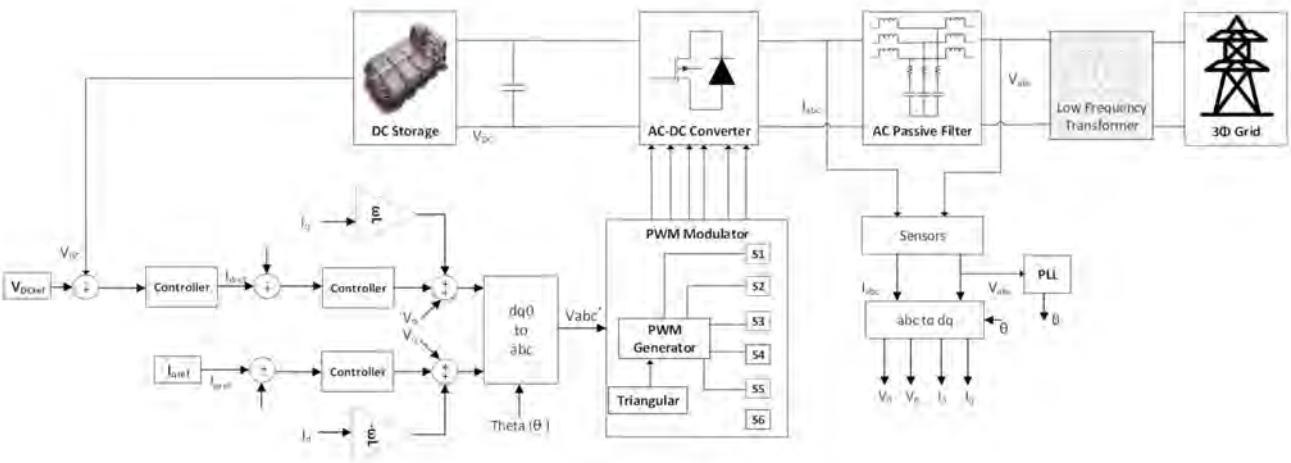


Figure 4. Classical dual-loop control of charger.

Three controllers were used in the classic control of DC voltage and current for three-phase AC–DC converters. One outer-loop voltage controller tracked Vdc [V], and the other two inner-loop current controllers were for Id and Iq [A]. One of the transformation methods, such as the zero-order hold (ZOH), Tustin's, and modal methods, was used to discretize the continuous-time multi-input multi-output (MIMO) model. Two methods of transformation were utilized here such as Tustin's and modal methods. The digital z-domain controller was designed by means of methods such as the continuous-time frequency response. Figure 4 provides the complete dual outer and inner loop, comprising the voltage and current controller. A controller was constructed by means of a linear model with the inclusion of sensor delays and computational delays [23].

The overshoot, rise time, settling time, integral absolute error (IAE), and integral time absolute error (ITAE) could all be reduced by tuning the controller using an optimization algorithm [24].

The state-space linear model of the AFE converter was used to design PI controllers in this study. The first-order differential equation was used to derive the AFE converter's state-space model in the reference dq frame [22]. The closed-loop control design included

the sensors and PWM delays, i.e., 10 µs for voltage sensor (LEM DVC 1000-P) delay, 3 µs for current sensor (ISB-425-A-802), and 0.5 µs for PWM. After a close-loop analysis, the PI controller was tuned according to margins and frequencies. The inner loop current PI controllers were designed at <1/10 of the switching frequency, and the outer closed-loop voltage control was designed at 50 Hz line frequency. The gain margin (gM) at the gain crossover frequency (ωcg) and phase margin (PM) at the phase crossover frequency (ωcp) of the voltage control were 22.3 dB at (2.11×10^3 rad/s) and 58° at (346 rad/s), and of the current control were 33.9 dB at (3.17×10^5 rad/s) and 51° at (1.73×10^3 rad/s).

Then, in an offline (closed-loop linear model) and online (closed-loop simulation model) setup, their results were compared. At a minimum value of the objective function, i.e., ITAE and IAE of the voltage error, the controller's robustness could be achieved. The PI, lead–lag, PR, and MPR control of current controllers were designed at the same margins and frequencies, as shown in the Bode plot in Figure 5. Then, their performances were compared in an offline (with closed-loop linear model) and online (closed-loop simulation model) setup. The robustness of the controller could be observed at a minimum value of the objective function, i.e., ITAE and IAE of the voltage error. The transfer functions of the PI, lead–lag, PR, and MPR controls [2,24–27] are shown in Table 2. This analysis of ITAE and IAE of the voltage error was carried out in a non-linear simulation of the charger and is shown in Table 3. The transfer functions of controllers, gM, PM, ωcp, and ωcg, are also tabulated in Table 3.

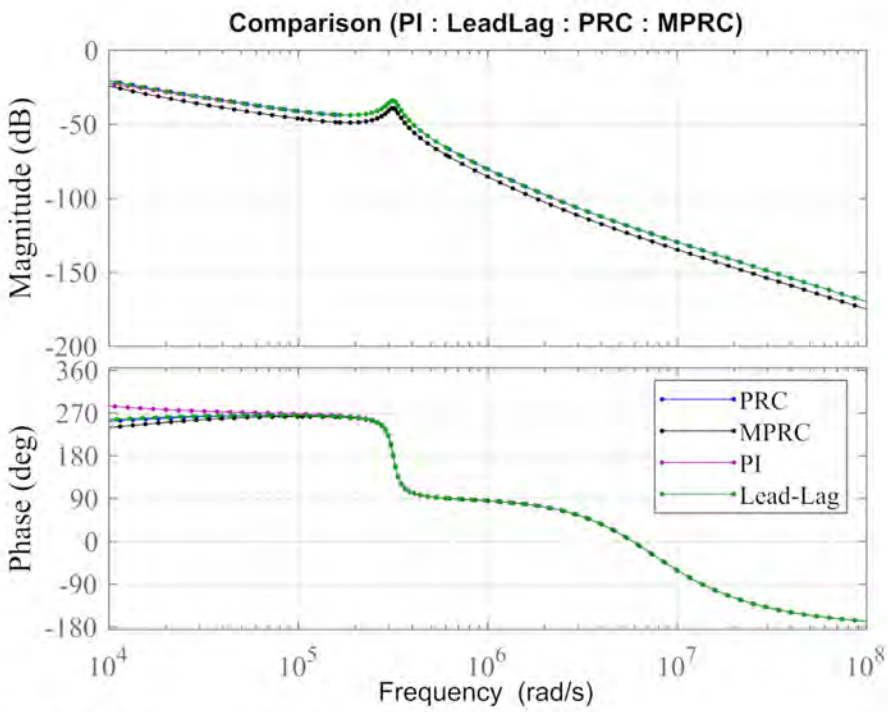


Figure 5. Bode plot comparison of PI, lead–lag, PRC, and MPRC.

For the PR control, the proportional gain K_p related the system's dynamic response, the resonant gain K_r regulated the phase shift of reference and output, and resonant frequency ω_0 was set to 50 Hz (314.16 rad/s). In the procedure of design of MPR control, four parameters were considered: proportional gain K_p, resonant gain K_r, ω_c, and ω_0. The resonant frequency ω_0 can be considered as 50 Hz (314.16 rad/s). All control transfer functions are elaborated on in Table 2 [18–21]. The control design parameters of all controllers are illustrated in Table 3.

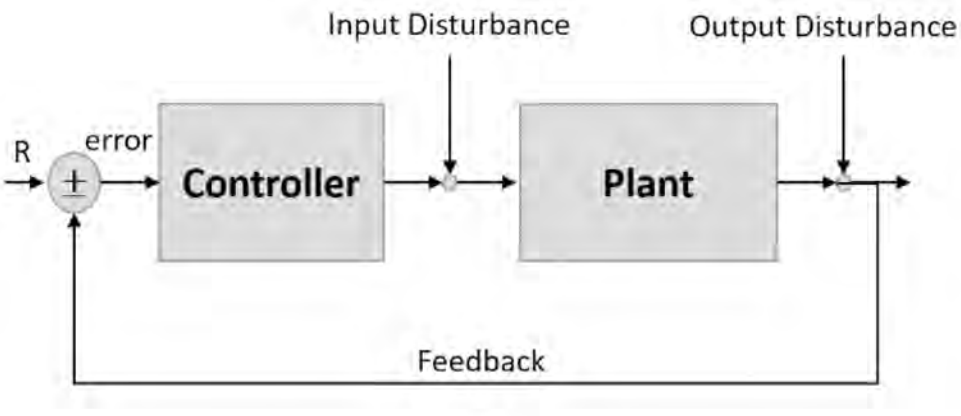
Table 2. Generalized controllers.

Controller	Generalized Transfer Function
PI	$K_p + \frac{K_i}{s}$
Lead–Lag	$\sqrt{\alpha}\frac{s+\frac{\omega_0}{\sqrt{\alpha}}}{s+\omega_0\sqrt{\alpha}}$ $-180^{\circ} < \theta < 180^{\circ}$, $\alpha = \frac{1+\sin\theta}{1-\mathrm{Sin}\ \theta}$
Proportional Resonance	$K_p + \frac{2K_r s}{s^2+\omega_0^2}$ $\omega_0 = 2\pi f\ (\mathrm{rad/s})$,
Modified Proportional Resonance	$K_p + \frac{2K_r\omega_c s}{s^2+2\omega_c s+\omega_0^2}$ $\omega_0 = 2\pi f\ (\mathrm{rad/s})$, $\omega_c = \pi \pm 10\% f(\mathrm{rad/s})$

Table 3. Controller design parameters.

Controller	Control Parameters	Transfer Function	GM (dB)	PM (deg)	Wcp (rad/s)	Wcg (rad/s)	ITAE	IAE
Id/Iq Current Control	$Kp = 0.08$, $Ki = 520$	$\frac{0.08(s+6500)}{s}$	33.9	51	1.73×10^3	3.17×10^5	85.95	19.70
	PRC	$\frac{0.08\left(s^2+25s+3.029\times10^6\right)}{s^2+3.029\times10^6}$	33.9	51	1.74×10^3	3.17×10^5	126.94	28.39
	MPRC	$\frac{0.08(s+5463)(s+449.2)}{s^2+319.6s+2.454\times10^6}$	33.9	41	2.2×10^3	3.17×10^5	127.78	28.66
	Lead–Lag	$\frac{0.04476(s+9721)}{(s+19.48)}$	39	57	1.61×10^3	3.17×10^5	87.23	19.95
Vdc Voltage control	$Kp = 0.13$, $Ki = 92$	$\frac{0.13(s+707.7)}{s}$	22.3	58	346	2.11×10^3	85.95	19.70

In addition, a closed-loop linear model was used to perform a disturbance rejection analysis. In the presence of input and output disturbances, it provided information about the designed controller. When a disturbance entered a system, the disturbance rejection plot could reveal information about the controller's effectiveness. The system responded quickly to controller disturbances in order to return to a stable state. Figure 6a shows a block diagram of input/output disturbance rejection and a comparison of the PI, lead–lag, PR, and MPR controls in a closed-loop input/output disturbance rejection.



(a)

Figure 6. *Cont.*

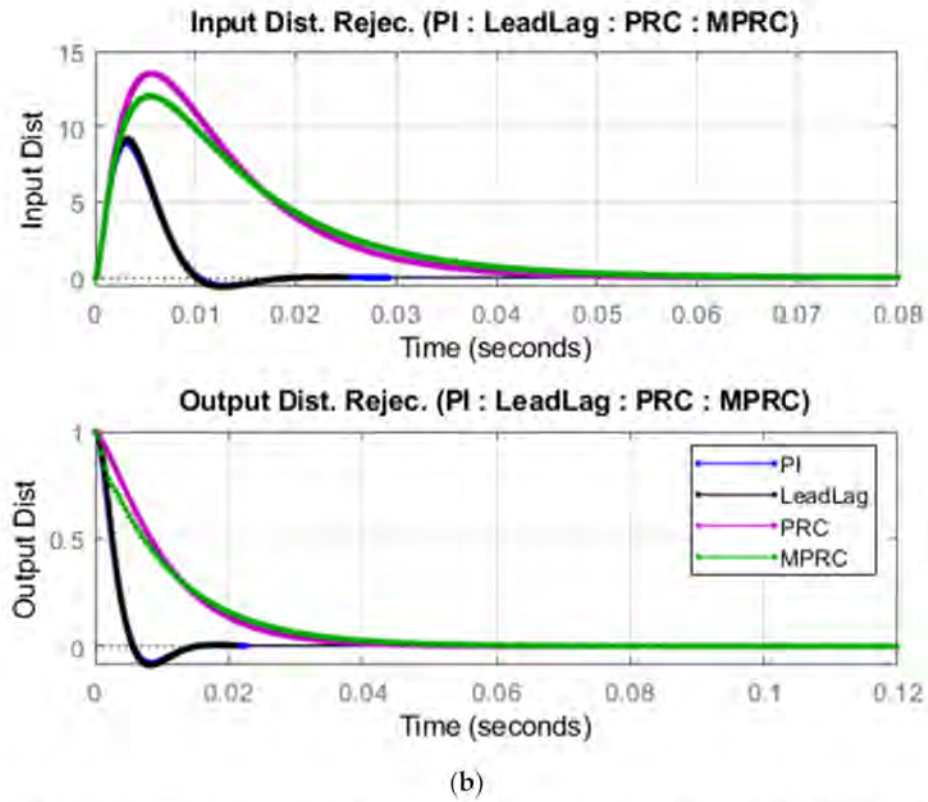


Figure 6. Disturbance rejection; (**a**) block diagram, (**b**) comparison of PI, lead–lag, PRC, and MPRC.

In the closed-loop Bode response comparison of all current controllers, displayed in Figure 5, the magnitude and frequency responses of the PI, lead–lag, PR, and MPR controllers were identical because all controllers were designed at the same gM, PM, ωcp, and ωcg. However, the disturbance rejection response of the outer loop voltage controller with the PI and lead–lag was different from the PR and MPR controls, as shown in Figure 6b. From all the above results, it was determined that the PI and lead–lag behaved equally. The PRC and MRPC responses, on the other hand, were slow, with a lot of overshoot and settling time. They were then implemented in a non-linear simulation after discretization of the sample time, as shown in the next section of simulation results. To gain more justification, a thorough comparison analysis of the PI, lead–lag, PR, and MPR controls was carried out.

4. Simulation Results

A simulation model for the off-board charger was developed to check the dynamic performances of the controller. Two major analyses were conducted in the simulation model: reference tracking and a disturbance rejection analysis. All simulation results were generated according to the parameters as shown in Table 3.

Different AC faults were injected into the simulation in the dynamic disturbance analysis to check the controller's behavior during and after a fault. For analysis and validation of controller performance, single-phase-to-line faults (1-line–ground), two-phase-to-line faults (2-line–ground), three-phase-to-line faults (3-line–ground), and line-to-line faults (line–line) were considered. Grid AC voltage and AC current during faults are shown in Figure 7.

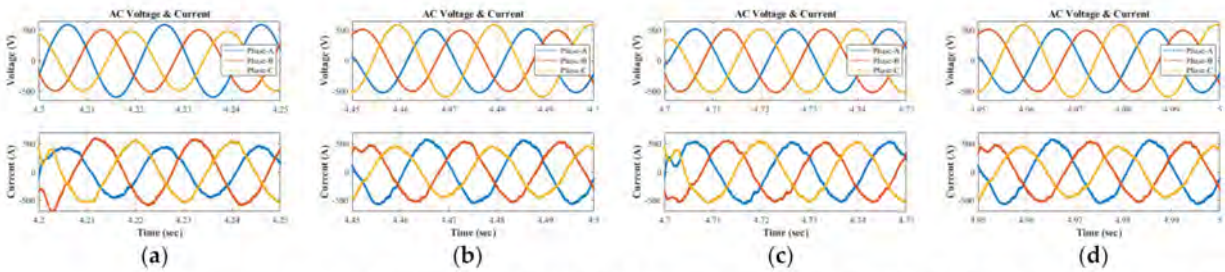


Figure 7. 3–phase AC faults; (**a**) 1 line–ground, (**b**) 2 line–ground, (**c**) 3 line–ground and (**d**) line–line.

The simulation results of the designed controllers are depicted in Figure 8. In this plot, red is the reference command, blue is the PI, black is lead–lag, magenta is PR, and green is MPR-based control. Initially, the DC reference was set to 650 V with no load. From 0 to 3.3 s, the converter related to the DC link capacitor pre-charge circuit, and after 3.3 s, the DC link capacitor was directly connected to the converter. At 3.5 s, a DC resistive load was connected to the converter. During this interval, PWM controller signals were not enabled and the system operated as a diode rectifier. At 3.8 s the controller was enabled, and it tracked the reference DC voltage of 650 V. Then, the DC reference changed from 650 V to 750 V at 4 s. In the results, all controllers follow the reference voltage command, but every controller has its own profile, as shown in Figure 8. Furthermore, step-by-step AC faults were inserted into the system to check the capability of the controllers. Faults of 1 line–ground, 2 line–ground, 3 line–ground and line–line were injected at different times: 4.2, 4.45, 4.7, and 4.95 s, respectively. The controllers performed well in all cases but had nonidentical overshoot, rise time, settling time, ITAE, and IAE.

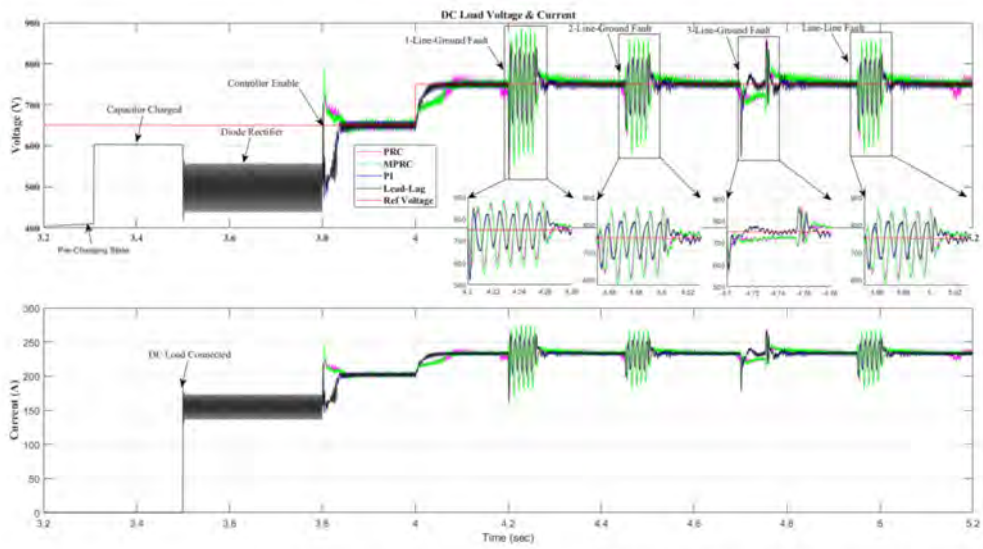


Figure 8. DC voltage and current comparison of PI, lead–lag, PRC, and MPRC controllers at 175 kW.

Table 3 and Figure 8 summarize the simulation results, which show that the PI and lead–lag behaved similarly and had less overshoot, rise time, settling time, ITAE, and IAE. PRC and MRPC responses, on the other hand, were unsatisfactory due to higher overshoot, ITAE, and IAE. As a result, both PI and lead–lag could be used to implement RT. In comparison to lead–lag, PI control on RT–FPGA is relatively simple to implement. As a result, for RT implementation, the PI controller was chosen.

The THD of the line current with the PI control was also estimated and observed at less than 5% at full load and at 20% of full load; the THD analysis is shown in Figure 9. The THD of the line current was calculated using the MATLAB Powergui tool of FFT analysis. The general mathematical representation of THD is as follows in Equation (10), the ratio

between the root mean square (RMS) of harmonic magnitude and RMS magnitude of the fundamental frequency of 50 Hz.

$$\text{THD} = \frac{\text{Total RMS current of harmonics}}{\text{RMS current of fundamental}} = \sqrt{\frac{\sum_{n=2}^{5} I_n^2}{I_1}} \times 100\ \% \tag{10}$$

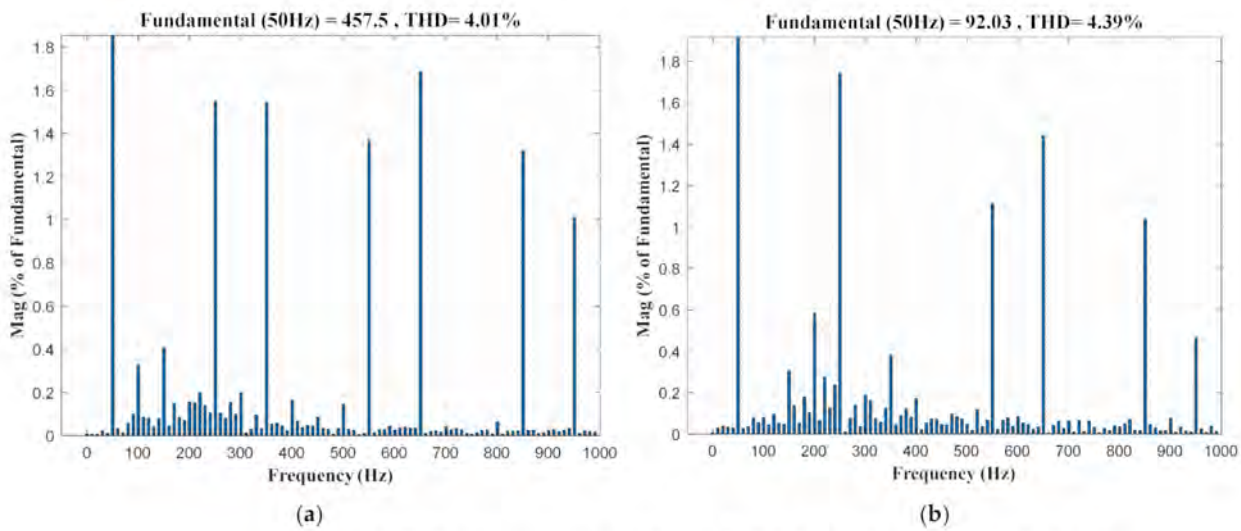


Figure 9. THD of line current; (**a**) full load, (**b**) 20% load following the standards < 5%.

5. Real-Time Control Implementation

This paper now introduces the practical RT implementation of the controller correlated with the XSG program. The controller of the off-board charger was designed in the z-domain, as depicted in Figure 8. An experimental setup was developed and employed in the laboratory to validate the controller's robustness. A dSPACE MicroLabBox with an embedded hardware board of Xilinx Kintex-7 XC7K325T FPGA was utilized to implement the control strategy [17]. The discrete control is shown in in Figure 10.

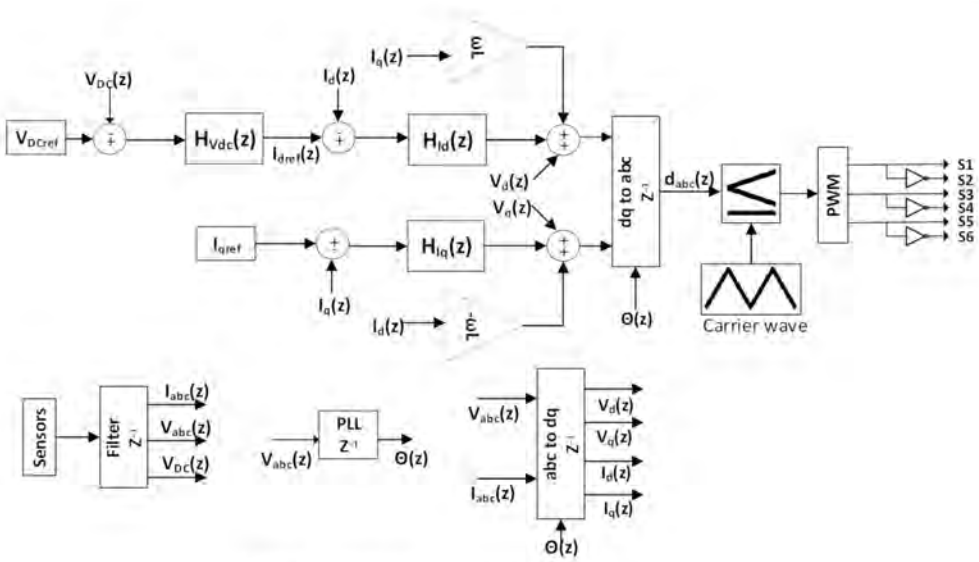


Figure 10. Digital control FPGA implementation.

5.1. Controller Sampling Time

The period clock of the FPGA of dSpace MicroLabBox was 10 ns. Therefore, the output digital PWM signals were generated at a sampling time of 10 ns. The controllers, analog sensing measurements, sensor filters, PLL, carrier wave, and all calculations (i.e., abc-dq0, dq0-abc, and trigonometric calculation) were performed at a sampling time of 10µsec. The FPGA block was designed in MATLAB/Simulink for the sampling time of the controller, as shown in Figure 11.

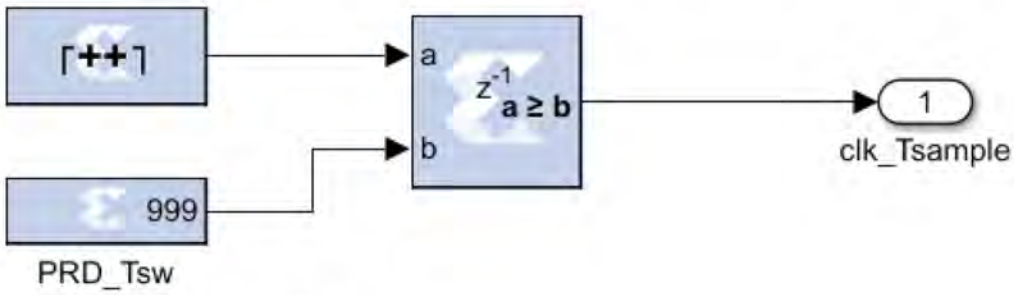


Figure 11. Block for sampling time (10 µs).

5.2. Sensors Calibration

5.2.1. Voltage Sensors

The analog voltage sense transducer (DVC 1000-P) was used for three-phase AC and DC voltage measurements. This voltage transducer gave output voltage in the range of 0 to 5 V maximum. The scaling factor of the sensors was calculated for the implementation of the RT controller (MicroLabBox). The 16-bit data came from the analog port of dSpace MicroLabBox of maximum (±10 V or $\left(\pm\frac{2^{16}}{2}\right)$). The voltage transducer's output was connected to the analog input port of MicrolabBox. The analog input of the voltage sensor was multiplied with a factor $\left(\frac{10}{32{,}676}\right)$ to convert it into the sensor output voltage [V] for the measurement of maximum ±1888 V. The scaling factor for the accurate voltage measurement is further elaborated on in Equation (11). Moreover, a 10th order moving average filter was integrated to wash out the noise of voltage sensors.

$$\text{Actual Voltage (V)} = \left(\text{Sensor Voltage}_{\text{out}} - 2.498\right) \times 754.6 \tag{11}$$

5.2.2. Current Sensors

The analog current sense transducer (ISB-425-A-YZZ) was used for three-phase AC and DC current measurements. This current sensor gave an output voltage in the range of 0 to maximum 5 V according to the factor of 4.706 mV/A. The scaling factor of the current sensors was calculated for the implementation of the RT controller (MicroLabBox). Similar to the voltage sensor, the 16-bit data came from the analog port of dSpace MicroLabBox of maximum (±10 V or $\left(\pm\frac{2^{16}}{2}\right)$). The current transducer output was connected to the analog input port of MicrolabBox. The analog input of the current sensor was multiplied with a factor $\left(\frac{10}{32{,}676}\right)$ to convert it into a sensor output voltage [V] for the measurement of maximum ±528 A. The scaling factor for the accurate current measurement is illustrated in Equation (12). Moreover, a 10th order moving average filter was integrated at the output of this block to wash out the noise of current sensors.

$$\text{Actual Current (A)} = \left(\text{Sensor Voltage}_{\text{out}} - 2.4825\right) \times 212.5 \tag{12}$$

5.3. Phase Lock Loop (PLL)

A PLL was used to calculate the phase angle and fundamental frequency based on the zero voltage crossing for the synchronization of converters to the AC grid. Furthermore,

the PLL was also utilized for grid synchronization, and for controlling and estimating state variables. PLL-based synchronization techniques are the most conventional and widely accepted [28,29]. Hence, RT–PLL was implemented on an FPGA to estimate the grid frequency and angle of three-phase grid voltages. The phase angle of the PLL was further used for Clarke (abc to dq0) and Park (dq0 to abc) transformations. The FPGA-based PLL implementation block is shown in Figure 12.

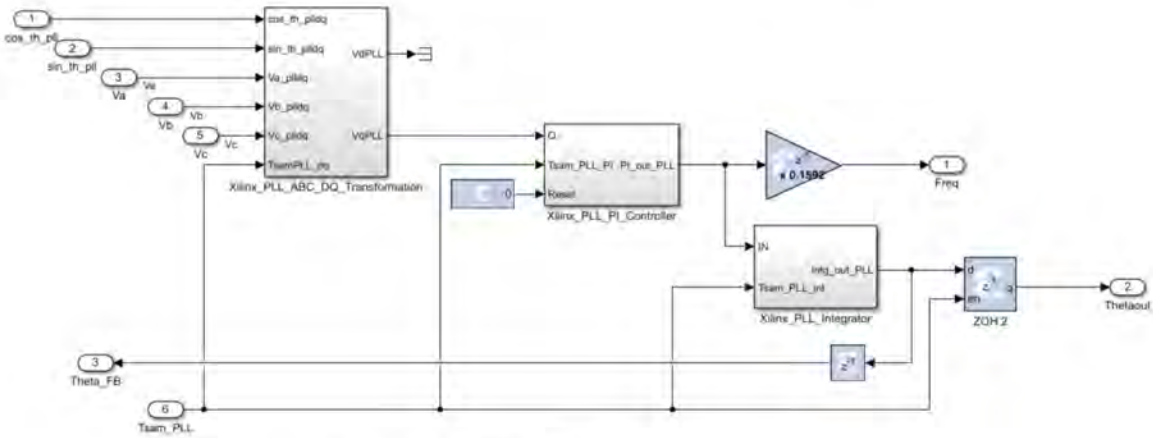


Figure 12. Phase lock loop (PLL).

5.4. PI Controller

Discrete PI controllers were implemented in RT–FPGA for dual-loop control, i.e., DC voltage ($H_{Vdc}(z)$), I_d ($H_{Id}(z)$), and I_q ($H_{Iq}(z)$) controls as shown in Figure 13. The outer voltage loop in the dual-loop control structure generated the reference current for the inner control loop of the current. Using methods similar to continuous-time frequency response methods, the digital PI controller was designed directly in the z-domain [23]. The transfer function of the digital z-domain PI controller is represented in Equation (13); T_s is the sampling time of the controller.

$$H(z) = K_p + \frac{K_i T_s z}{z - 1} \tag{13}$$

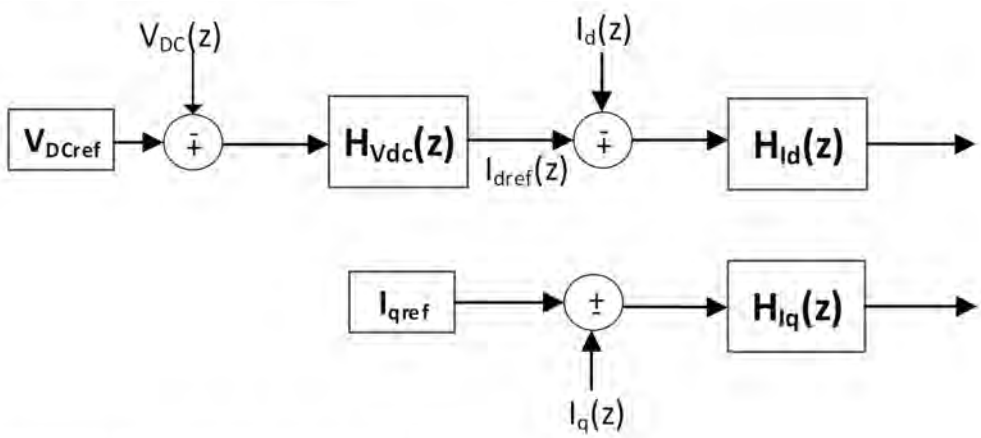


Figure 13. PI controller for voltage and current.

5.5. Clarke/Park Transformation

The transformation blocks (i.e., abc to dq0 and dq0 to abc) were designed and implemented in RT–FPGA for voltage and current measurements. The following equations were

implemented for dual loop voltage and current control design: Equations (14) and (15) for abc-to-dq transformation, and Equations (16)–(18) for dq-to-abc transformation.

$$V_d = \frac{2}{3}\left(\mathrm{Sin}(\theta)\ V_a + \frac{1}{2}\left(-\mathrm{Sin}(\theta)\ -\ \sqrt{3}\,\mathrm{Cos}(\theta)\right)V_b + \frac{1}{2}\left(-\mathrm{Sin}(\theta)\ +\ \sqrt{3}\,\mathrm{Cos}(\theta)\right)V_c\right) \tag{14}$$

$$V_q = \frac{2}{3}\left(\mathrm{Cos}(\theta)\ V_a + \frac{1}{2}\left(-\mathrm{Cos}(\theta)\ +\ \sqrt{3}\,\mathrm{Sin}(\theta)\right)V_b + \frac{1}{2}\left(-\mathrm{Cos}(\theta)\ -\ \sqrt{3}\,\mathrm{Sin}(\theta)\right)V_c\right) \tag{15}$$

$$V_a = \mathrm{Cos}(\theta)\ V_q + \mathrm{Sin}(\theta)\ V_d \tag{16}$$

$$V_b = \frac{1}{2}\left(-\mathrm{Sin}(\theta)\ -\ \sqrt{3}\,\mathrm{Cos}(\theta)\right)V_d + \frac{1}{2}\left(-\mathrm{Cos}(\theta)\ +\ \sqrt{3}\,\mathrm{Sin}(\theta)\right)V_q \tag{17}$$

$$V_c = -V_a - V_b \tag{18}$$

5.6. PWM Signals

The controller was designed at a switching frequency of 40 kHz. Therefore, a triangular wave was generated in RT–FPGA at 40 kHz. The amplitude of the triangular wave was 2 (by multiplying with 0.0016). In addition, this triangular wave was used to generate 40 kHz PWM signals by comparing it with the controller's duty cycle (magnitude between 0 and 2), as shown in Figure 14.

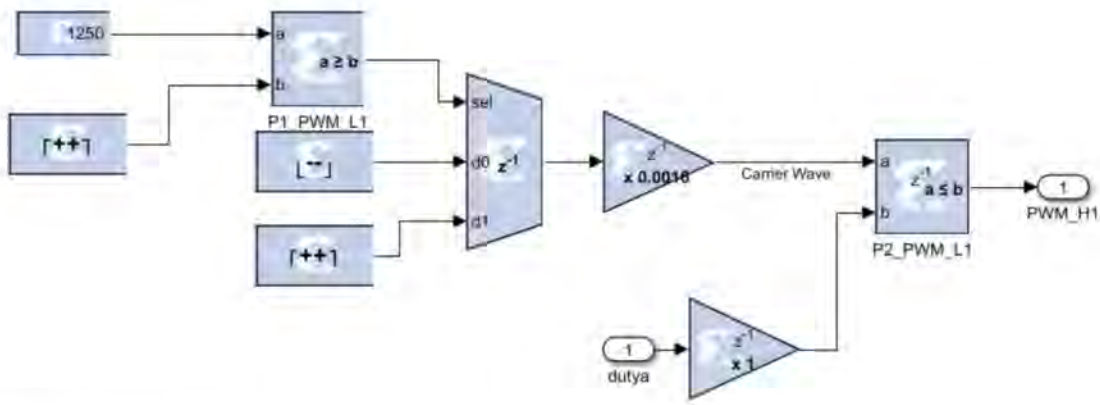


Figure 14. PWM generation.

6. Experimental Setup and Results

6.1. Experimental Setup

A three-phase AC grid and a DC resistive load were connected to create the test setup. The off-board charger was powered by a three-phase grid. The three LC filters of 100 uH–10 uF were connected on the grid side of the converter, as depicted in Figure 15. Ten DC link capacitors of 85 uF were connected on the DC side of the converter as shown in Figure 16b. Two snubber capacitors of 220 uF were connected at the drain–source of each half-bridge module. Four analog voltage transducers (DVC 1000-P) and four current transducers were used to measure current and voltage on both the DC and AC sides of the charger (ISB-425-A-YZZ). For testing, the lab resistor bank was used as a DC load. A double-sided liquid cooling system was connected to the radiator as shown in Figures 15 and 16b, and all temperature data were logged on a computer drive by temperature sensors and an infrared thermal camera. The SiC technology-based Infineon double-sided half-bridge power electronics (PE) modules and the dual-sided liquid cooling system, explicitly developed for the HiPerform EU project, are shown in Figure 16a,b. For the generation of 40 kHz PWM square wave signals, the real-time controller was implemented on the dSpace MicroLabBox. The dSpace GUI was designed to provide reference commands, monitoring, and measurements, such as DC voltage, DC current, and

three-phase AC voltage and current. All experimental data was logged in the computer database. The testing setup of the charger is shown in Figure 15.

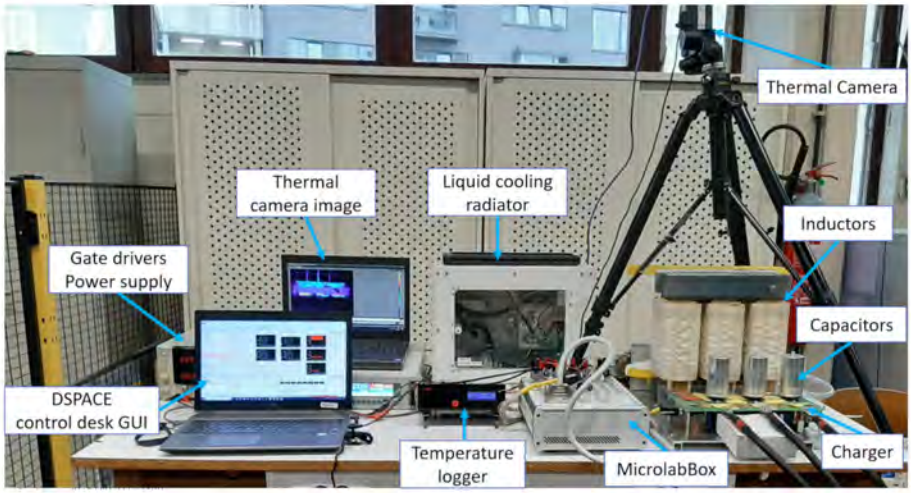


Figure 15. Off–board charger test setup.

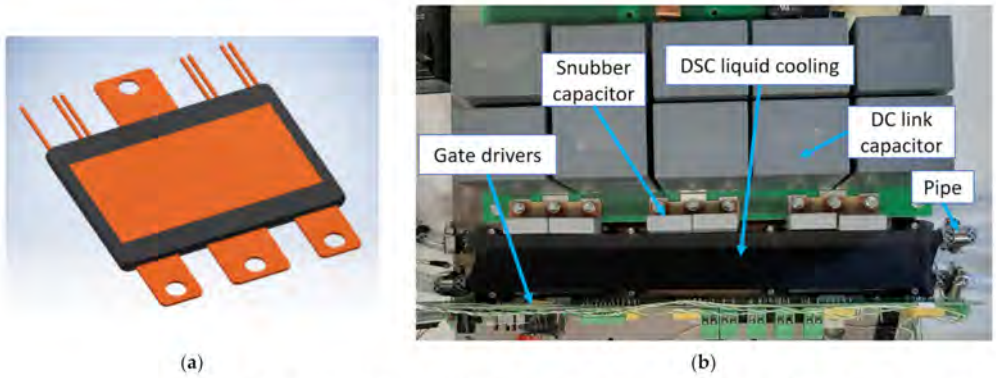


Figure 16. AFE with liquid cooling; (**a**) half–bridge DSC module, (**b**) DSC modules with plates.

6.2. Experimental Results

The real-time off-board charger voltage–current controller was implemented on the FPGA of dSpace MicroLabBox at 40 kHz switching frequency. The data acquisition was made with MicroLabBox. The charger's voltages, currents, and enable flags data were logged at a sampling frequency of 0.1 kHz. The logged parameters included line-to-line voltages v_{ab}, v_{bc}, v_{ca} [V], three-phase currents i_a, i_b, i_c [A], and DC input current i_{dc} [A] and voltage V_{dc} [V].

The goal of the test was to ensure that the controller worked properly in the experimental setup. As a result, this test was carried out at one third of the 400 V phase voltage. The controller's performance was put to the test in two ways. By changing the reference command to 50 V in test 1, DC voltage reference tracking was tested. Figures 17 and 18 show the DC and AC current and voltage responses, respectively. In test 2, a variation of the DC load was tested at a fixed voltage reference. DC voltage and three-phase AC current responses are depicted in Figure 19. The controller was practically observed to track the reference signal in both tests successfully. Two spikes of 15 V in measured DC voltage in Figure 19 occurred because of the sudden change of load. The resistive load increased at 950 s and then reduced to the initial state at 961 s. The resistive load increased at 950 s and then reduced to the initial state at 961 s. The THD of the line current from experimental data was 4.97%, as depicted in Figure 20, and efficiency was 97% at 12 kW power.

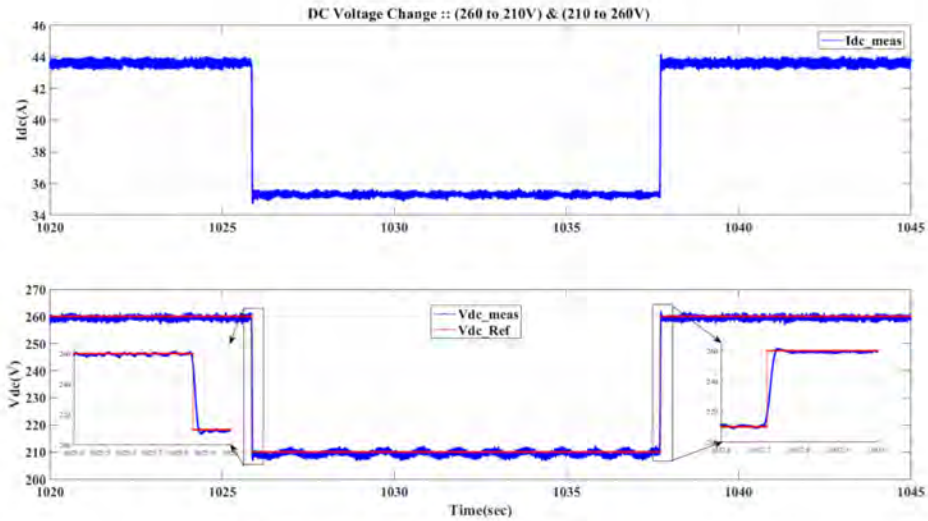


Figure 17. Test 1: DC voltage reference tracking.

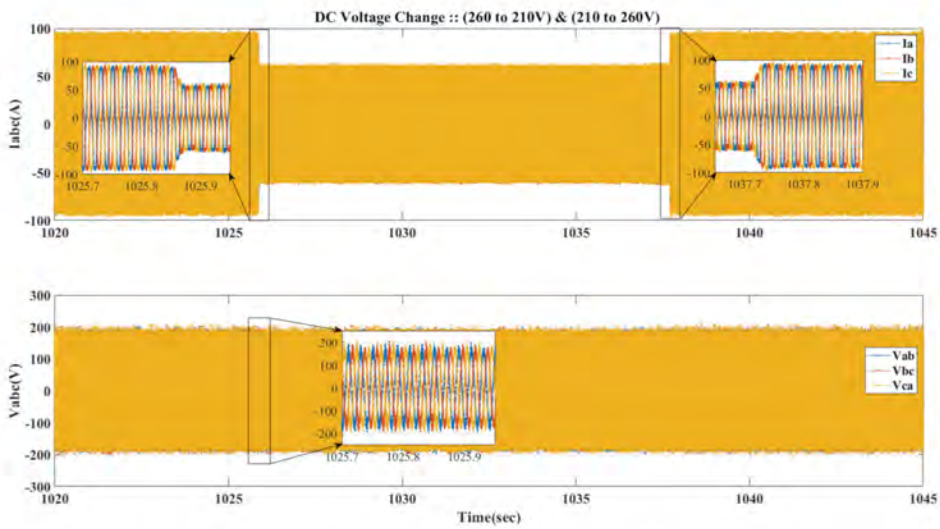


Figure 18. Test 1: Three–phase AC voltages and currents.

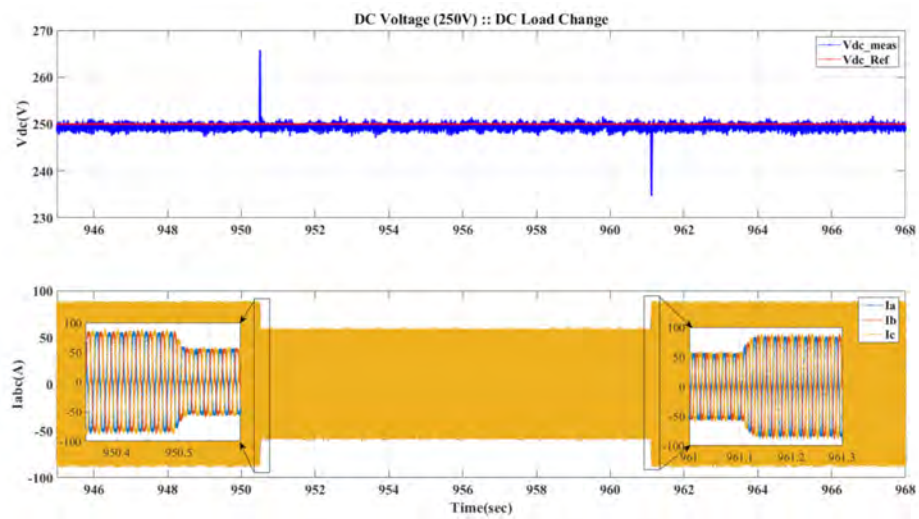


Figure 19. Test 2: DC voltage and three–phase AC currents.

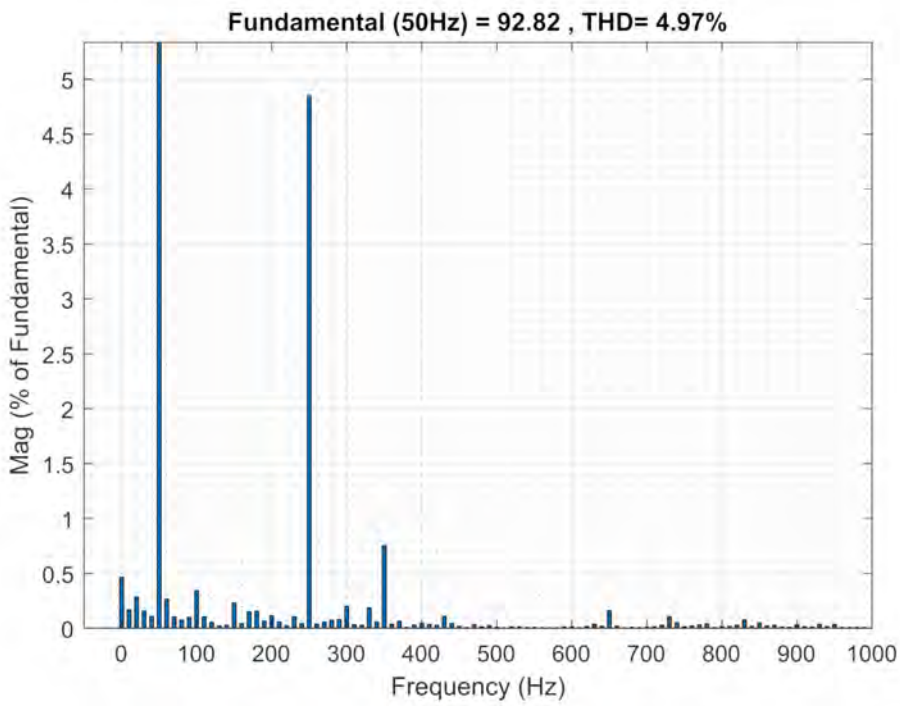


Figure 20. Experimental THD of line current.

7. Conclusions

In this paper, the modeling, design control, and implementation of a next-generation SiC-based off-board charger for BEBs are described. Such charging infrastructure will be required in the near future to deal with the growing number of BEBs in cities and their heavy load on the electricity grid. SiC switches operate at a high switching frequency and allow for high energy savings and better power quality compared to Si-technology. Nonetheless, dealing with their fast dynamics necessitates accurate modeling and control design. Therefore, a linear and non-linear MATLAB simulation model of the off-board charger were developed. System performance was verified in simulation through the evaluation of reference tracking, system ripples, and THD of the line current. Four types of controllers, i.e., PI, lead–lag, PR, and MPR, were designed with a linear model and validated in a non-linear simulation model. In terms of performance and RT implementation, it is concluded that the PI controller is a better choice than other controllers. The designed controller had a gain margin of 22.3, a phase margin of 58°, and achieved a minimum ITAE of 19.70 and IAE of 85.95. The line current THD was below 5% and the PF above 99%. A dual-loop voltage and current control were successfully implemented and tested on the FPGA of a dSpace MicroLabBox at 40 kHz switching frequency. The provided experimental results of the control system demonstrated the correct operation of the real-time implementation of the controller by tracking the reference command, thus enabling the off-board charger for BEBs used in public transport.

As the infrastructure of charging plays a key role in the deployment of BEBs, robust control design is essential to achieve a highly efficient and reliable fast-charging system. Nevertheless, proper control architecture design still needs to be developed for a bidirectional operation, i.e., the V2G and G2V of the chargers and the correction of unbalanced voltage in the grid, with the implementation of controls for WBG devices operating at high switching frequencies. This will need to be tackled in future research.

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Conflicts of Interest: The authors declare no conflict of interest.

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